iT4032D
50-ps Wideband Phase Delay With 180-deg. Flipper
(Advanced Information)

Description

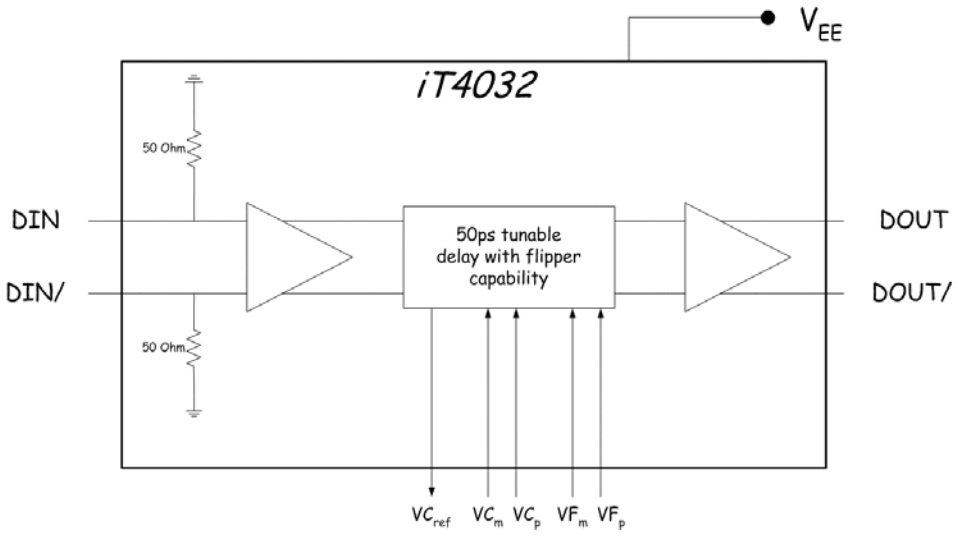
The iT4032D is an ultra-wideband phase delay fabricated using 0.1-µm HBT GaAs technology. The high output voltage, excellent rise and fall times, and the high eye diagram quality at all data rates up to 12.5 Gb/s makes the iT4032D suitable for timing adjustment in data and clock distribution at a very high speed. Complex digital applications that can benefit from the iT4032D include clock data recovery, edge detectors, NRZ/RZ converters, MUX/DEMUX, and data restoration It is based on an ECL topology in order to guarantee high-speed operation. The device features a single delay element that provides up to 50 ps delay and a 180 deg. shift capability.

The delay control can be either differential (using both VCp and VCm) or single-ended (VCp is the active control pad while VCm is shorted to VCref). The nominal control voltage range for the delay is from -2.2 V to -3.0 V, whether the control is single-ended or differential. The flipping control can be either differential (using both VFp and VFn), or single-ended (VFp is the active control pad while VFm is shorted to VCref). The nominal control voltage for the flipping is -2.2 V or -3.0 V whether the control is single-ended or differential. The device is capable of delaying NRZ streams with a data rate up to 12.5 Gb/s or a clock signal with frequency up to 10.7 GHz. The inputs and the outputs are DC coupled. At the input side the internal 50-ohm resistors avoid the need for external impedance matching terminations. The iT4032D uses SCFL I/O levels and is designed so to allow for either single ended or differential data input.

Features

- Wideband signal handling: up to 12.5 Gb/s NRZ
- Delay adjustment: to 50 ps
- Flipping capability (180 deg. shift)
- 900 mVpp typical single-ended output
- Jitter RMS: <1.5 ps
- Output rise time (20% – 80 %): <22 ps
- Output fall time (20% – 80 %): <20 ps
- 50-ohm matched DC-coupled inputs and outputs
- Differential or single-ended I/O
- Power consumption: 1.15 W

Device Diagram



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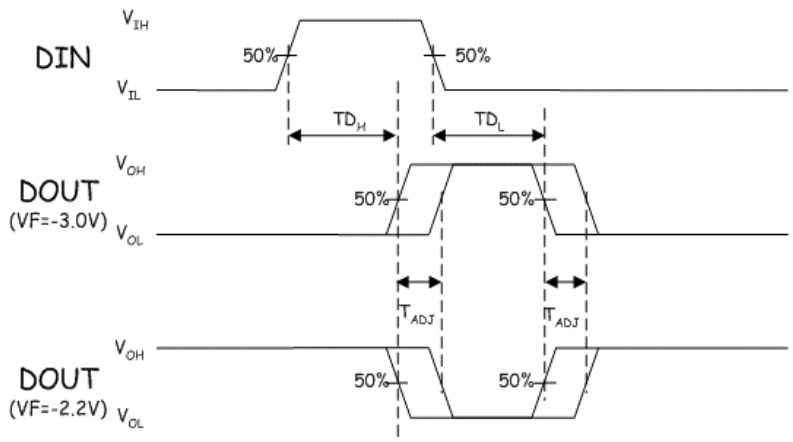
Timing Diagram



Absolute Maximum Ratings

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameters/conditions	Min.	Max.	Units
V_{EE}	Power supply voltage	-5.5	0	V
V_{IH}	Input voltage level, high level	-1.5	1.5	V
V_{IL}	Input voltage level, low level	-1.5	1.5	V
VC	Delay control voltage	-5.0	0	V
VF	Flipping control voltage	-5.0	0	V
T_A	Operating temperature range – die	-15	125	°C
T_{STG}	Storage temperature	-65	150	°C

Recommended Operational Conditions

Symbol	Parameters/conditions	Min.	Typ.	Max	Units
T_A	Operating temperature range – die	0		85	°C
V_{EE}	Power supply voltage		-5		V
VC	Delay control voltage	-3.0	-2.6	-2.2	V
VF	Flipping control voltage	-3.0		-2.2	V
V_{IH}	Input voltage level, high level (single ended)		0.0		V
V_{IL}	Input voltage level, low level (single ended)		-0.9		V
V_{INDC}	DC input voltage (with DC-coupled input)		-0.45		V

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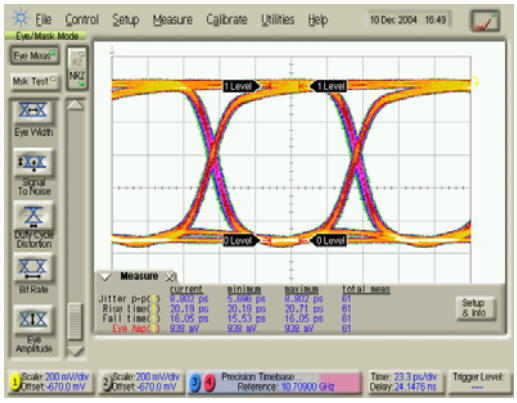
Electrical Characteristics

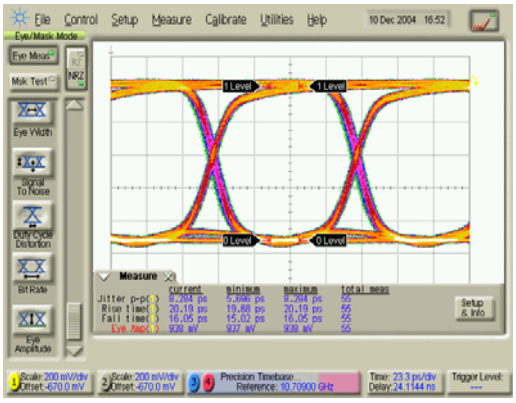
Symbol	Parameters	Min	Typ	Max	Units
V_{EE}	Power supply voltage	-4.5	-5.00	-5.25	V
V_{IH}	Input voltage level, high level (single ended)		0.0		V
V_{IL}	Input voltage level, low level (single ended)		-0.9		V
V_{INDC}	DC input voltage (with DC-coupled input) (2)		-0.45		V
V_{OUT}	Data output voltage amplidude (3)	0.8	0.9	1.0	V
T_R	Output rise time (20% – 80%)		22		ps
T_F	Output fall time (20% – 80%)		20		ps
TD_H	Output delay low-high transition(4)		180		ps
TD_L	Output delay high-low transition(4)		180		ps
T_{ADJ}	Output phase delay adjustment(4)		50		ps
S_{11}	Input return loss (up to 15 GHz)		23		dB
S_{22}	Output return loss (up to 15 GHz)		8		dB
F_{MAX}	Maximum clock frequency		10.7		GHz
J_{p-p}	Peak-to-peak jitter(5)		9		ps
J_{rms}	RMS jitter(5)		1.5		ps
I_{EE}	Power supply current		230		mA
P_D	Power dissipation		1.15		W

1. Electrical characteristics at ambient temperature.
2. In case of single-ended input the unused pin has to be tied to VINDC.
3. In case of single-ended output, the unused pad must be terminated with 50 ohms to ground.
4. Refer to timing diagram.
5. On a 10.7 Gb/s PRBS pattern.

Eye Diagram Performance



Die measurement
Vee: -5.0 V Input data rate: 10.7 Gb/s
Single-ended data input: +/-450 mVpp
Control voltage: VCm= VFm =VCREF
VCp=-2.2 V; VFp=-3.0 V



Die measurement
Vee: -5.0 V Input data rate: 10.7 Gb/s
Single-ended data input: +/-450 mVpp
Control voltage: VCm=VFm=VCREF;
VCp =-3.0 V; VFp =-3.0 V

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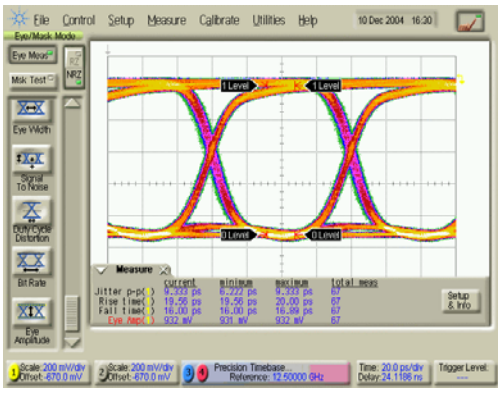
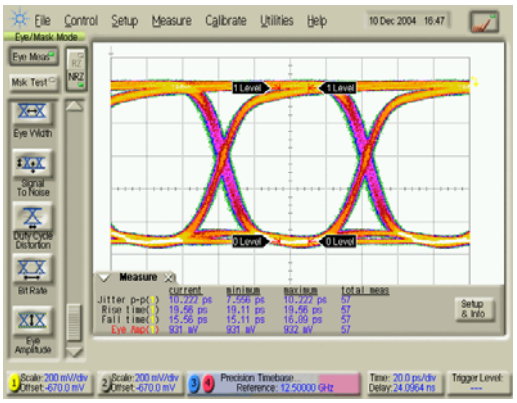
Eye Diagram Performance (cont.)



Die measurement
Vee: -5.0 V
Input data rate: 12.5 Gb/s
Single-ended data input: +/-450 mVpp
Control voltage: VCm=VFm=VCREF;
VCp=-2.2 V; VFp=-3.0 V



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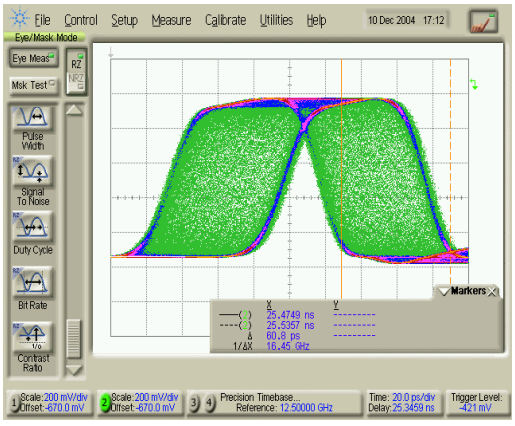
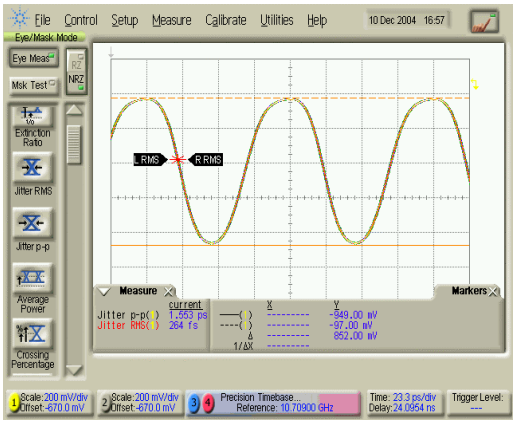


Die measurement
Vee: 5.0 V
Input data rate: 12.5 Gb/s
Single-ended data input: +/-450 mVpp
Control voltage: VCm=VFm=VCREF;
VCp=-2.2 V to -3 V (accumulating); VFp=-3.0 V



Die measurement
Vee: 5.0 V
Input data rate: 10.7 Gb/s
Single-ended clock input: +/-450 mVpp
Control voltage: VCm=VFm=VCREF;
VCp=-2.2 V to -3 V (accumulating); VFp=-3.0 V

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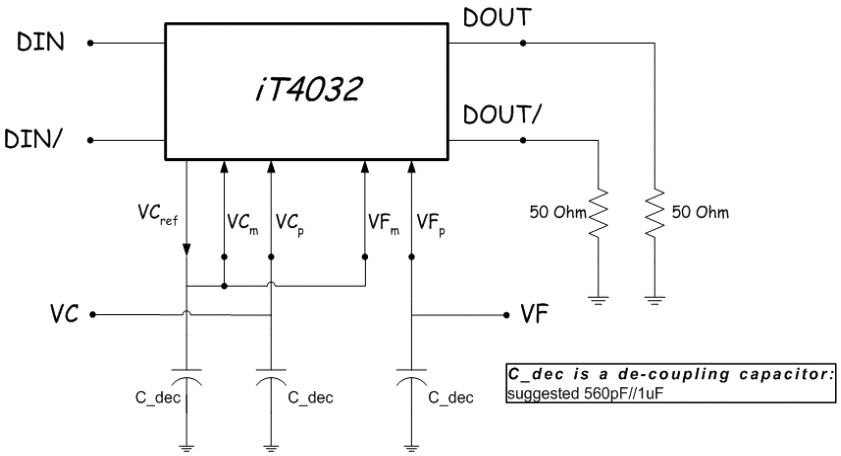
Recommended Operational Setup



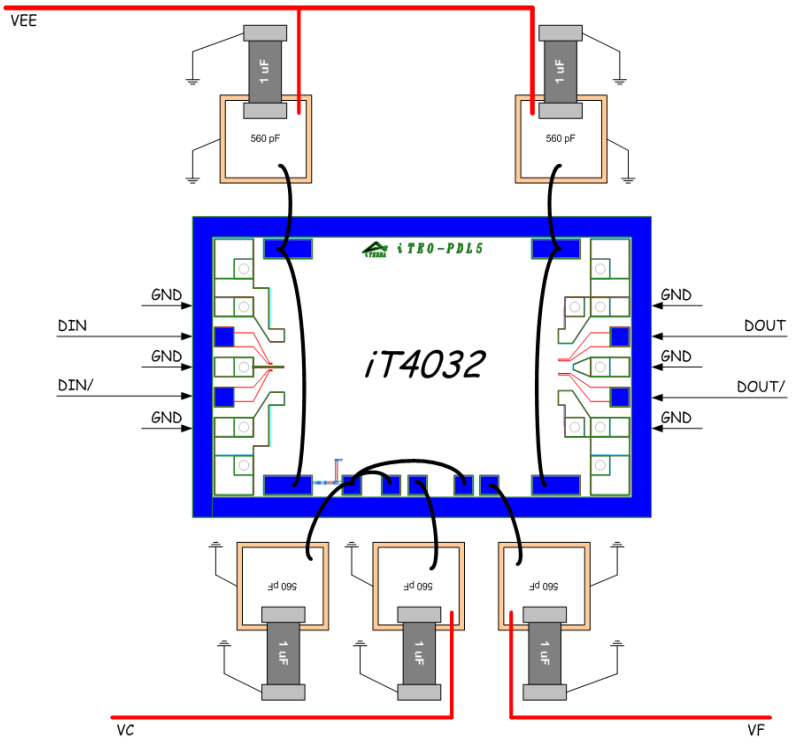
Recommended Chip Mounting

Chip size
2235 µm ±10 µm
x 1400 µm ±10 µm

Chip thickness: 104 µm ±3 µm

Pad size: 100 µm
x 100 µm

RF pad pitch: 150 µm



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Pad Positions And Dimensions

Chip size:
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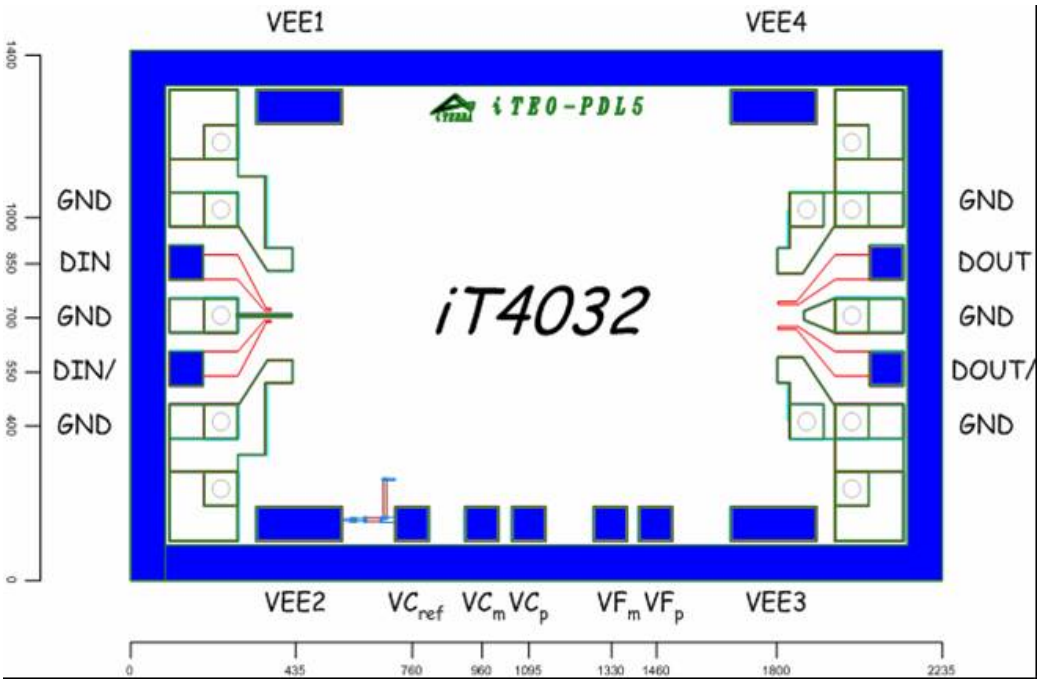
Chip thickness: 104 µm ±3 µm

Pad size: 100 µm x 100 µm

RF pad pitch: 150 µm



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