PALC22V10H-25/35
PALC22V10H-25/30/40

24-Pin Universal CMOS PAL® Device

DISTINCTIVE CHARACTERISTICS

- **CMOS technology cuts power in half (90 mA commercial/100 mA military) while matching bipolar 22V10 speed**
- **10 input/output macrocells for architectural flexibility**
- **Varied product term distribution**
  – Up to 16 product terms per output
- **Outputs programmable as registered or combinatorial**
- **Programmable output polarity**
- **Global register asynchronous reset and synchronous preset**
- **Preloadable output registers for testability**
- **Automatic register reset on power-up**
- **Erasable in windowed 24-pin SKINNYDIP® package**
- **Cost-effective OTP 24-pin SKINNYDIP packages and 28-pin Plastic Leaded Chip Carriers**
- **High-speed CMOS technology**
  – 25 ns t_{PD} for "-25" commercial version
  – 35 ns t_{PD} for "-35" commercial version
  – 25 ns t_{PD} for "-25" military version
  – 30 ns t_{PD} for "-30" military version
  – 40 ns t_{PD} for "-40" military version

GENERAL DESCRIPTION

The PALC22V10 is a second-generation Programmable Array Logic (PAL) device built with low-power CMOS technology. It utilizes the familiar sum-of-products (AND-OR) logic structure, allowing users to program custom logic functions. The PALC22V10 permits the development of custom LSI functions of 500 to 800 equivalent gate complexity.

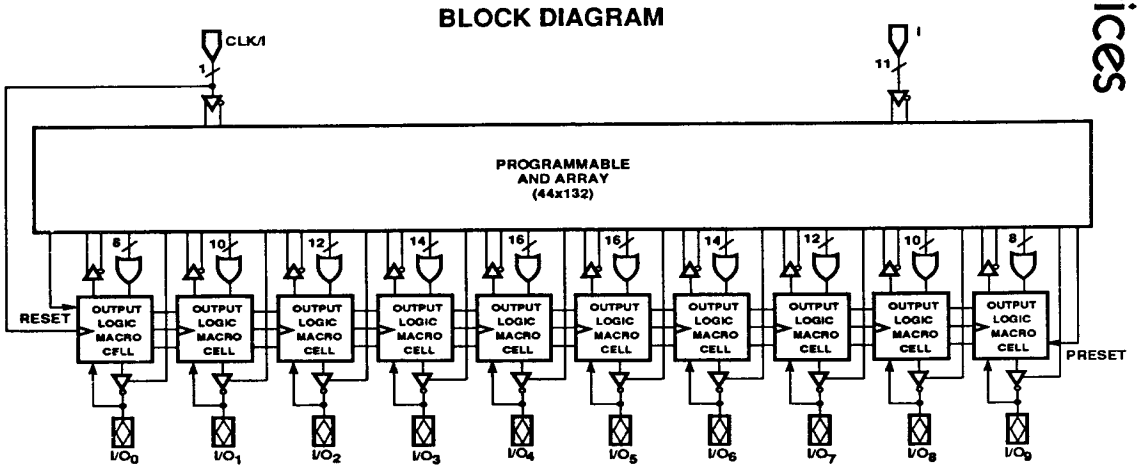
The PALC22V10 contains up to 22 inputs and 10 outputs. It incorporates the unique capability of defining and programming the architecture of each output on an individual basis. Each output is user-programmable for either registered or combinatorial operation. This allows the designer to optimize the device design by having only as many registers as needed. In addition, each output has user-programmable output polarity, further simplifying design and contributing to the precise application requirements.

Increased logic power has been built into the PALC22V10 by increasing the number of product terms from eight per output to an average of twelve per output. Further innovation can be seen in the introduction of varied product-term distribution. This technique allocates from eight to sixteen logical product terms to each output (please refer to the Block Diagram for distribution details). This varied allocation of terms allows far more complex functions to be implemented than in previous devices.

System operation has been enhanced by the addition of a synchronous-PRESET and an asynchronous-RESET product term. These terms are common to all output registers.

The PALC22V10 also incorporates power-up RESET and the capability to PRELOAD the output registers to any desired state during testing. PRELOAD is essential to permit full logical verification during test.

BLOCK DIAGRAM



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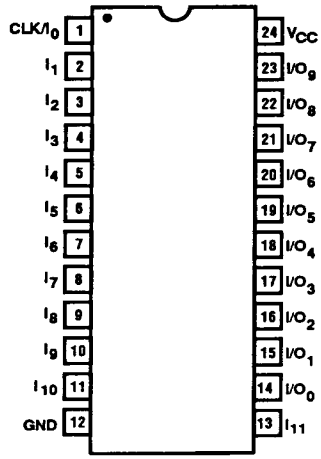
* This part is covered by various U.S. and foreign patents owned by Advanced Micro Devices.

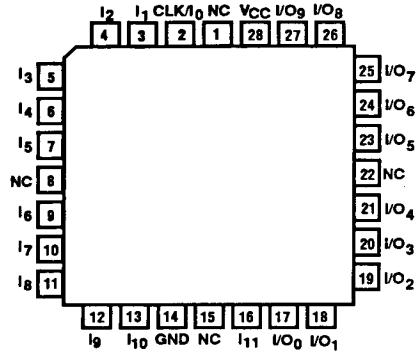
CONNECTION DIAGRAMS
(Top View)

SKINNYDIP



Note: Pin 1 is marked for orientation

PLCC/LCC



Pin Designations:

I	= Input
I/O	= Input/Output
V_{CC}	= Supply Voltage
GND	= Ground
CLK	= Clock
NC	= No Connection

ORDERING INFORMATION

Standard Products

AMD/MMI standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed/Power Option (If applicable)
c. Temperature Range
d. Package Type
e. Optional Processing

PAL C 22 V 10 H-25 C NS

a. DEVICE NUMBER/ DESCRIPTION PROGRAMMABLE ARRAY LOGIC

CMOS TECHNOLOGY

NUMBER OF ARRAY INPUTS

OUTPUT TYPE
V = Versatile

NUMBER OF FLIP-FLOPS

b. SPEED/POWER OPTION
H-25 = 25 ns (Half Power)
H-35 = 35 ns (Half Power)

c. TEMPERATURE RANGE
C = Commercial (0°C to +75°C)

d. PACKAGE TYPE
NS = 24-Pin Plastic SKINNYDIP
JS = 24-Pin Ceramic SKINNYDIP
QS = 24-Pin Windowed Ceramic SKINNYDIP
FN = 28-Pin Plastic Leaded Chip Carrier

e. OPTIONAL PROCESSING
Blank = Standard processing

Valid Combinations	
PALC22V10H-25	NS,JS,QS,FN
PALC22V10H-35	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

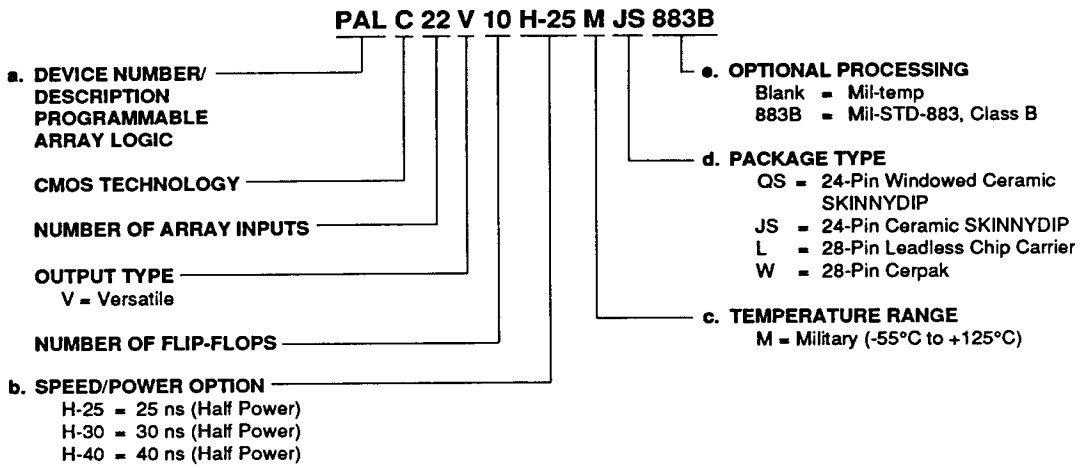
Note: Devices are marked with MMI logo.

ORDERING INFORMATION (cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883, Class B requirements. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed/Power Option (if applicable)
c. Temperature Range
d. Package Type
e. Optional Processing



Valid Combinations	
PALC22V10H-25	QS, JS, W, L
PALC22V10H-30	
PALC22V10H-40	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations.

Group A Tests

Group A Tests consist of Subgroups: 1, 2, 3, 7, 8, 9, 10, 11.

Note: Devices are marked with MMI logo.

Combination	Military Case Outline MIL-M-38510 Appendix C
QS	X
JS	L
L	3
W	K

FUNCTIONAL DESCRIPTION

The PALC22V10 is a second-generation Programmable Array Logic device. It contains a programmable array organized in the familiar sum-of-products (AND-OR) structure.

The block diagram below shows the basic architecture of the PALC22V10. There are up to 22 inputs and 10 outputs available. The inputs are connected to a programmable-AND array which contains 120 logical product terms. Initially the AND gates are connected to both the TRUE and COMPLEMENT of every input. By selective programming of connections, the AND gates may be "connected" to only the TRUE input (by programming the COMPLEMENT bit), to only the COMPLEMENT input (by programming the TRUE bit), or to neither type of input (by programming both bits), establishing a logical "don't care." When both the TRUE and COMPLEMENT bits are left intact, a logical FALSE results on the output of the AND gate. An AND gate with all bits programmed will assume the logical-TRUE state. The outputs of the AND gates are connected to fixed-OR gates. There is an average of 12 product terms per OR gate (output), and as the Block Diagram shows, varied product term distribution has been implemented. This technique allocates different quantities of logical product terms to different outputs, allowing more complex logical functions to be performed than were previously possible. Up to 16 logical terms can be evaluated in one output in a single clock cycle (no feedback necessary).

Output Logic Macrocells

A dramatic innovation in logic design is the implementation on the PALC22V10 of variable output architecture. This allows the user to program, on an output-by-output basis, the function of the outputs. As shown in the Output Logic Macrocell (OLM) diagram below, each output cell contains two additional bits, S_0 and S_1. S_1 controls whether the output will be registered or combinatorial. S_0 controls the output polarity (active HIGH or active LOW). Depending on the states of these two bits, an individual output will operate in one of four modes (see the logic diagrams on the next page): Registered/Active LOW, Registered/Active HIGH, Combinatorial/Active LOW, and Combinatorial/Active HIGH (note that the feedback path also changes with output mode). This innovation gives the designer more flexibility and enables optimization of the device for precise application requirements. It also allows for better device utilization – programming only as many registers as are needed.

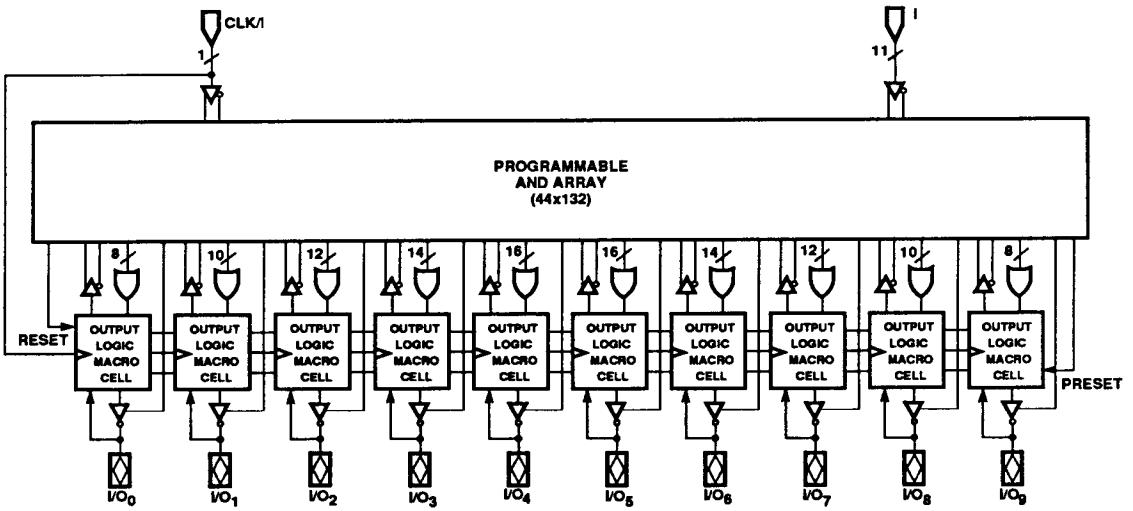
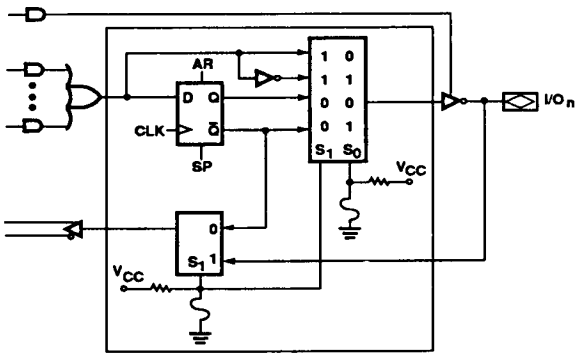


Figure 1. Block Diagram



S_1	S_0	Output Configuration
0	0	Registered/Active LOW
0	1	Registered/Active HIGH
1	0	Combinatorial/Active LOW
1	1	Combinatorial/Active HIGH

0 = Unprogrammed bit

1 = Programmed bit

Figure 2. Output Logic Macrocell Diagram

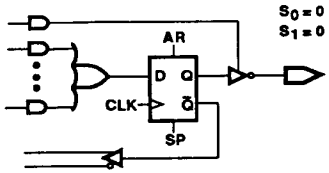


Figure 3-1. Registered/Active LOW

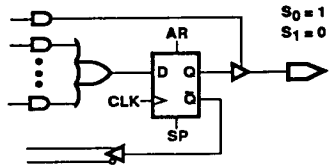


Figure 3-2. Registered/Active HIGH

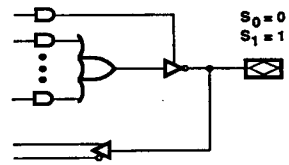


Figure 3-3. Combinatorial/Active LOW

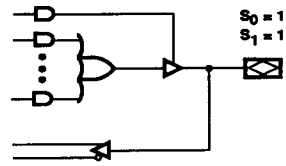


Figure 3-4. Combinatorial/Active HIGH

PRESET/RESET

To improve in-system functionality, the PALC22V10 has additional PRESET and RESET product terms. These terms are connected to all registered outputs. When the synchronous-PRESET product term is asserted (HIGH), the output registers will be loaded with a HIGH on the next LOW-to-HIGH clock transition. When the asynchronous-RESET product term is asserted (HIGH), the output registers will be immediately loaded with a LOW (independent of the clock). These functions are particularly useful for applications such as system power-on and reset.

PRELOAD

To simplify testing, the PALC22V10 is designed with PRELOAD circuitry that provides an easy method of testing registered devices for logical functionality. PRELOAD allows any arbitrary state value to be loaded into the output registers.

A typical functional test sequence would be to verify all possible state transitions for the device being tested. To verify these transitions requires the ability to set the state registers into an arbitrary "present state" value. Once this is done, the state machine is then clocked into a new state, or "next state." The next state is then checked to validate the transition from the present state. In this way any state transition can be checked.

Security Bit

After programming and verification, a PALC22V10 design can be secured by programming the security bit. Once programmed, this bit defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs.

Quality and Testability

The PALC22V10 offers a very high level of built-in quality. Extra programmable bits and the erasability of the device provide a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

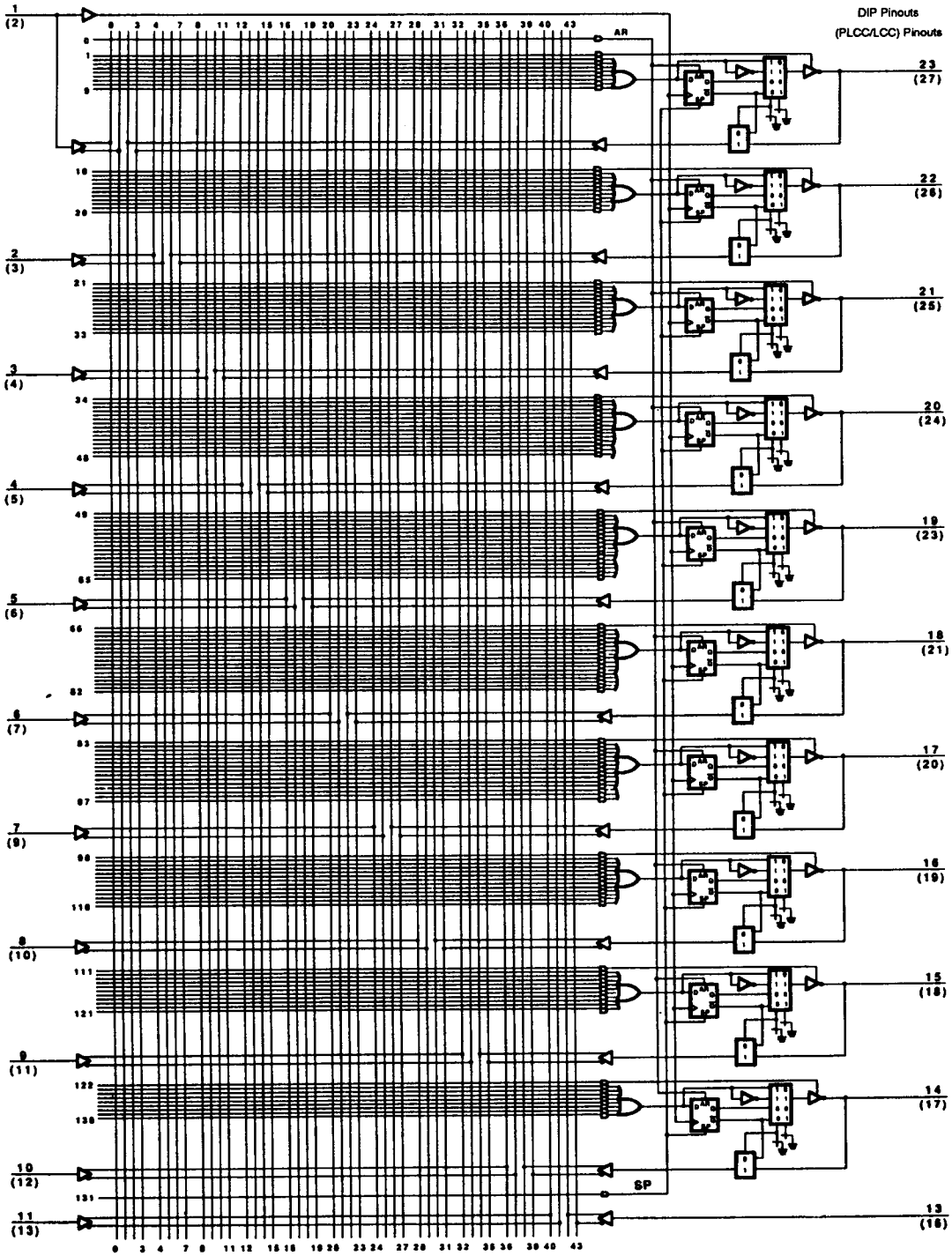


Figure 4. Logic Diagram

ABSOLUTE MAXIMUM RATINGS

Storage temperature ..... -65°C to +150°C
Supply voltage to ground potential
(Pin 24 to Pin 12) Continuous ..... -0.5 V to +7 V
DC voltage applied to outputs
(except during programming) ..... -0.5 V to +7 V
DC input voltage ..... -3 V to +7 V
DC output current into outputs ..... 16 mA
Ambient temperature with power applied ..... -55°C to +125°C
UV light exposure ..... 7258 W-sec/cm^2
Static discharge ..... >2001 V
Latchup current (T_A = 0°C to +75°C) ..... >100 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) devices
Temperature (T_A) Operating free air ..... 0°C to +75°C
Supply Voltage (V_{CC}) ..... +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS Over commercial operating range unless otherwise specified.

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –3.2 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16 mA		0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Current (Note 3)	V_{CC} = Max., V_{IN} = 2.4 V			-10	µA
I_{IL}	Input LOW Current (Note 3)	V_{CC} = Max., V_{IN} = 0.40 V			10	µA
I_I	Input HIGH Current	V_{CC} = Max., V_{IN} = 5.5 V			10	µA
I_{OS}	Output Short-Circuit Current	V_{CC} = Max., V_{OUT} = 0.5 V (Note 2)		-30	-90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., V_I = GND, Outputs Open			90	mA
I_{OZH}	Output Leakage Current (Note 3)	V_{CC} = Max., V_{IN} = V_{IL} or V_{IH}	V_O = 2.4 V		40	µA
I_{OZL}			V_O = 0.4 V		-40	

Notes: 1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. No more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.
3. I/O pin leakage is the worst case of I_{OZX} or I_{IX} (where X = H or L).

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V at f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V at f = 1 MHz	8	

Notes: 1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS Over commercial operating range unless otherwise specified (Note 1).

Parameter Symbol	Parameter Description		-35		-25		Unit
			Min.	Max.	Min.	Max.	
t_{PD}	Input or Feedback to Non-Registered Output (Note 2)	Active LOW		35		25	ns
		Active HIGH					
t_S	Setup Time from Input, Feedback or SP to Clock		25		15		ns
t_H	Hold Time		0		0		ns
t_{CO}	Clock to Output			25		15	ns
t_{CF}	Clock to Feedback (Note 3)			18		13	ns
t_{AR}	Asynchronous Reset to Registered Output			35		25	ns
t_{ARW}	Asynchronous Reset Width		35		25		ns
t_{ARR}	Asynchronous Reset Recovery Time		35		25		ns
t_{SPR}	Synchronous Preset Recovery Time		35		25		ns
t_{WL}	Width of Clock	LOW	17		13		ns
t_{WH}		HIGH	17		13		ns
f_{MAX}	Maximum frequency (Note 4)	External Feedback $1/(t_S + t_{CO})$	20		33.3		MHz
		Internal Feedback $1/(t_S + t_{CF})$	23		35		MHz
		No Feedback $1/(t_{WL} + t_{WH})$	29		38		MHz
t_{EA}	Input to Output Enable (Note 5)			35		25	ns
t_{ER}	Input to Output Disable (Note 5)			35		25	ns

Notes:
1. Commercial Test Conditions: $R_1 = 300\ \Omega$, $R_2 = 390\ \Omega$ (see Switching Test Circuit).
2. t_{PD} is tested with switch S_1 closed and $C_L = 50$ pF (including jig capacitance). $V_{IH} = 3$ V, $V_{IL} = 0$ V, $V_T = 1.5$ V.
3. Calculated from measured f_{MAX} internal.
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
5. For three-state outputs, output enable times are tested with $C_L = 50$ pF to the 1.5 V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. Output disable times are tested with $C_L = 5$ pF. HIGH to high-impedance tests are made to an output voltage of $V_{OH} - 0.5$ V with S_1 open; LOW to high-impedance tests are made to the $V_{OL} + 0.5$ V level with S_1 closed.

ABSOLUTE MAXIMUM RATINGS

Storage temperature ..... -65°C to +150°C
Supply voltage to ground potential
(Pin 24 to Pin 12) Continuous ..... -0.5 V to +7 V
DC voltage applied to outputs
(except during programming) ..... -0.5 V to +7 V
DC input voltage ..... -3 V to +7 V
DC output current into outputs ..... 16 mA
Ambient temperature with power applied ..... -55°C to +125°C
UV light exposure ..... 7258 W-sec/cm²
Static discharge voltage ..... >2001 V
Latchup current (T_A = 0°C to +75°C) ..... >100 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Military (M) devices*
Temperature (T_C) ..... –55°C Min.
Temperature (T_C) ..... +125°C Max.
Supply Voltage (V_{CC}) ..... +4.50 V to +5.50 V

*Military products 100% tested at T_C = +25°C, +125°C, and –55°C.

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS Over military operating range unless otherwise specified (Note 4).

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = –2 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12 mA		0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Current (Note 3)	V_{CC} = Max., V_{IN} = 2.4 V			10	µA
I_{IL}	Input LOW Current (Note 3)	V_{CC} = Max., V_{IN} = 0.40 V			-10	µA
I_I	Input HIGH Current	V_{CC} = Max., V_{IN} = 5.5 V			10	µA
I_{OS}	Output Short-Circuit Current	V_{CC} = Max., V_{OUT} = 0.5 V (Note 2)		-30	-90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., V_I = GND, Outputs Open (Note 5)			100	mA
I_{OZH}	Output Leakage Current (Note 3)	V_{CC} = Max., V_{IN} = V_{IL} or V_{IH}	V_O = 2.4 V		40	µA
I_{OZL}			V_O = 0.4 V		-40	

Notes:
1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. No more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.
3. I/O pin leakage is the worst case of I_{OZX} or I_{IX} (where X = H or L).
4. For APL Products, Group A, Subgroups 1, 2, 3, 7, 8, 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
5. Refer to Military Applications section of PAL Device Handbook for measurement technique.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V at f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V at f = 1 MHz	8	

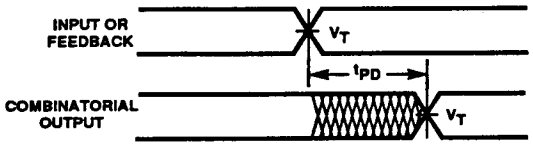
Notes: 1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS Over commercial operating range unless otherwise specified (Notes 1, 6).

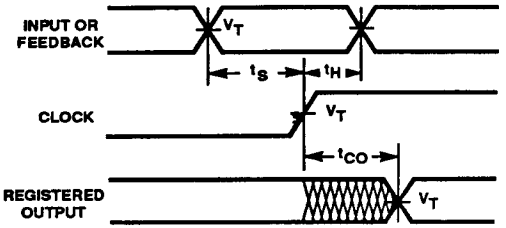
Parameter Symbol	Parameter Description		-40		-30		-25		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input or Feedback to Non-Registered Output (Note 2)	Active LOW		40		30		25	ns
		Active HIGH							
t_S	Setup Time from Input, Feedback or SP to Clock		25		20		20		ns
t_H	Hold Time		0		0		0		ns
t_{CO}	Clock to Output			25		20		20	ns
t_{CF}	Clock to Feedback (Note 3)			20		18		15	ns
t_{AR}	Asynchronous Reset to Registered Output			40		30		25	ns
t_{ARW}	Asynchronous Reset Width		40		30		25		ns
t_{ARR}	Asynchronous Reset Recovery Time			40		30		25	ns
t_{SPR}	Synchronous Preset Recovery Time		40		35		30		ns
t_{WL}	Width of Clock	LOW	20		15		15		ns
t_{WH}		HIGH	20		15		15		ns
f_{MAX}	Maximum frequency (Note 4)	External Feedback $1/(t_S + t_{CO})$	20		25		25		MHz
		Internal Feedback $1/(t_S + t_{CF})$	22.2		26.3		28.6		
		No Feedback $1/(t_{WL} + t_{WH})$	25		33.3		33.3		
t_{EA}	Input to Output Enable (Note 5)			40		30		25	ns
t_{ER}	Input to Output Disable (Note 5)			40		30		25	ns

Notes:
1. Military Test Conditions: $R_1 = 338\ \Omega$, $R_2 = 248\ \Omega$ (see Switching Test Circuit).
2. t_{PD} is tested with switch S_1 closed and $C_L = 50$ pF (including jig capacitance). $V_{IH} = 3$ V, $V_{IL} = 0$ V, $V_T = 1.5$ V.
3. Calculated from measured f_{MAX} internal.
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
5. For three-state outputs, output enable times are tested with $C_L = 50$ pF to the 1.5 V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. Output disable times are tested with $C_L = 5$ pF. HIGH to high-impedance tests are made to an output voltage of V_{OH} - 0.5 V with S_1 open; LOW to high-impedance tests are made to the V_{OL} + 0.5 V level with S_1 closed.
6. Included in Group A are Subgroups 1, 2, 3, 7, 8, 9, 10, and 11 tests per MIL-STD-883, Method 5005 unless otherwise noted.

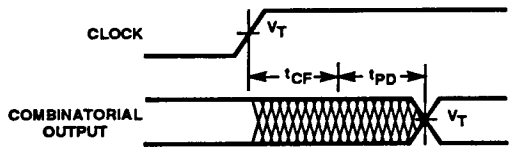
SWITCHING WAVEFORMS



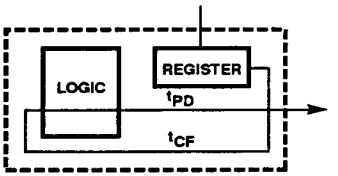
Combinatorial Output

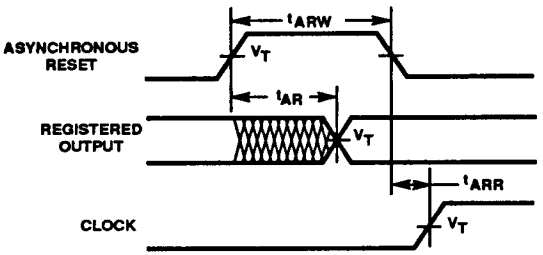


Registered Output

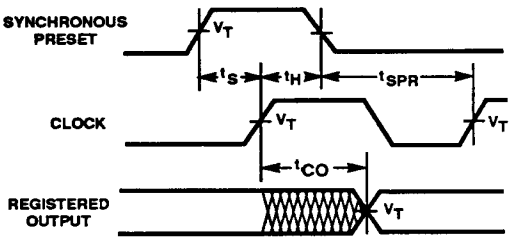


Clock to Feedback to Combinatorial Output(See Path at Right)

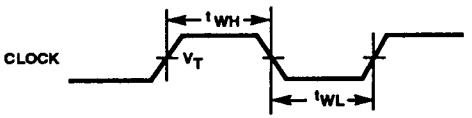




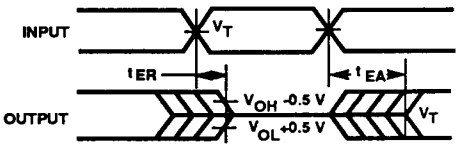
Asynchronous Reset



Synchronous Preset



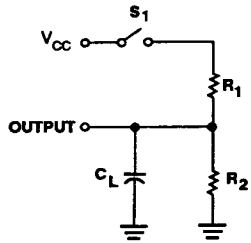
Clock Width



Input to Output Disable/Enable

Notes:
1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V
3. Input rise and fall times 2 - 5 ns typical

SWITCHING TEST CIRCUIT

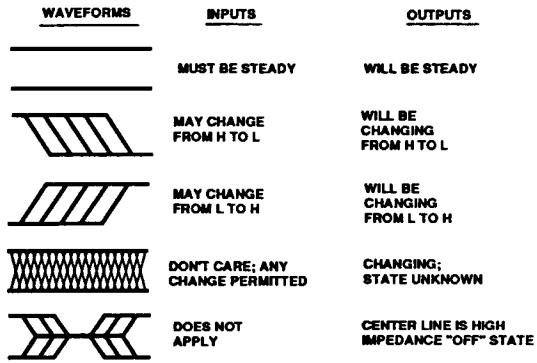


Commercial Specification	Switch S_1	C_L	C Device		Measured Output Value
			R_1	R_2	
t_{PD}, t_{CO}, t_{CF}	Closed	50 pF	300 Ω	390 Ω	1.5 V
t_{EA}	Z->H: open Z->L: closed	50 pF	300 Ω	390 Ω	1.5 V
t_{ER}	H->Z: open L->Z: closed	5 pF	300 Ω	390 Ω	H->Z: V_{OH} -0.5 V L->Z: V_{OL} +0.5 V

Military Specification	Switch S_1	C_L	M Device		Measured Output Value
			R_1	R_2	
t_{PD}, t_{CO}, t_{CF}	Closed	50 pF	338 Ω	248 Ω	1.5 V
t_{EA}	Z->H: open Z->L: closed	50 pF	338 Ω	248 Ω	1.5 V
t_{ER}	H->Z: open L->Z: closed	5 pF	338 Ω	248 Ω	H->Z: V_{OH} -0.5 V L->Z: V_{OL} +0.5 V

SWITCHING WAVEFORMS

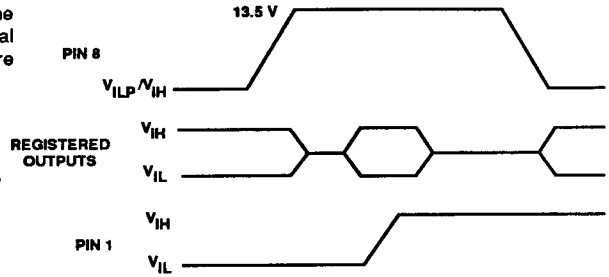
KEY TO SWITCHING WAVEFORMS



OUTPUT REGISTER PRELOAD

The preload function allows the register to be loaded from the output pins. This feature aids functional testing of sequential designs by allowing direct loading of output states. The procedure is:

1. Raise V_{CC} to 5.0 V ± 0.5 V.
2. Disable output registers by setting pin 8 (DIP) to 13.5 V ± 0.5 V.
3. Apply V_{IL}/V_{IH} as desired to all registered output pins. Leave combinatorial outputs floating.
4. Clock output registers.
5. Remove V_{IL}/V_{IH} from all registered output pins.
6. Remove high voltage from pin 8.
7. Enable output registers per programmed pattern.
8. Verify for V_{OL}/V_{OH} at all registered output pins, according to programmed polarity.



PROGRAMMING AND ERASING

The PALC22V10 can be programmed on standard logic programmers. Programmers approved by Advanced Micro Devices are listed on Page 15. The PALC22V10 may be erased by ultraviolet light when contained in the windowed package.

For erasure, the recommended ultraviolet light wavelength is 2537 Angstroms. The minimum dose required is 72000 mW-sec/cm² (UV intensity x exposure time). For an ultraviolet lamp with a 20 mW/cm² power rating, the minimum exposure time would be 72000/20 seconds, or 60 minutes. The device needs to be within one inch of the lamp during erasure.

Permanent damage may result if the device is exposed to high intensity UV light for an extended period of time. The recommended maximum dosage is 7258 W-sec/cm².

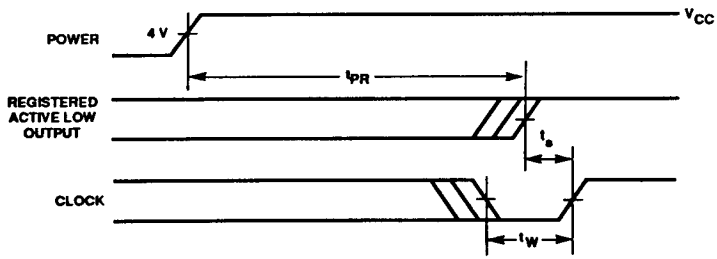
Wavelengths of light less than 4000 Angstroms can partially erase the device in the windowed package. For this reason, an opaque label should be placed over the window, especially if the device will be exposed to sunlight or fluorescent lighting for extended periods of time.

POWER-UP RESET

The registered devices in the AMD PAL Family have been designed with the capability to reset during system power-up. Following power-up, all registers will be reset to LOW. The output state will depend on the polarity of the output buffer. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the asynchronous operation of the power-up reset, and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Min.	Typ.	Max.	Unit
t_{PR}	Power-Up Reset Time		600	1000	ns
t_s	Input or Feedback Setup Time	See Switching Characteristics table			
t_w	Clock Width				



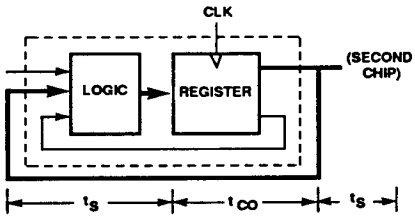
f_{MAX} PARAMETERS

The parameter f_{MAX} is the maximum clock rate at which the device is guaranteed to operate. Because flexibility inherent in programmable logic devices offers a choice of clocked flip-flop designs, f_{MAX} is specified for two types of synchronous designs.

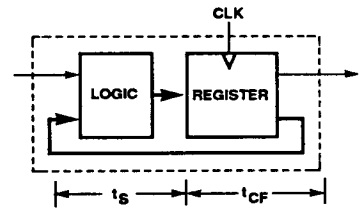
The first type of design is a state machine with feedback signals sent off-chip. This external feedback could go back to the device inputs, or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input setup time for the external signals ($t_s + t_{CO}$). The reciprocal, f_{MAX}, is the maximum frequency with external feedback or in conjunction with an equivalent speed device. This f_{MAX} is designated "f_{MAX} external."

The second type of design is a single-chip state machine with internal feedback only. In this case, flip-flop inputs are defined by the device inputs and flip-flop outputs. Under these conditions, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic to the flip-flop inputs ($t_s + t_{CF}$). This f_{MAX} is designated "f_{MAX} internal."

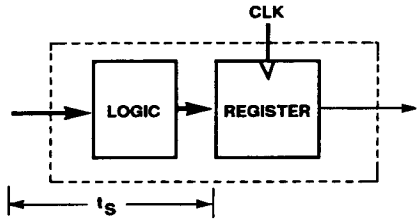
The third type of design is a simple data path application. In this case, input data is presented to the flip-flop and clocked through; no feedback is employed. Under these conditions, the period is limited by the sum of the data setup time and the data hold time ($t_s + t_H$). However, a lower limit for the period of each f_{MAX} type is the minimum clock period ($t_{WH} + t_{WL}$). Usually, this minimum clock period determines the period for the third f_{MAX}, designated "f_{MAX} no feedback."



f_{MAX} External Feedback; $1/(t_s + t_{CO})$



f_{MAX} Internal Feedback; $1/(t_s + t_{CF})$



f_{MAX} No Feedback; $1/(t_s + t_H)$ or $1/(t_{WH} + t_{WL})$

Programmers/Development Systems (Subject to change)

MANUFACTURER	PROGRAMMER CONFIGURATION
Adams MacDonald 800 Airport Road Monterey, CA 93940 (408) 373-3607	Contact progammer manufacturer
Data I/O Corporation 10525 Willows Road NE PO Box 97046 Redmond, WA 98073-9746 (800) 247-5700	System 29A, 29B LogicPak™ 303A-V04 Adapter 303A-011A-V04 Adapter 303A-011B-V03 Model 60, rev. V10 UniSite™ 40, rev. 2.3 Family/Pinout Code DB-28
Digelec Inc. 22736 Vanowen Canoga Park, CA 91307 (800) 227-8834 or (415) 965-7020	System 860, rev. A-1.2
Kontron Electronics Inc. 1230 Charleston Road Mountain View, CA 94039-7230 (415) 965-7020	System EPP-80 Module UPM-B or UPM-C, rev. 2.0
Logical Devices 1201 E. Northwest 65th Place Fort Lauderdale, FL 33309 (800) 331-7766 or (305) 974-0967	Contact programmer manufacturer
Micropross Parc d'Activite des Pres 5, rue Denis-Papin 59650 Villeneuve-d'Ascq (20) 47.90.40	ROM 5000, rev. 4.6
Stag Microsystems Inc. 1600 Wyatt Drive, Suite 3 Santa Clara, CA 95054 (408) 988-1118	ZL30/A, rev. 30A26 PPZ, rev. 33 Code 24-70
Varix Corporation 1210 E. Campbell Road, Suite 100 Richardson, TX 75081 (214) 437-0777	Omni Programmer, rev. 5.00A
MANUFACTURER	**SOFTWARE DEVELOPMENT SYSTEM**
Advanced Micro Devices 901 Thompson Place Sunnyvale, CA 94088-3453 (800) 222-9323	PALASM®2 Software, rev. 2.22 and later
Data I/O Corporation 10525 Willows Road NE PO Box 97046 Redmond, WA 98073-9746 (800) 247-5700	ABEL™ Software, rev. 1.0 and later
Logical Devices 1201 E. Northwest 65th Place Fort Lauderdale, FL 33309 (800) 331-7766 or (305) 974-0967	CUPL™ Software, rev. 1.0 and later

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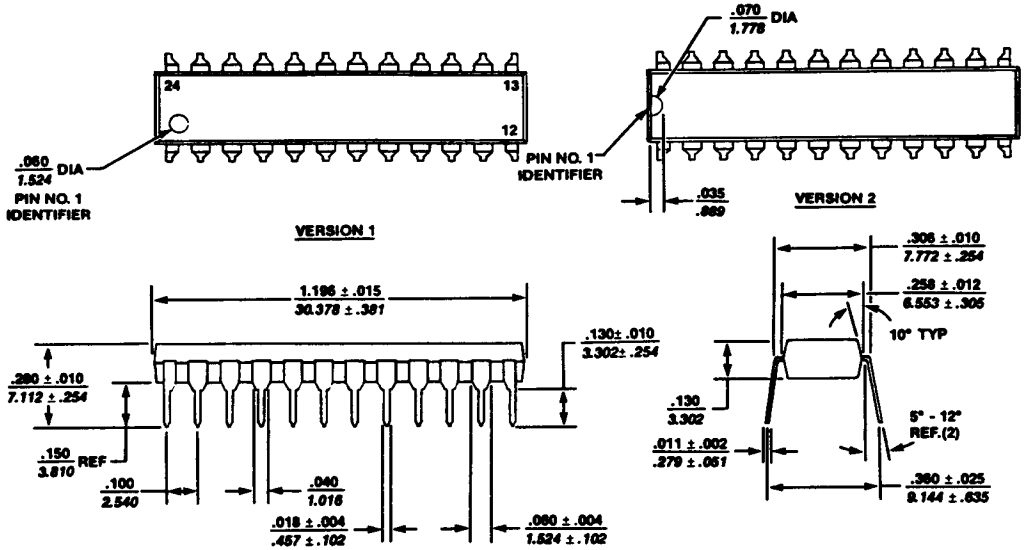
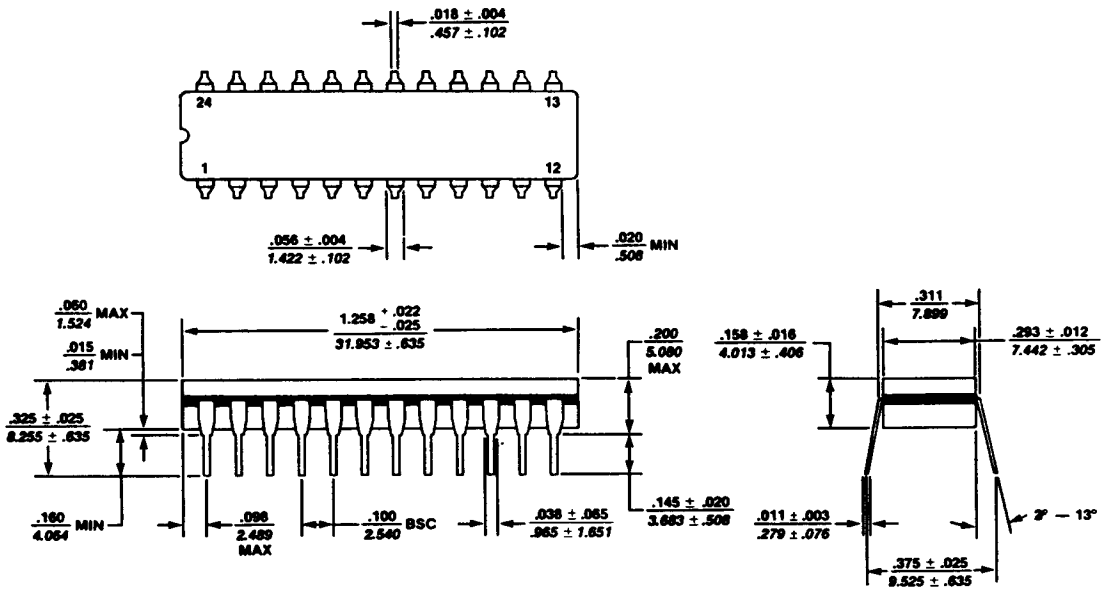
PACKAGE DRAWINGS

24NS Molded SKINNYDIP



PID# 10747A

24JS Ceramic SKINNYDIP



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

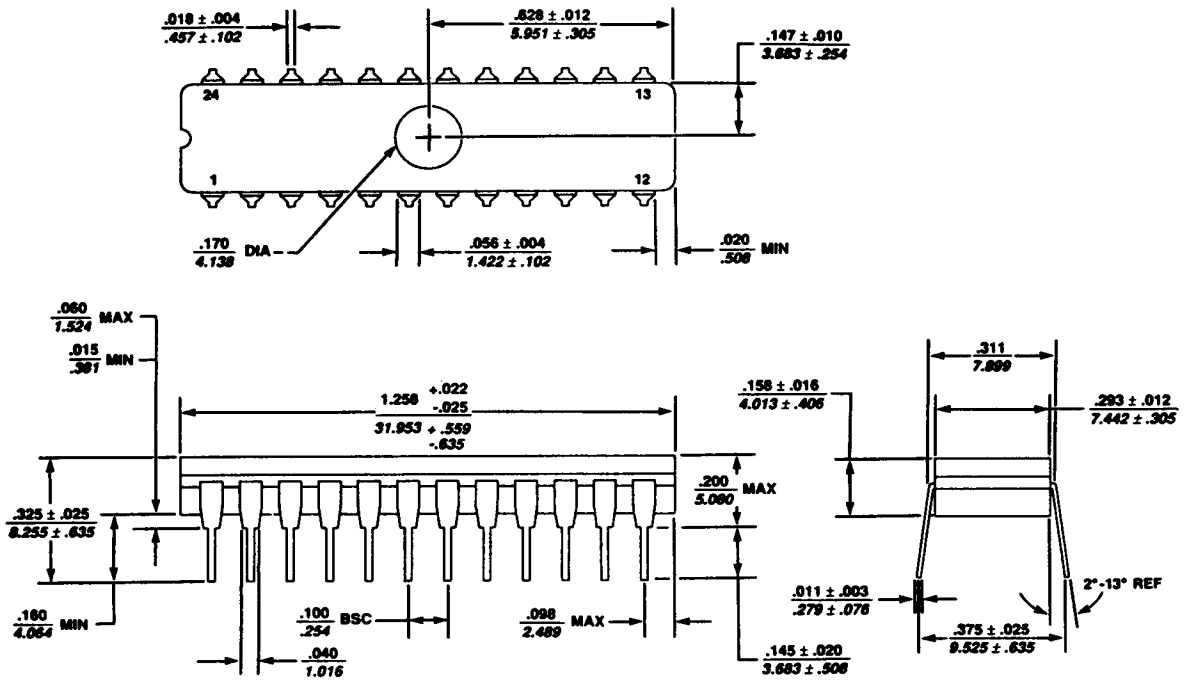
PID# 10752A

*For reference only.

Note: Package dimensions shown here are for Commercial parts. For Military, refer to MIL-M-38510, Appendix C.

PACKAGE DRAWINGS

24QS Window CERDIP
(5/16" x 1 1/4")



UNLESS OTHERWISE SPECIFIED:
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ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

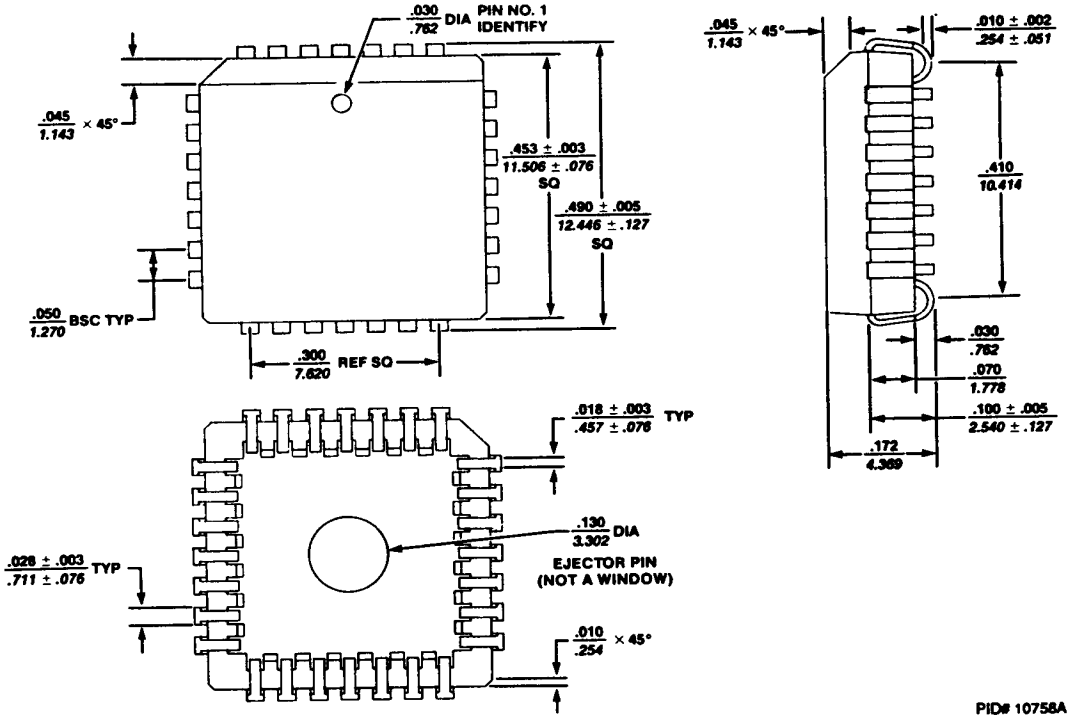
PID# 10755A

Note: Package dimensions shown here are for Commercial parts. For Military, refer to MIL-M-38510, Appendix C.

PACKAGE DRAWING

28NL/FN Molded Chip Carrier

(.451" x .451")



PID# 10758A

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