PEEL™22CV10A

CMOS Programmable Electrically Erasable Logic Device

T-46-13-27

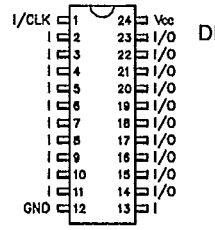
Features

- **Advanced CMOS EEPROM Technology**
- **Ultra High Performance**
  - 10ns, 12ns and 15ns (t_{PD}) versions
  - fmax as fast as 83.3MHz
- **Low Power Consumption**
  - 110mA + 0.5mA/MHz max
- **EE Reprogrammability**
  - Low-risk reprogrammable inventory
  - Superior programming and functional yield
  - Erases and programs in seconds
- **Development and Programming Support**
  - Third-party software and programmers
  - ICT PEEL Development System and software.
- **Architectural Flexibility**
  - 132 product term x 44 input AND array
  - Up to 22 inputs and 10 outputs
  - Variable product term distribution (8 to 16 per output) for greater logic flexibility
  - Independently programmable 4 or 12-configuration I/O macrocells
  - Synchronous preset, asynchronous clear
  - Independently programmable output enables
- **Application Versatility**
  - Replaces random SSI/MSI logic
  - Pin and JEDEC-file compatible with the bipolar AmPAL22V10 and CMOS PALC22V10

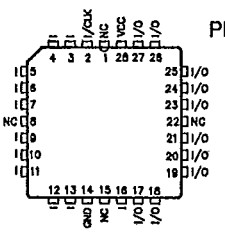
General Description

The ICT PEEL22CV10A-10, PEEL22CV10A-12 and PEEL22CV10A-15 are CMOS Programmable Electrically Erasable Logic Devices that provides a high-performance, low-power, reprogrammable, and architecturally enhanced alternative to early generation programmable logic devices (PLDs). Designed in advanced CMOS EEPROM technology, the PEEL22CV10A rivals speed parameters of comparable bipolar PLDs while providing a dramatic improvement in active power consumption. The EE reprogrammability of the PEEL22CV10A allows cost effective plastic packaging, low risk inventory, reduced development and retrofit costs, and enhanced testability to ensure 100% field programmability and function. The PEEL22CV10A's flexible architecture offers complete function and JEDEC-file compatibility with the bipolar AmPAL22V10 and the CMOS PALC22V10. Applications for the PEEL22CV10A include: replacement of random SSI/MSI logic circuitry and user customized sequential and combinatorial functions such as counters, shift registers, state machines, address decoders, multiplexers, etc. Development and programming support for the PEEL22CV10A is provided by ICT and third-party manufacturers.

Pin Configuration (Figure 1)

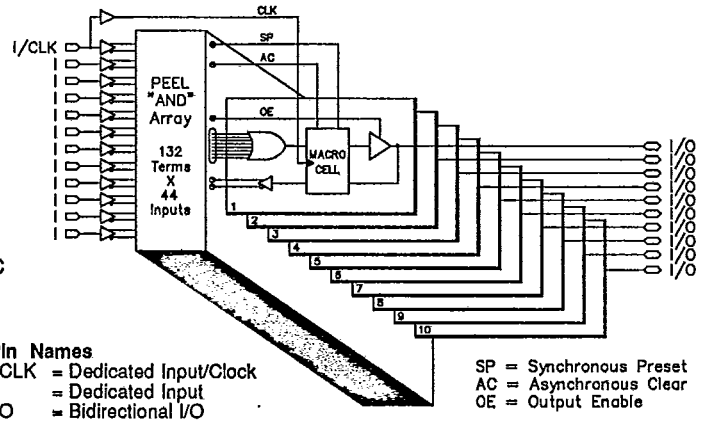


DIP



PLCC

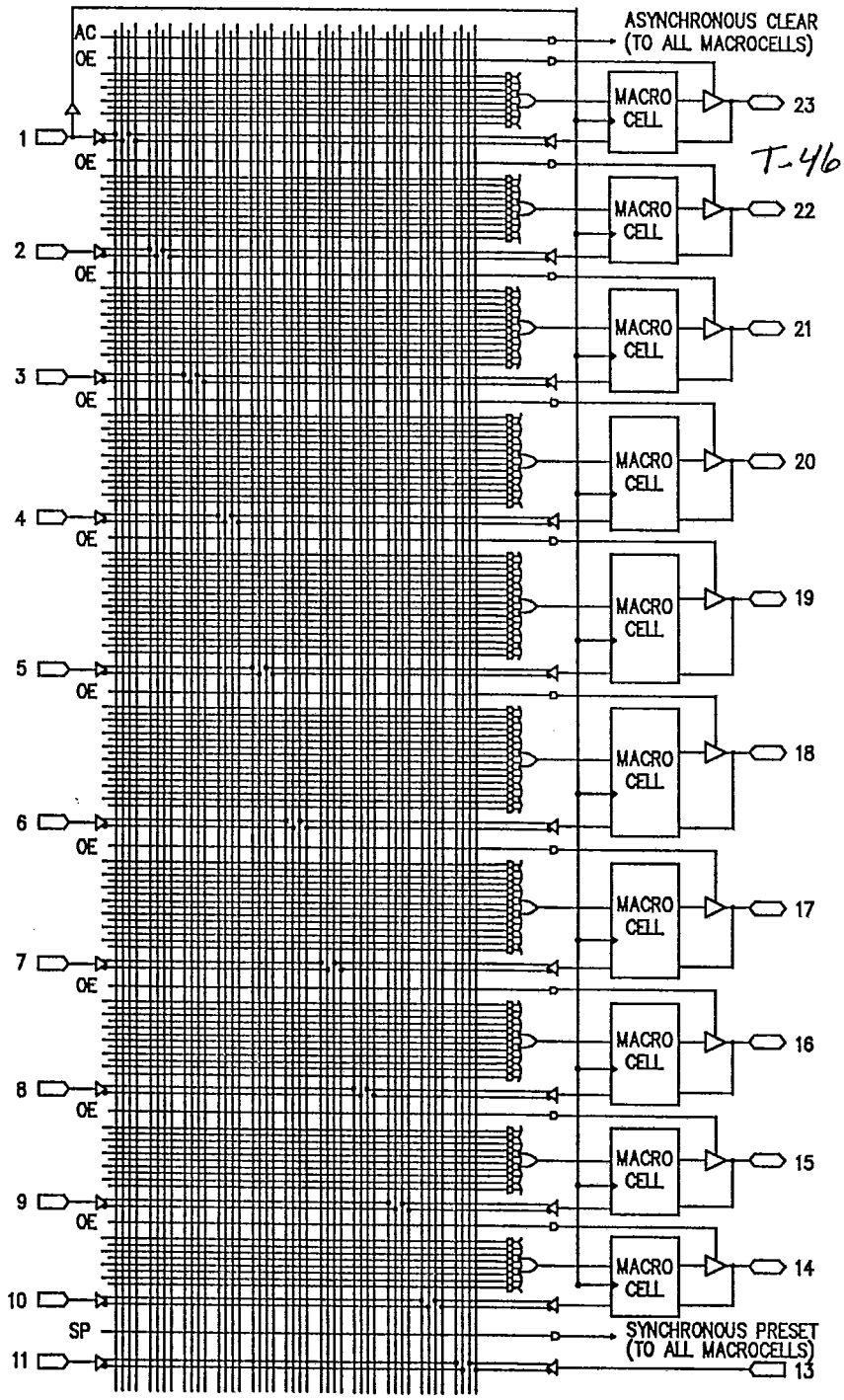
Block Diagram (Figure 2)



Pin Names

I/CLK	= Dedicated Input/Clock
I	= Dedicated Input
I/O	= Bidirectional I/O
GND	= Ground
Vcc	= Power Supply

SP = Synchronous Preset
AC = Asynchronous Clear
OE = Output Enable



T-46-13-27

Figure 3. PEEL22CV10A Logic Array Diagram

T-46-13-27

Function Description
The PEEL22CV10A implements logic functions as sum-of-products expressions in a programmable-AND/fixed-OR logic array. User-defined functions are created by programming the connections of input signals into the array. User-configurable output structures in the form of I/O macrocells further increase logic flexibility.

Architecture Overview
The PEEL22CV10A architecture is illustrated in the block diagram of figure 2. Twelve dedicated inputs and 10 I/Os provide up to 22 inputs and 10 outputs for creation of logic functions. At the core of the device is a programmable electrically-erasable AND array which drives a fixed OR array. With this structure, the PEEL22CV10A can implement up to 10 sum-of-products logic expressions.

Associated with each of the 10 OR functions is an I/O macrocell which can be independently programmed to one of 4 different configurations. The programmable macrocells allow each I/O to create sequential or combinatorial logic functions with either active-high or active-low polarity.

AND/OR Logic Array
The programmable AND array of the PEEL22CV10A (shown in figure 3) is formed by input lines intersecting product terms. The input lines and product terms are used as follows:

44 Input Lines:

- 24 input lines carry the true and complement of the signals applied to the 12 input pins
- 20 additional lines carry the true and complement values of feedback or input signals from the 10 I/Os

132 product terms:

- 120 product terms (arranged in 2 groups of 8, 10, 12,14, and 16) used to form logical sums
- 10 output enable terms (one for each I/O)
- 1 global synchronous present term
- 1 global asynchronous clear term

At each input-line/product-term intersection there is an EEPROM memory cell which determines whether or not there is a logical connection at that intersection. Each product term is essentially a 44-input

AND gate. A product term which is connected to both the true and compliment of an input signal will always be FALSE, and thus will not effect the OR function that it drives. When all the connections on a product term are opened, a don't care state exists and that term will always be TRUE.

When programming the PEEL22CV10A, the device programmer first performs a bulk erase to instantly remove the previous pattern. The erase cycle opens every logical connection in the array. The device is then configured to perform the user-defined function by programming selected connections in the AND array. (Note that PEEL device programmers automatically program the connections on unused product terms so that they will have no effect on the output function)

Variable Product Term Distribution
The PEEL22CV10A provides 120 product terms to drive the 10 OR functions. These product terms are distributed among the outputs in groups of 8, 10, 12, 14, and 16 to form logical sums (see figure 3). This distribution allows optimum use of device resources.

Programmable I/O Macrocell
The output macrocell provides complete control over the architecture of each output. The ability to configure each output independently permits users to tailor the configuration of the PEEL22CV10A to the precise requirements of their designs.

Macrocell Architecture
Each I/O macrocell, as shown in figure 4, consists of a D-type flip-flop and two signal-select multiplexers. The configuration of each macrocell of the PEEL22CV10A is determined by the two EEPROM bits controlling these multiplexers shown in table 1. Four EEPROM bits are used to determine the twelve-configuration macrocells of the PEEL22CV10+ found in table 2. These bits determine output polarity, feedback paths, and output type (registered or non-registered). Equivalent circuits for the macrocell configurations are illustrated in figures 5 and 6.

Output Type
The signal from the OR array can be fed directly to the output pin (combinatorial function) or latched in the D-type flip-flop (registered function). The D-type flip-flop latches data on the rising edge of the clock and is controlled by the global preset and clear terms. When the synchronous preset term is satisfied, the Q output of the register will be set HIGH at the next rising edge of the clock input. Satisfying the asynchronous clear term will set Q LOW, regardless of the clock state. If both terms are satisfied simultaneously, the clear will override the preset.

Output Polarity
Each macrocell can be configured to implement active-high or active-low logic. Programmable polarity eliminates the need for external inverters.

T-46-13-27

Output Enable

The output of each I/O macrocell can be enabled or disabled under the control of its associated programmable output enable product term. When the logical conditions programmed on the output enable term are satisfied, the output signal is propagated to the I/O pin. Otherwise, the output buffer is driven into the high-impedance state.

Under the control of the output enable term, the I/O pin can function as a dedicated input, a dedicated output, or a bi-directional I/O. Opening every connection on the output enable term will permanently enable the output buffer and yield a dedicated output. Conversely, if every connection is intact, the enable term will always be logically false and the I/O will function as a dedicated input.

Input/Feedback Select

When configuring an I/O macrocell to implement a registered function (configurations 1 and 2 in Figure 5), the $\overline{Q}$ output of the flip-flop drives the feedback term. When configuring and I/O mcrocell to implement a combinatorial function (configurations 3 and 4 in Figure 5), the feedback signal is taken from the I/O pin. In this case, the pin can be used as a dedicated input or a bi-directionl I/O. (Refer also to Table 1)

Bi-directional /O

The input/feedback signal is taken from the I/O pin when using the pin as a dedicated input or as a bi-directional I/O. (Note that it is possible to create a registered output function with bi-directional I/O.)

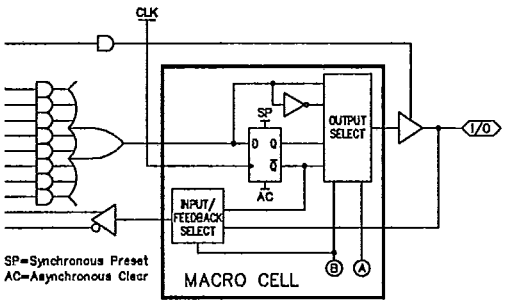


Figure 4. 22CV10A Macro Cell Block Diagram

Combinatorial Feedback

The signal-select multiplexer gives the macrocell the ability to feedback the output directly from the OR gate, regardless of whether the output function is registered or combinatorial. This feature allows the creation of asynchronous latches, even when the output must be disabled. (Refer to configurations 5, 6, 7, and 8 in figure 6.)

Registered Feedback

Feedback also can be taken from the register, regardless of whether the output function is to be combinatorial or registered. When implementing configurations 11 and 12 in figure 6, the register can be used for internal latching of data while leaving the external output free for combinatorial functions.

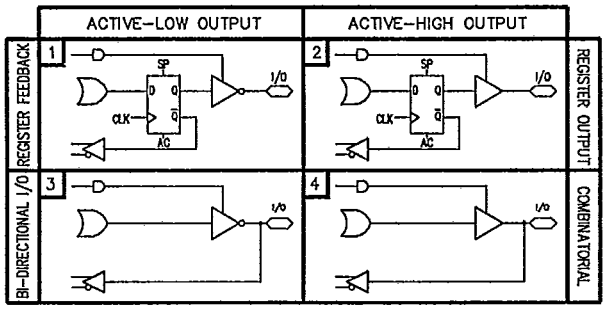


Figure 5. Equivalent Circuits for the Four Configurations of the PEEL22CV10A I/0 Macrocell.

Configuration #	A	B	Input/Feedback Select	Output Select	
1	0	0	Register Feedback	Register	Active Low
2	1	0			Active High
3	0	1	Bi-Directional I/O	Combinatorial	Active Low
4	1	1			Active High

Table 1. PEEL22CV10A Macrocell Configuration Bits

Additional Macro Cell Configurations

Besides the standard four-configuration macro cells, each PEEL22CV10A provides an additional eight configurations (twelve total) that can be used to increase design flexibility (see figure 6). These configurations are the same provided by other PEEL devices, the 18CV8, 20CG10, and 22CV10Z. For logic assembly of all twelve configurations, specify PEEL22CV10A+ or PEEL22CV10Z (with Z-bit set to 1), and for programming select PEEL22CV10A+.

Design Security

The PEEL22CV10A provides a special EEPROM security bit that prevents unauthorized reading or copying of designs programmed into the device. The security bit is set by the PLD programmer, either at the conclusion of the programming cycle or as a separate step, after the device has been programmed. Once the security bit is set it is impossible to verify (read) or program the PEEL until the entire device has first been erased with the bulk-erase function.

Signature Word

The signature word feature allows a 24-bit code to be programmed into the PEEL22CV10A. The code can be read back even after the security bit has been set. The signature word can be used to identify the pattern programmed into the device or to record the design revision, etc.

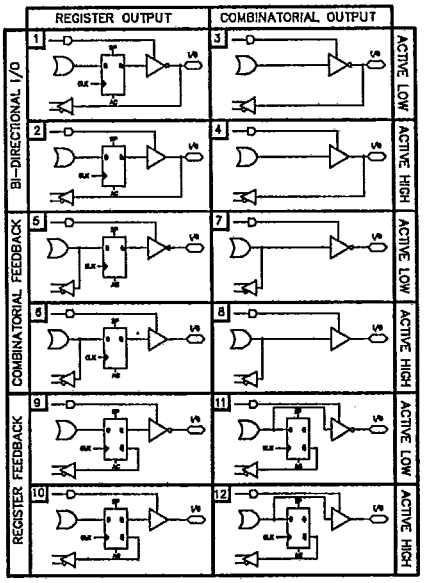


Figure 6. Equivalent Circuits for the Twelve Configurations of the PEEL22CV10A+ I/0 Macrocell.

Configuration #	A	B	C	D	Input/Feedback Select	Output Select	
1	0	0	1	0	Bi-Directional I/O	Register	Active Low
2	1	0	1	0	"	"	Active High
3	0	1	0	0	"	Combinatorial	Active Low
4	1	1	0	0	"	"	Active High
5	0	0	1	1	Combinatorial Feedback	Register	Active Low
6	1	0	1	1	"	"	Active High
7	0	1	1	1	"	Combinatorial	Active Low
8	1	1	1	1	"	"	Active High
9	0	0	0	0	Register Feedback	Regisiter	Active Low
10	1	0	0	0	"	"	Active High
11	0	1	1	0	"	Combinatorial	Active Low
12	1	1	1	0	"	"	Active High

Table 2. PEEL22CV10A+ Macrocell Configuration Bits

INTERNATIONAL CMOS TECHNOLOGY, INC.

PEEL™22CV10A

Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	− 0.5 to + 7.0	V
V_I, V_O	Voltage Applied to Any Pin [3]	Relative to GND [1]	− 0.5 to V_{CC} + 0.6	V
I_O	Output Current *	Per pin (I_{OL}, I_{OH})	± 25	mA
T_{ST}	Storage Temperature		− 65 to + 125	°C
T_{LT}	Lead Temperature	Soldering 10 seconds	+ 300	°C

Operating Ranges

T-46-13-27

Symbol	Alternate Source Symbol*	Parameter	Conditions	Min	Max	Unit
V_{CC}	V_{CC}	Supply Voltage	Commercial [2]	4.75	5.25	V
T_A	T_A	Ambient Temperature	Commercial [2]	0	70	°C
T_R		Clock Rise Time	See note 4		250	nS
T_F		Clock Fall Time	See note 4		250	nS
T_{RVCC}		VCC Rise Time	See note 4		250	mS

D.C. Electrical Characteristics

Over the operating range

Symbol	Alternate Source Symbol*	Parameter	Conditions	Min	Max	Unit
V_{OH}	V_{OH}	Output HIGH Voltage - TTL	V_{CC} = Min, I_{OH} = −4.0mA	2.4		V
V_{OHC}		Output HIGH Voltage-CMOS	V_{CC} = Min, I_{OH} = −10µA	V_{CC} − 0.1		V
V_{OL}	V_{OL}	Output LOW Voltage - TTL	V_{CC} = Min, I_{OL} = 12mA		0.5	V
V_{OLC}		Output LOW Voltage-CMOS	V_{CC} = Min, I_{OL} = 10µA		0.1	V
V_{IH}	V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.3	V
V_{IL}	V_{IL}	Input LOW Level		− 0.3	0.8	V
I_{IX}	I_{IL}, I_{IH}, I_{IX}	Input Leakage Current	V_{CC} = Max, GND ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{OZ}	I_{OZ}	Output Leakage Current	I/O = High-Z, GND ≤ V_O ≤ V_{CC}		±10	µA
I_{SC}	I_{SC}	Output Short Circuit Current	V_{CC} = Max, V_O = 0.5V [10]	− 30	− 120	mA
I_{CCAC}	I_{CC}	Vcc Active Current CMOS	V_{IN} = Vcc or GND [5,11]		110 + 0.5mA/MHz	mA
I_{CCAT}	I_{CC}	Vcc Active Current, TTL	V_{IN} = V_{IL} or V_{IH} [5,11]		120 + 0.5mA/MHz	mA
C_{IN} [8]	C_{IN}	Input Capacitance	T_A = 25°C, V_{CC} = 5.0V @ f = 1MHz		6	pF
C_{OUT} [8]	C_{OUT}	Output Capacitance			12	pF

* Alternate source symbols are shown to compare the specifications of the PEEL22CV10A to other pin-compatible devices.

INTERNATIONAL CMOS TECHNOLOGY, INC.

PEEL™22CV10A

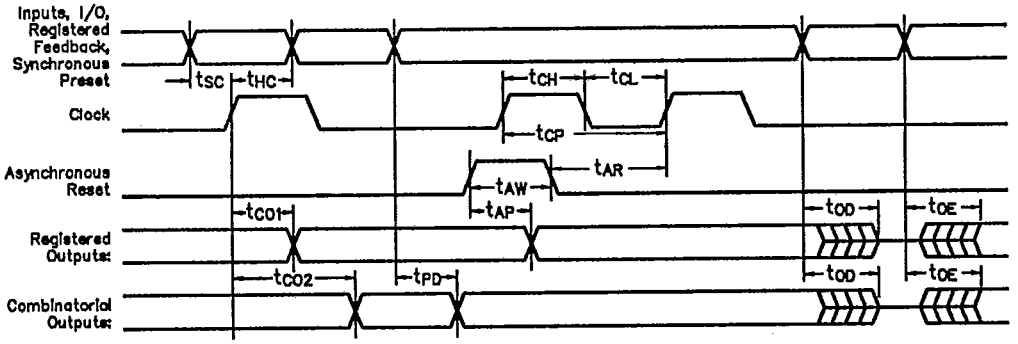
T-46-13-27

A.C. Electrical Characteristics Over the Operating Range [9,12]

Symbol	Alternate Source Symbol*	Parameter	22CV10A-10		22CV10A-12		22CV10A-15		Unit
			Min	Max	Min	Max	Min	Max	
t_{PD}	t_{PD}	Input[6] to non-registered output		10		12		15	ns
t_{OE}	t_{EA}	Input [6] to output enable [7]		10		12		15	ns
t_{OD}	t_{ER}	Input [6] to output disable [7]		10		12		15	ns
t_{CO1}	t_{CO}	Clock to output		8		9		10	ns
t_{CO2}		Clock to combinatorial output delay via internal registered feedback		14		16		19	ns
t_{SC}	t_S	Input [6] or feedback setup to clock	7		8		10		ns
t_{HC}	t_H	Input [6] hold after clock	0		0		0		ns
t_{CL},t_{CH}	t_W	Clock width - clock low time, clock high time [4]	6		7		8		ns
t_{CP}	t_P	Min clock period Extenal (t_{SC} + t_{CO1})	15		17		20		ns
f_{max1}		Max clock freq. Internal Feedback[13]	76.9		66.7		52.6		MHz
f_{max2}	f_{max}	Max clock freq. External ($1/t_{CP}$)[13]	66.6		58.8		50.0		MHz
f_{max3}		Max clock freq. No Feedback ($1/t_{CL}+t_{CH}$)[13]	83.3		71.4		62.5		MHz
t_{AW}	t_{AW}	Asynchronous Reset pulse width	10		12		15		ns
t_{AP}	t_{AP}	Input [6] to Asynchronous Reset		12		15		18	ns
t_{AR}	t_{AR}	Asynchronous Reset recovery time		12		15		18	ns
t_{RESET}		Power-on reset time for registers in clear state [4]		5		5		5	µs

* Alternate source symbols are shown to compare the PEEL22CV10A specifications to other pin-compatible devices.

Switching Waveforms



1. Minimum DC input is – 0.5V, however inputs may undershoot to – 2.0V for periods less than 20nS.
2. Voltage applied to input or output must not exceed V_{CC} +1.0V.
3. V_I and V_O are not specified for program/verify operation.
4. Test points for Clock and V_{CC} in t_R, t_F, t_{CL}, t_{CH}, and t_{RESET} are referenced at 10% and 90% levels.
5. I/O pins open (no load).
6. "Input" refers to an Input pin signal.
7. t_{OE} is measured from input transition to $V_{REF} \pm 0.1V$, t_{OD} is measured from input transition to $V_{OH} - 0.1V$ or $V_{OL} + 0.1V$; $V_{REF} = V_L$ see test loads at the end of this section.
8. Capacitances are tested on a sample basis.
9. Test conditions assume: signal transition times of 5ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
10. Test one output at a time for a duration of less than 1 sec.
11. ICC for a typical application: This parameter is tested with the device programmed as a 10-bit Counter.
12. PEEL Device test loads are specified at the end of this section.
13. Parameters are not 100% tested. Specifications are based on intial characterization and are tested after any design or process modification which may affect operational frequency.

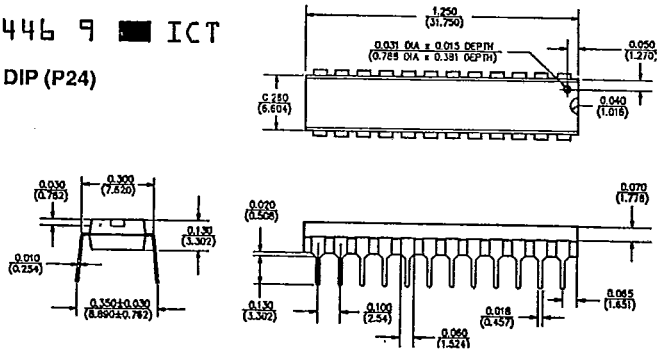
T-46-13-27

Package Outlines

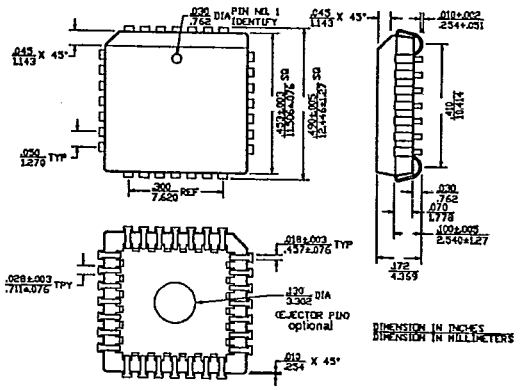
All dimensions in: inches (millimeters)

Dimension tolerences unless otherwise specified are 0.005 (0.127)

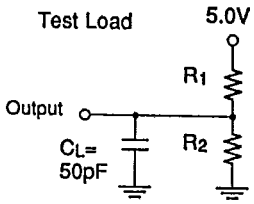
■ 24-Pin Plastic DIP (P24)



■ 28-Pin PLCC (J28)

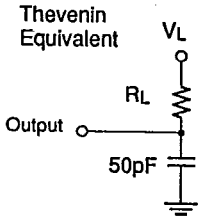


Test Loads (Figure 6)



CMOS Interface
R1=480KΩ
R2=480KΩ

TTL Interface
R1=308Ω
R2=193Ω



CMOS Interface
RL=228KΩ
VL=2.375V

TTL Interface
RL=119Ω
VL=1.93V

Preliminary Designation

The "Preliminary" designation on an ICT data sheet indicates that the product is not fully characterized. The specifications are subject to change, are based on design goals or preliminary part evaluation, and are not guaranteed. ICT or an authorized sales representative should be consulted for current information before using this product

Specifications, Patents, Life Support Policy, Trademarks

ICT reserves the right to make changes in specifications at any time and without notice. The information furnished by ICT in this publication is believed to be accurate and reliable. However, no responsibility is assumed by ICT for its use, nor for any infingements of patents of other rights of third parties resulting from its use. No license is granted under any patents or patent rights of ICT. ICT's products are not authorized for use as critical components in life support devices or systems without the written approval of the president of International CMOS Technology, Inc. Life support devices, or systems, are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness

PEEL™ is a Trademark of International CMOS Technology, Inc.
PAL® is a registered trademark of Monolithic Memories, Inc.

INTERNATIONAL CMOS TECHNOLOGY, INC.
2125 Lundy Avenue
San Jose, California 95131
Telephone (408) 434-0678
TWX (901) 997-1531
FAX (408) 434-0688