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T-46-19-07

# PEEL™ 22CV10-25

## CMOS Programmable Electrically Erasable Logic Device

### Features

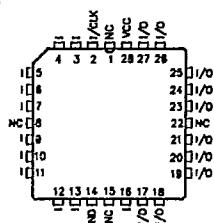
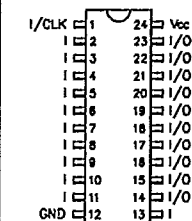
- **Advanced CMOS EEPROM Technology**
- **Low Power Consumption**
  - 67mA at 25MHz
- **High Performance**
  - $t_{PD} = 25ns$ ,
  - $f_{max} = 33.3Mhz$
- **EE Reprogrammability**
  - Low-risk reprogrammable inventory
  - Superior programming and functional yield
  - Erases and programs in seconds
- **Development and Programming Support**
  - Third-party software and programmers
  - ICT PEEL Development System and software.
- **Architectural Flexibility**
  - 132 product term x 44 input AND array
  - Up to 22 inputs and 10 outputs
  - Variable product term distribution (8 to 16 per output) for greater logic flexibility
  - Independently programmable I/O macrocells
  - Synchronous preset, asynchronous clear
  - Independently programmable output enables
- **Application Versatility**
  - Replaces random SSI/MSI logic
  - Pin and JEDEC compatible with the bipolar AmPAL22V10 and CMOS PALC22V10

### General Description

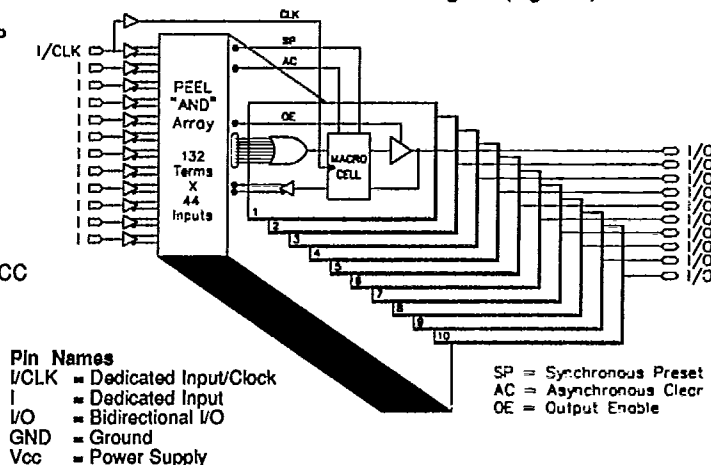
The ICT PEEL22CV10-25 is a CMOS Programmable Electrically Erasable Logic Device that provides a high-performance, low-power, reprogrammable, and architecturally enhanced alternative to early generation programmable logic devices (PLDs). Designed in advanced CMOS EEPROM technology, the PEEL22CV10-25 rivals speed parameters of comparable bipolar PLDs while providing a dramatic improvement in active power consumption. The EE reprogrammability of the PEEL22CV10-25 allows cost effective plastic packaging, low risk inventory, reduced development and retrofit costs, and enhanced testability to en-

sure 100% field programmability and function. The PEEL22CV10-25's flexible architecture offers complete function and JEDEC-file compatibility with the bipolar AmPAL22V10 and the CMOS PALC22V10. Applications for the PEEL22CV10A-25 include: replacement of random SSI/MSI logic circuitry and user customized sequential and combinatorial functions such as counters, shift registers, state machines, address decoders, multiplexers, etc. Development and programming support for the PEEL22CV10-25 is provided by ICT and third-party manufacturers.

Pin Configuration (Figure 1)



Block Diagram (Figure 2)





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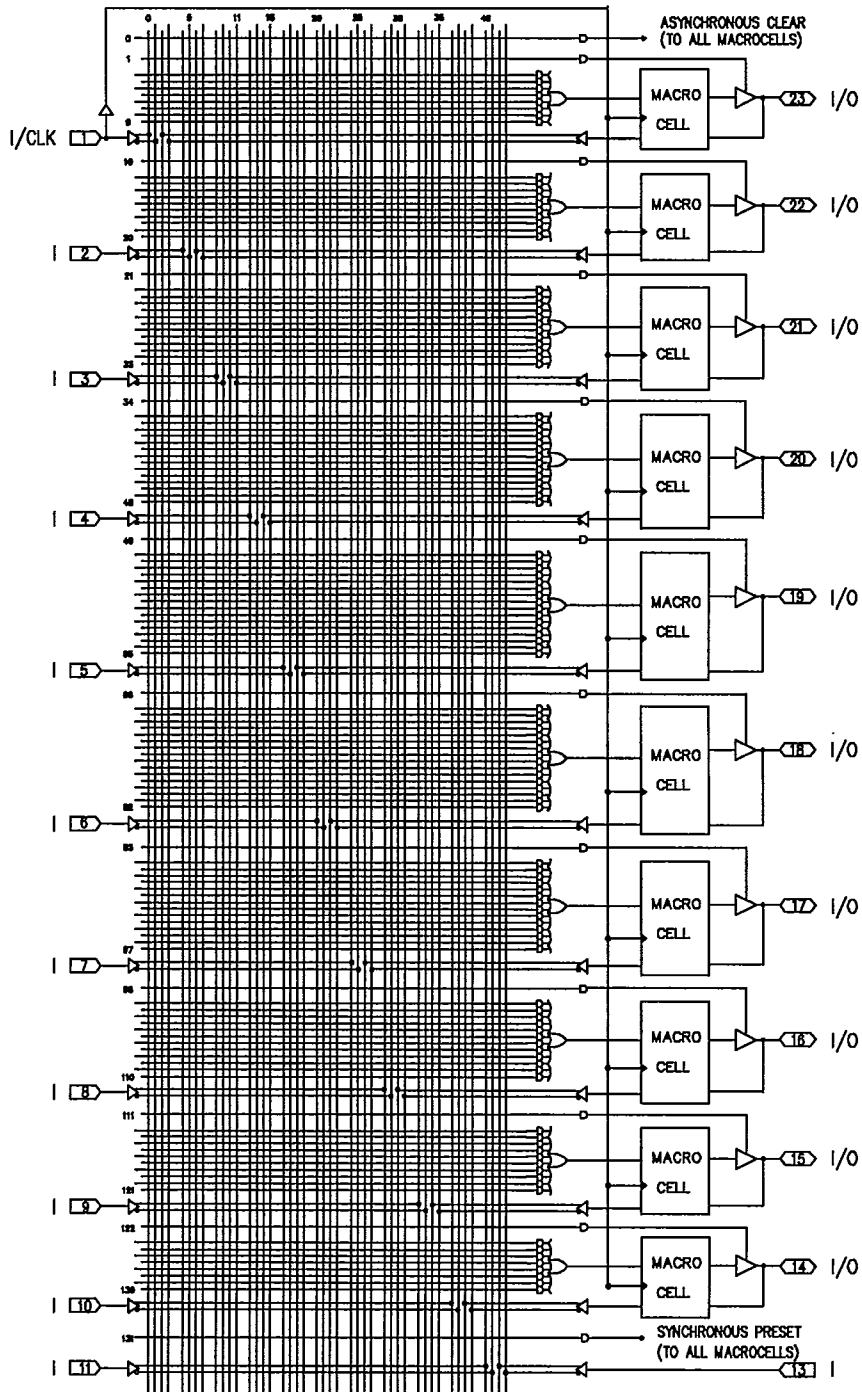


Figure 3. PEEL22CV10 Logic Array Diagram



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### Function Description

The PEEL22CV10 implements logic functions as sum-of-products expressions in a programmable-AND/fixed-OR logic array. User-defined functions are created by programming the connections of input signals into the array. User-configurable output structures in the form of I/O macrocells further increase logic flexibility.

### Architecture Overview

The PEEL22CV10 architecture is illustrated in the block diagram of figure 2. Twelve dedicated inputs and 10 I/Os provide up to 22 inputs and 10 outputs for creation of logic functions. At the core of the device is a programmable electrically-erasable AND array which drives a fixed OR array. With this structure, the PEEL22CV10 can implement up to 10 sum-of-products logic expressions.

Associated with each of the 10 OR functions is an I/O macrocell which can be independently programmed to one of 4 different configurations. The programmable macrocells allow each I/O to create sequential or combinatorial logic functions with either active-high or active-low polarity.

### AND/OR Logic Array

The programmable AND array of the PEEL22CV10 (shown in figure 3) is formed by input lines intersecting product terms. The input lines and product terms are used as follows:

44 Input Lines:

24 input lines carry the true and complement of the signals applied to the 12 input pins

20 additional lines carry the true and complement values of feedback or input signals from the 10 I/Os

132 product terms:

120 product terms (arranged in 2 groups of 8, 10, 12, 14, and 16) used to form logical sums

10 output enable terms (one for each I/O)

1 global synchronous present term

1 global asynchronous clear term

At each input-line/product-term intersection there is an EEPROM memory cell which determines whether or not there is a logical connection at that intersection. Each product term is essentially a 44-input AND gate. A product term which is connected to both the true and complement of an input signal will

always be FALSE, and thus will not effect the OR function that it drives. When all the connections on a product term are opened, a don't care state exists and that term will always be TRUE.

When programming the PEEL22CV10, the device programmer first performs a bulk erase to remove the previous pattern. The erase cycle opens every logical connection in the array. The device is then configured to perform the user-defined function by programming selected connections in the AND array. (Note that PEEL device programmers automatically program the connections on unused product terms so that they will have no effect on the output function)

### Variable Product Term Distribution

The PEEL22CV10 provides 120 product terms to drive the 10 OR functions. These product terms are distributed among the outputs in groups of 8, 10, 12, 14, and 16 to form logical sums (see figure 3). This distribution allows optimum use of device resources.

### Programmable I/O Macrocell

The output macrocell provides complete control over the architecture of each output. The ability to configure each output independently permits users to tailor the configuration of the PEEL22CV10 to the precise requirements of their designs.

### Macrocell Architecture

Each I/O macrocell, as shown in figure 4, consists of a D-type flip-flop and two signal-select multiplexers. The configuration of each macrocell of the PEEL22CV10 is determined by the two EEPROM bits controlling these multiplexers shown in table 1. Four EEPROM bits are used to determine the twelve-configuration macrocells of the PEEL22CV10 found in table 2. These bits determine output polarity, feedback paths, and output type (registered or non-registered). Equivalent circuits for the macrocell configurations are illustrated in figures 5 and 6.

### Output Type

The signal from the OR array can be fed directly to the output pin (combinatorial function) or latched in the D-type flip-flop (registered function). The D-type flip-flop latches data on the rising edge of the clock and is controlled by the global preset and clear terms. When the synchronous preset term is satisfied, the Q output of the register will be set HIGH at the next rising edge of the clock input. Satisfying the asynchronous clear term will set Q LOW, regardless of the clock state. If both terms are satisfied simultaneously, the clear will override the preset.

### Output Polarity

Each macrocell can be configured to implement active-high or active-low logic. Programmable polarity eliminates the need for external inverters.



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### Output Enable

The output of each I/O macrocell can be enabled or disabled under the control of its associated programmable output enable product term. When the logical conditions programmed on the output enable term are satisfied, the output signal is propagated to the I/O pin. Otherwise, the output buffer is driven into the high-impedance state.

Under the control of the output enable term, the I/O pin can function as a dedicated input, a dedicated output, or a bi-directional I/O. Opening every connection on the output enable term will permanently enable the output buffer and yield a dedicated output. Conversely, if every connection is intact, the enable term will always be logically false and the I/O will function as a dedicated input.

### Input/Feedback Select

When configuring an I/O macrocell to implement a registered function (configurations 1 and 2 in Figure 5), the Q output of the flip-flop drives the feedback term. When configuring an I/O macrocell to implement a combinatorial function (configurations 3 and 4 in Figure 5), the feedback signal is taken from the I/O pin. In this case, the pin can be used as a dedicated input or a bi-directional I/O. (Refer also to Table 1)

### Bi-directional I/O

The input/feedback signal is taken from the I/O pin when using the pin as a dedicated input or as a bi-directional I/O. (Note that it is possible to create a registered output function with bi-directional I/O.)

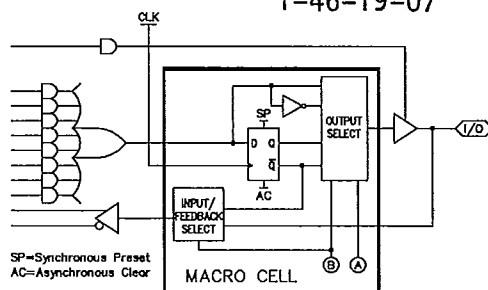


Figure 4. 22CV10 Macro Cell Block Diagram

### Combinatorial Feedback

The signal-select multiplexer gives the macrocell the ability to feedback the output directly from the OR gate, regardless of whether the output function is registered or combinatorial. This feature allows the creation of asynchronous latches, even when the output must be disabled. (Refer to configurations 5, 6, 7, and 8 in figure 6.)

### Registered Feedback

Feedback also can be taken from the register, regardless of whether the output function is to be combinatorial or registered. When implementing configurations 11 and 12 in figure 6, the register can be used for internal latching of data while leaving the external output free for combinatorial functions.

### Additional Macro Cell Configurations

Besides the standard four-configuration macro cells, each PEEL22CV10 provides an additional eight configurations (twelve total) that can be used to increase design flexibility (see figure 6). These configurations

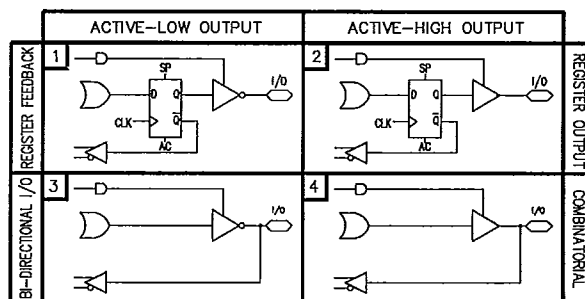


Figure 5. Equivalent Circuits for the Four Configurations of the PEEL22CV10 I/O Macrocell.

| Configuration |   |   | Input/Feedback Select | Output Select |
|---------------|---|---|-----------------------|---------------|
| #             | A | B |                       |               |
| 1             | 0 | 0 | Register Feedback     | Active Low    |
| 2             | 1 | 0 |                       | Active High   |
| 3             | 0 | 1 | Bi-Directional I/O    | Active Low    |
| 4             | 1 | 1 |                       | Active High   |

Table 1. PEEL22CV10 Macrocell Configuration Bits



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are the same provided by other PEEL devices, the 18CV8, 20CG10, and 22CV10Z. For logic assembly of all twelve configurations, specify PEEL22CV10A+ or PEEL22CV10Z (with Z-bit set to 1), and for programming select PEEL22CV10A+.

### Design Security

The PEEL22CV10 provides a special EEPROM security bit that prevents unauthorized reading or copying of designs programmed into the device. The security bit is set by the PLD programmer, either at the conclusion of the programming cycle or as a separate step, after the device has been

programmed. Once the security bit is set it is impossible to verify (read) or program the PEEL until the entire device has first been erased with the bulk-erase function.

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### Signature Word

The signature word feature allows a 24-bit code to be programmed into the PEEL22CV10. The code can be read back even after the security bit has been set. The signature word can be used to identify the pattern programmed into the device or to record the design revision, etc.

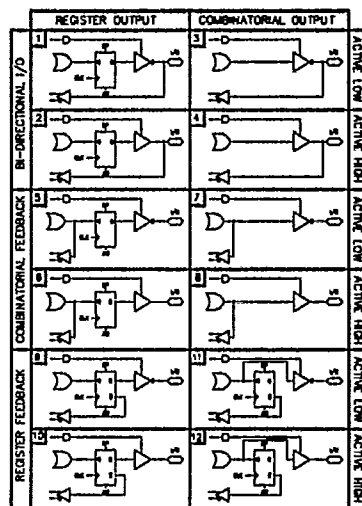


Figure 6. Equivalent Circuits for the Twelve Configurations of the PEEL22CV10A+ I/O Macrocell.

| Configuration |   |   |   |   | Input/Feedback Select  |  | Output Select |             |
|---------------|---|---|---|---|------------------------|--|---------------|-------------|
| #             | A | B | C | D |                        |  |               |             |
| 1             | 0 | 0 | 1 | 0 | Bi-Directional I/O     |  | Register      | Active Low  |
| 2             | 1 | 0 | 1 | 0 | "                      |  | "             | Active High |
| 3             | 0 | 1 | 0 | 0 | "                      |  | Combinatorial | Active Low  |
| 4             | 1 | 1 | 0 | 0 | "                      |  | "             | Active High |
| 5             | 0 | 0 | 1 | 1 | Combinatorial Feedback |  | Register      | Active Low  |
| 6             | 1 | 0 | 1 | 1 | "                      |  | "             | Active High |
| 7             | 0 | 1 | 1 | 1 | "                      |  | Combinatorial | Active Low  |
| 8             | 1 | 1 | 1 | 1 | "                      |  | "             | Active High |
| 9             | 0 | 0 | 0 | 0 | Register Feedback      |  | Register      | Active Low  |
| 10            | 1 | 0 | 0 | 0 | "                      |  | "             | Active High |
| 11            | 0 | 1 | 1 | 0 | "                      |  | Combinatorial | Active Low  |
| 12            | 1 | 1 | 1 | 0 | "                      |  | "             | Active High |

Table 2. PEEL22CV10A+ Macrocell Configuration Bits



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## Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage

| Symbol                          | Parameter                               | Conditions                                   | Rating                         | Unit |
|---------------------------------|---|--|--------------------------------|------|
| V <sub>CC</sub>                 | Supply Voltage                          | Relative to GND                              | – 0.5 to + 7.0                 | V    |
| V <sub>I</sub> , V <sub>O</sub> | Voltage Applied to Any Pin <sup>6</sup> | Relative to GND <sup>1</sup>                 | – 0.5 to V <sub>CC</sub> + 0.6 | V    |
| I <sub>O</sub>                  | Output Current                          | Per pin (I <sub>OL</sub> , I <sub>OH</sub> ) | ± 25                           | mA   |
| T <sub>ST</sub>                 | Storage Temperature                     |  | – 65 to +150                   | °C   |
| T <sub>LT</sub>                 | Lead Temperature                        | Soldering 10 seconds                         | + 300                          | °C   |

## Operating Ranges<sup>2</sup>

| Symbol            | Parameter                 | Conditions | Min  | Max  | Unit |
|-------------------|---------------------------|------------|------|------|------|
| V <sub>CC</sub>   | Supply Voltage            | Commercial | 4.75 | 5.25 | V    |
|                   |                           | Industrial | 4.5  | 5.5  | V    |
| T <sub>A</sub>    | Ambient Temperature       | Commercial | 0    | + 70 | °C   |
|                   |                           | Industrial | – 40 | + 85 | °C   |
| T <sub>R</sub>    | Clock Rise Time           | See note 4 |      | 250  | ns   |
| T <sub>F</sub>    | Clock Fall Time           | See note 4 |      | 250  | ns   |
| T <sub>RVCC</sub> | V <sub>CC</sub> Rise Time | See note 4 |      | 250  | ms   |

## D.C. Electrical Characteristics

Over the operating range

| Symbol                        | Parameter                    | Conditions  | Min                   | Max                   | Unit |
|-------------------------------|------------------------------|---|-----------------------|-----------------------|------|
| V <sub>OH</sub>               | Output HIGH Voltage - TTL    | V <sub>CC</sub> = Min, I <sub>OH</sub> = – 4.0mA                                | 2.4                   |                       | V    |
| V <sub>OHc</sub>              | Output HIGH Voltage-CMOS     | V <sub>CC</sub> = Min, I <sub>OH</sub> = –10μA                                  | V <sub>CC</sub> – 0.1 |                       | V    |
| V <sub>OL</sub>               | Output LOW Voltage - TTL     | V <sub>CC</sub> = Min, I <sub>OL</sub> = 8mA                                    |                       | 0.5                   | V    |
| V <sub>OLc</sub>              | Output LOW Voltage-CMOS      | V <sub>CC</sub> = Min, I <sub>OL</sub> = 10μA                                   |                       | 0.1                   | V    |
| V <sub>IH</sub>               | Input HIGH Level             |   | 2.0                   | V <sub>CC</sub> + 0.3 | V    |
| V <sub>IL</sub>               | Input LOW Level              |   | – 0.3                 | 0.8                   | V    |
| I <sub>IL</sub>               | Input Leakage Current        | V <sub>CC</sub> = Max, GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>                  |                       | ±10                   | μA   |
| I <sub>OZ</sub>               | Output Leakage Current       | I/O = High-Z, GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub>                            |                       | ±10                   | μA   |
| I <sub>SC</sub>               | Output Short Circuit Current | V <sub>CC</sub> =5V, V <sub>O</sub> =0.5V <sup>10</sup> , T <sub>A</sub> =25°C  | – 30                  | –90                   | mA   |
| I <sub>CC</sub>               | V <sub>CC</sub> Current      | V <sub>IN</sub> = 0V or 3V <sup>5,11</sup><br>f = 25MHz<br>All outputs disabled |                       | 67                    | mA   |
| C <sub>IN</sub> <sup>8</sup>  | Input Capacitance            | T <sub>A</sub> = 25°C, V <sub>CC</sub> = 5.0V<br>@ f = 1MHz                     |                       | 6                     | pF   |
| C <sub>OUT</sub> <sup>8</sup> | Output Capacitance           |   |                       | 12                    | pF   |



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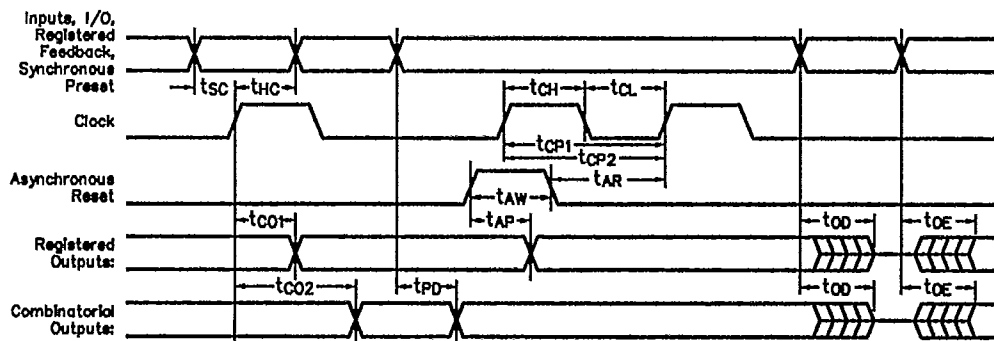
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A.C. Electrical Characteristics Over the Operating Range <sup>9,12</sup>

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| Symbol                            | Parameter   | 22CV10-25 |     | Unit |
|-----------------------------------|---|-----------|-----|------|
|                                   |   | Min       | Max |      |
| t <sub>PD</sub>                   | Input <sup>6</sup> or feedback to non-registered output                         |           | 25  | ns   |
| t <sub>OE</sub>                   | Input <sup>6</sup> to output enable <sup>7</sup>                                |           | 25  | ns   |
| t <sub>OD</sub>                   | Input <sup>6</sup> to output disable <sup>7</sup>                               |           | 25  | ns   |
| t <sub>CO1</sub>                  | Clock to output   |           | 15  | ns   |
| t <sub>CO2</sub>                  | Clock to combinatorial output delay via internal registered feedback            |           | 35  | ns   |
| t <sub>SC</sub>                   | Input <sup>6</sup> or feedback setup to clock                                   | 15        |     | ns   |
| t <sub>HC</sub>                   | Input <sup>6</sup> hold after clock   | 0         |     | ns   |
| t <sub>CL</sub> , t <sub>CH</sub> | Clock width - clock low time, clock high time <sup>4</sup>                      | 13        |     | ns   |
| t <sub>CP1</sub>                  | Minimum clock period (register feedback to registered output via internal path) | 27        |     | ns   |
| f <sub>max1</sub>                 | Maximum clock frequency (1/t <sub>CP1</sub> )                                   | 37        |     | MHz  |
| t <sub>CP2</sub>                  | Minimum clock period (t <sub>SC</sub> + t <sub>CO1</sub> )                      | 30        |     | ns   |
| f <sub>max2</sub>                 | Maximum clock frequency (1/t <sub>CP2</sub> )                                   | 33.3      |     | MHz  |
| t <sub>AW</sub>                   | Asynchronous Reset pulse width  | 25        |     | ns   |
| t <sub>AP</sub>                   | Input <sup>6</sup> to Asynchronous Reset  |           | 25  | ns   |
| t <sub>AR</sub>                   | Asynchronous Reset recovery time  |           | 25  | ns   |
| t <sub>RESET</sub>                | Power-on reset time for registers in clear state <sup>4</sup>                   |           | 5   | μs   |

## Switching Waveforms



1. Minimum DC input is -0.5V, however inputs may undershoot to -2.0V for periods less than 20ns.
2. Contact ICT for other operating ranges.
3. V<sub>I</sub> and V<sub>O</sub> are not specified for program/verify operation.
4. Test points for Clock and V<sub>CC</sub> in t<sub>sc</sub>, t<sub>hc</sub>, t<sub>cl</sub>, t<sub>ch</sub>, and t<sub>RESET</sub> are referenced at 10% and 90% levels.
5. I/O pins are 0V or 3V.
6. "Input" refers to an Input pin signal.
7. t<sub>OE</sub> is measured from input transition to V<sub>REF</sub> ± 0.1V, t<sub>OD</sub> is measured from input transition to V<sub>OH</sub> - 0.1V or V<sub>OL</sub> + 0.1V; V<sub>REF</sub> = V<sub>I</sub> see test loads at the end of this section.

8. Capacitances are tested on a sample basis.
9. Test conditions assume: signal transition times of 5ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
10. Test one output at a time for a duration of less than 1 sec.
11. ICC for a typical application: This parameter is tested with the device programmed as a 10-bit Counter.
12. PEEL Device test loads are specified at the end of this section.