One Chip Voice Recognition LSI

RF5A128(OTP ROM)/RF5S830(MASK ROM)

OUTLINE

RICOH's One Chip Voice Recognition LSI is highly integrated IC that includes most of components (Mike AMP., ADC, Feature Extractor, CPU, Software Memories and Dictionary Memories) necessary for Voice Recognition system.
You can create Voice Recognition products simply and easily with this LSI and some external parts.

RF5A128 includes OTP (One Time Programmable) ROM for the Voice-Dictionary and software. It can be used for development and evaluation.

RF5S830 includes MASK ROM (other specifications are same as RF5A128) for mass production.

FEATURES

1. Functions

- One chip voice recognition LSI using RICOH's original BTSP (Binary Time Spectrum Pattern) method
- Adaptable for both speaker independent and dependent system
- Vocabulary* (Total time length)
  Speaker dependent 3 words (2 seconds)
  Speaker independent 10 words (7 seconds)
  * Expandable with external memories. A special control program should be developed to expand it.
- Including MIKE Amp. AD Converter, Dictionary Memories.
  A voice recognition system can be constructed only with the installation of some external capacitors (C) and resistors (R).
- User application available for implementation.
  The built-in CPU core "Ru8" with RICOH's original 16bit internal architecture allows implementation of a user application in addition to the voice recognition feature.
  Also available for use as a system controller with a voice recognition feature.
- Adaptable to multiple languages
  The same hardware allows adaptation to multiple languages such as Japanese, English, and German.
- Stand Alone mode (Switch port interface)
  8bit input, 8bit output
- External Host interface mode
  8bit data bus, 5bit control lines
- 8bit general I/O ports
- Standby mode (sleep input, wake up input)
- 80pin QFP

2. Hardware

- Internal CPU ····· Ru8 : RICOH's original 8bit (16bit internal) CPU
- Memories area inside ····· ROM 40kB (RF5A128-OTP ROM, RF5S830-MASK ROM)
  RAM 2kB
- Execution time ····· 125ns/ 15MHz (4.5 to 5.5V : Fastest command execution)
- Address space ····· 64kB (MAX.)
- AD Converter ····· 10bit (conversion time 21.0µs)
- Timer ····· 16bit reloadable timer × 1
  8bit watch dog timer × 1
- Interrupts ····· 3 external pins (WAKEUP, SLEEP, SRESET), External interface × 1, ADC × 1, Internal Timer × 1, NMI × 1
- Multiplier/ Divider ····· 16bit×16bit+32bit→32bit (signed), 32bit/ 16bit→16bit (unsigned)
- I/ O Ports ····· 8bit×3 (Software controllable input/ output)
- Mike Amp. gain ····· 60dB (MAX.)
- Buffer Amp. ····· 1 voltage follower for the anti-alias filter
- Clock frequency ····· 16MHz
- Operating voltage ····· 5V±10%
- Operating current ····· 50mA (MAX.)
- Stand-by current ····· 50µA (MAX.)

3. Memory capacity for the software

- Voice Recognition ····· ROM 20kB, RAM 1.2kB
- Independent dictionary ····· ROM 16kB (MAX.) (internal)
- Dependent dictionary ····· RAM 700B (MAX.) (internal)
- Users area ····· ROM 4kB, RAM 100B

4. Voice Recognition Specification

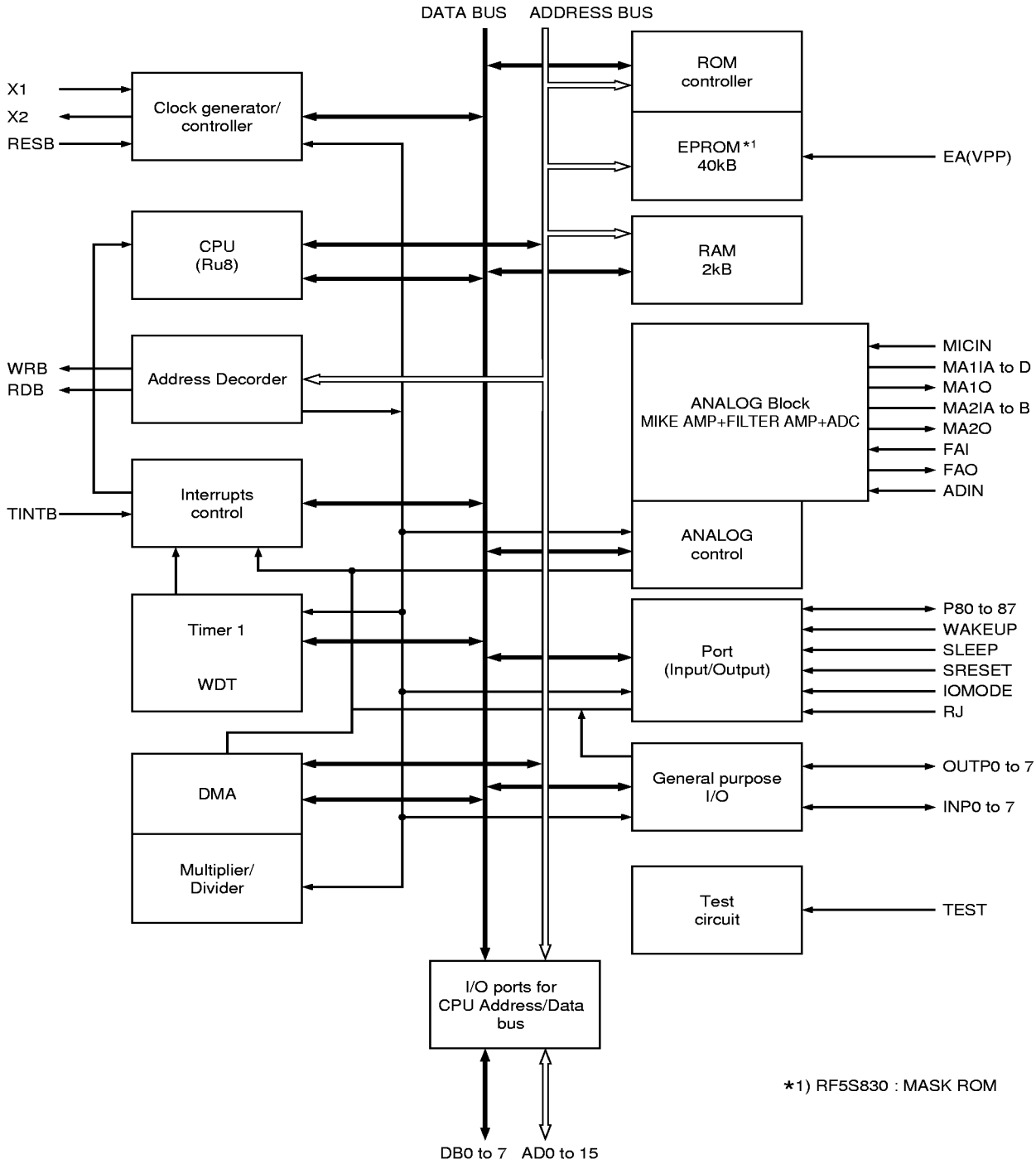
• Method	BTSP (Binary Time Spectrum Pattern)
• Speaker type	Discrete utterance. Speaker Independent and Dependent
• Word length	0.15 to 2.0 second/ word
• Word-to-word discreet time	Over 350ms
• Functions	Recognition (one time/ repetitive) Registration (Speaker Dependent) Deletion (Speaker Dependent) Reject Level Change
• Registration times	3 utterances/ 1 Word registration
• Dictionary capacity	Dependent $(66+200\times a) \times n+2$ (B) Independent $((66+400\times a) \times n+2) \times t$ (B) a : average dictionary-word length (s) n : number of words t : number of multi-templates (Independent only)

APPLICATIONS

Voice control for such applications as toys, video games, personal computers, PDA, home automation, office automation (OA), and factory automation (FA).

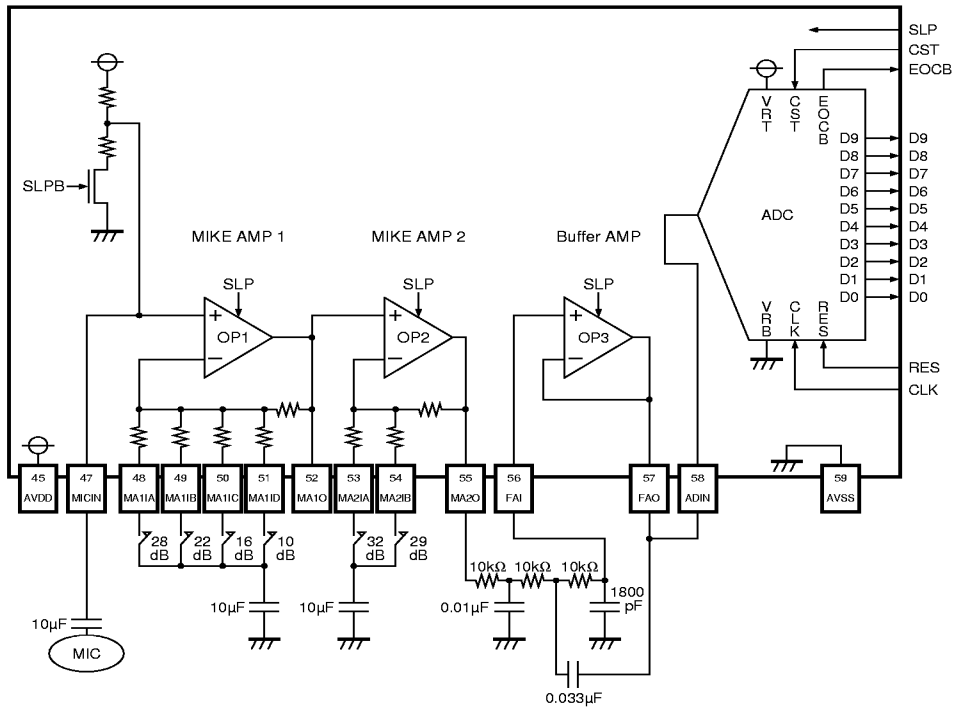
BLOCK DIAGRAM

• **RF5A128 Main Block Diagram**



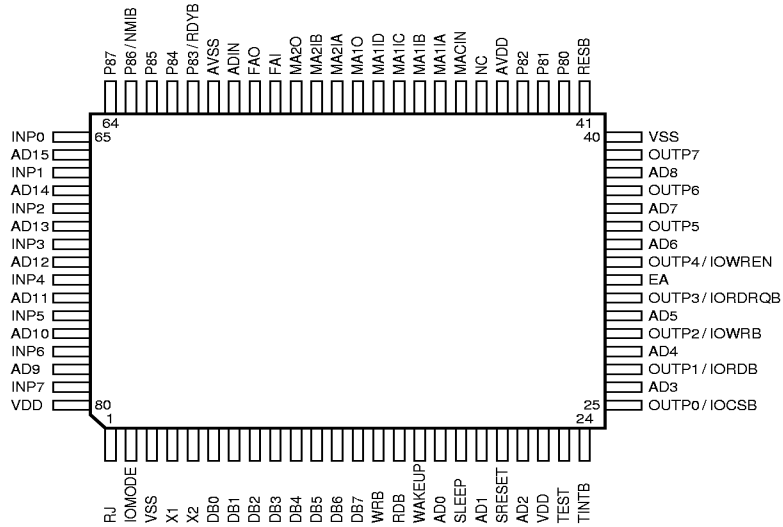
*1) RF5S830 : MASK ROM

• **ANALOG Block Diagram**



PIN CONFIGURATION

• **80 pin QFP**



PIN DESCRIPTION

Pin.NO.	SIGNAL	I/O*1	RESET*2	DESCRIPTION
4 5	X1 X2	I O	—	Clock pins. External vibrator can be connected. Externally-supplied clock signal can be connected to X1, with X2 opened.
41	RESB	I	PU	Reset input. LSI is RESET when this pin is LOW.
65,67,69 71,73,75 77,79	INP0 to 7	I/O (SPU)	HiZ	Stand Alone Mode : Command Inputs for Switches.
			HiZ	External Host Mode : Bi-directional DATA ports. The direction is controlled by IOCSB and (IOWRB or IORDB) input.
25,27,29 31,33,35 37,39	OUTP0 to 7	I/O (SPU)	HiZ	Stand Alone Mode : Results Outputs for drivers, etc.
				External Host Mode : DATA read and write control pins.
			HiZ	OUTP0 : IOCSB input Chip select from host.
			HiZ	OUTP1 : IORDB input Read signal from host.
			HiZ	OUTP2 : IOWRB input Write signal from host.
			H	OUTP3 : IORDRQB output Read request to host.
			H	OUTP4 : IOWREN output Write enable to host.
			HiZ	OUTP5 to 7 : Aux. IO port.
16	WAKEUP	I	PU	Wake up pulse signal input. This pin must be opened when not in use.
18	SLEEP	I	PU	Sleep pulse signal input.This pin must be opened when not in use.
20	SRESET	I	PU	Software reset pulse signal input.This pin must be opened when not in use.
2	IOMODE	I	HiZ	I/O mode selection input. L : Stand Alone Mode H : External Host Mode
1	RJ	I	HiZ	Reject Level selection input. L : Reject Level LOW H : Reject Level HIGH
42 to 44, 61,62,64	P80 to 82 P84,85,87	I/O	HiZ	General purpose I/O port. P80 is used to select Dependent-Dictionary.
60	P83/ RDYB	I/O	HiZ	General purpose I/O port. When this signal is low, the CPU's external access can be held. (When RDYB function enabled by the software.)
63	P86/ NMIB	I/O	HiZ	General purpose I/O port. When this signal goes to low, the internal NMI request is asserted. (When NMIB function enabled by the software.)

Pin.NO.	SIGNAL	I/O*1	RESET*2	DESCRIPTION
32	EA	I	—	ROM mode selection input. This signal is referenced during RESET state. L : External ROM mode H : Internal ROM mode
47	MICIN	I	—	Microphone inout.
48 to 51	MA1IA to D	—	—	Gain setting pins of MikeAmp 1. Several gain settings are obtained using external condenser connection.
52	MA1O	O	—	Output of MikeAmp 1. This is internally connected to the input of MikeAmp 2.
53 to 54	MA2IA to B	—	—	Gain setting pins of MikeAmp2. Several gain settings are obtained using external condenser connection.
56	FAI	I	—	Input of Buffer Amp for anti-alias filter.
57	FAO	O	—	Output of Buffer Amp for anti-alias filter.
58	ADIN	I	—	Input of AD converter.
17,19,21,26, 28,30,34,36, 38,78,76,74, 72,70,68,66	AD0 to 15	O	L *3	Address signal outputs for External ROM mode. Low level is output when Internal ROM mode *4
6 to 13	DB0 to 7	I/ O	L *3	DATA bus for External ROM mode. Low level is output when Internal ROM mode *4
15	RDB	O	H *3	Read signal outputs for External ROM mode. High level is output when Internal ROM mode *4
14	WRB	O	H *3	Write signal outputs for External ROM mode. High level is output when Internal ROMmode *4
23	TEST	I	PU	TEST pin. This must be opened or connected to the VDD.
24	TINTB	I	PU	TEST pin. This must be opened or connected to the VDD.
22,45,80	VDD, AVDD	—	—	Power Supply.
3,40,59	VSS, AVSS	—	—	Ground.

*1) Software Pull Up (SPU)means that internal pull-up can be controlled(ON/OFF) by software.
*2) PU means internal pull-up Input.
*3) These pins are set to VECTOR reading state when reset to External ROM mode.
*4) These pins are also activated when External address space is accessed, even in Internal ROM mode.

ABSOLUTE MAXIMUM RATING

Symbol	Item	Conditions	Rating	Unit
V_{CC}	Power supply voltage	VDD, AVDD pin *1, 2	–0.3 to 7.0	V
V_{TE}	Terminal Voltage		–0.3 to VCC+0.3	V
Tstg	Storage Temperature		–40 to 125	°C
P_D	Power Dissipation	TA=70°C	600	mW

*1) Power supply Pins are VDD, AVDD.
*2) The voltage difference of each power supply pin must not exceed 0.3V.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum ratings are threshold limit values that must not be exceeded even for an instant under any conditions. Moreover, such values for any two items must not be reached simultaneously. Operation above these absolute maximum ratings may cause degradation or permanent damage to the device. These are stress ratings only and do not necessarily imply functional operation below these limits.

RECOMMENDED OPERATING CONDITIONS

Symbol	Item	Conditions	Rating	Unit
V_{CC}	Power supply voltage	VDD, AVDD pin *1, 2	4.5 to 5.5	V
V_{TE}	Terminal Voltage		0 to Vcc	V
Top	Operating Temperature		0 to 70	°C
F_{CLK}	Operation Clock Frequency	(16.0MHz Software default)	15.2 to 16.8	MHz

*1) Power supply Pins are VDD, AVDD.
*2) The voltage difference of each power supply pin must not exceed 0.3V.

ELECTRICAL CHARACTERISTICS (ANALOG)

• Microphone amplifiers, Buffer amplifiers.

(Ta=0 to 70°C, V_{DD}=4.5 to 5.5V)

Symbol	Item	Conditions	Limits			Unit
			MIN.	TYP.	MAX.	
V_{DD}	Power Spply Voltage		4.5		5.5	V
I_{DDA}	Operating Current	No input signal (ADC not included)		1.5	2.4	mA
V_{REF}	Reference Voltage	V_{DD}=5.0V	2.4	2.5	2.6	V
V_{OF12}	Mike amp offset voltage		–10	0	10	mV
V_{OF3}	Buffer amp offset voltage		–20	0	20	mV
G_{MA1A}	Mike amp 1A Closed Loop Voltage Gain		27.5	28.0	28.5	dB
G_{MA1B}	Mike amp 1B Closed Loop Voltage Gain		21.5	22.0	22.5	dB
G_{MA1C}	Mike amp 1C Closed Loop Voltage Gain		15.5	16.0	16.5	dB
G_{MA1D}	Mike amp 1D Closed Loop Voltage Gain		9.5	10.0	10.5	dB
G_{MA2A}	Mike amp 2A Closed Loop Voltage Gain		31.5	32.0	32.5	dB
G_{MA2B}	Mike amp 2B Closed Loop Voltage Gain		28.5	29.0	29.5	dB

• ADC

(Ta=0 to 70°C, V_{DD}=4.5 to 5.5V)

Symbol	Item	Conditions	Limits			Unit
			MIN.	TYP.	MAX.	
RES	ADC resolution			10		Bit
V_{AIN}	Input voltage range		0		V_{DD}	V
E_{NL}	Linearity Error		–4	±2	+4	LSB
E_{ZS}	Offset Error Zero scale		–4	±2	+4	LSB
E_{FS}	Offset Error Full scale		–4	±2	+4	LSB
C_{IN}	Inport Capacitance			5	10	pF
F_{CLK}	Input Clock Frequency				1	MHz
T_{CON}	Conversion Time	F_{CLK}*=1MHz	21.0			µs
I_{DDA}	Operating Current (continuous)			3	5	mA
I_{DDS}	Operating Current (interval)	F_{CLK}*=1MHz Sampling frequency=8kHz		0.5	0.8	mA

*) FCLK is set by software

ELECTRICAL CHARACTERISTICS (DIGITAL)

• DC Characteristics

(Ta=0 to 70°C, V_{DD}=4.5 to 5.5V)

Symbol	Item	Conditions	Limits			Unit
			MIN.	TYP.	MAX.	
V_{IH}	"H" Input Voltage (CMOS)		V_{DD}×0.7		V_{DD}+0.3	V
V_{I}	"L" Input Voltage (CMOS)		–0.3		V_{DD}×0.3	V
V_{OH}	"H" Output Voltage	V_{DD}=4.5V, I_{OH}=–4mA	2.4			V
V_{OL}	"L" Output Voltage	V_{DD}=4.5V, I_{OL}=–4mA			0.4	V
I_{LI}	Input Current	V_{I}=0 to V_{DD}	–10		10	µA
I_{OZ}	Off State Output Current	V_{O}=0 to V_{DD}	–10		10	µA
I_{IH}	Pull up Leak Current	V_{I}=V_{DD}			10	µA
I_{IL}	Pull up Leak Current	V_{I}=0V	–10		–200	µA
I_{IH1}	X1 Leak Current	V_{I}=V_{DD}			50	µA
I_{IL1}	X1 Leak Current	V_{I}=0V			–50	µA
V_{T+-}	V_{T-} Hysteresis		0.3		0.73	V
V_{T+}	Input High Level Threshold		3.8			V
V_{T-}	Input Low Level Threshold				1.3	V
I_{CCS}	Stand-by Current				50	µA
I_{CC}	Operating Current				50	mA

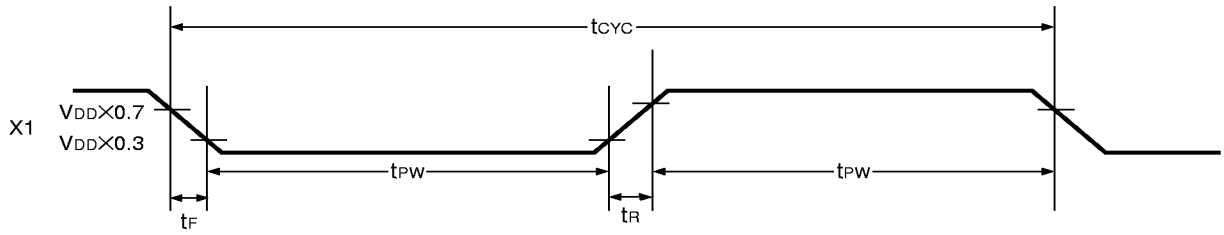
*) The direction of current flow to the LSI is assumed to be positive (+).

• AC Characteristics

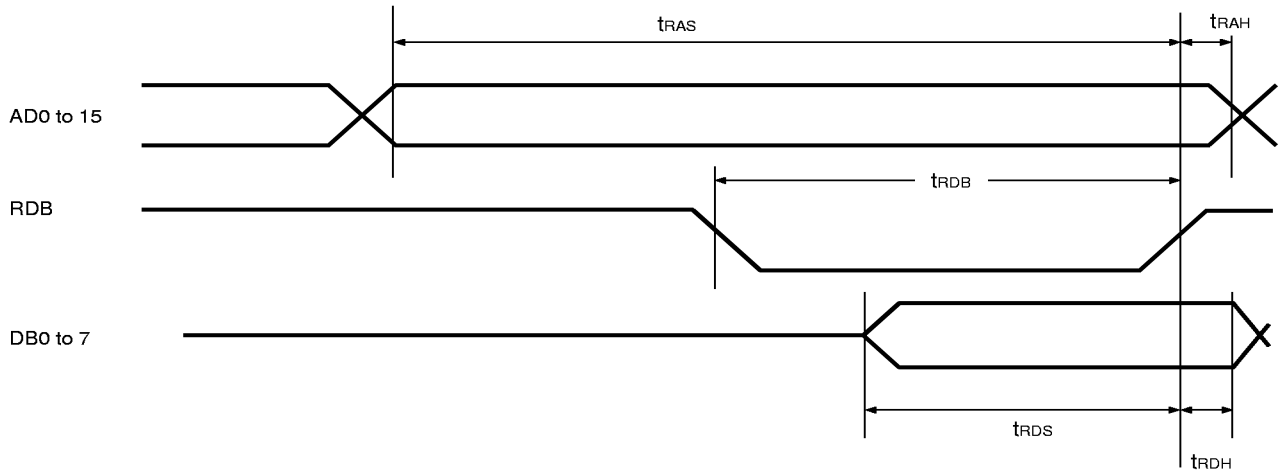
(Ta=0 to 70°C, V_{DD}=5.0V±10%)

Symbol	Item	Limits			Unit
		MIN.	TYP.	MAX.	
t_{CYC}	Clock Cycle		62.5		ns
t_{PW}	Clock Pulse Width (H,L)	27			ns
t_R	Clock Rising Time			5	ns
t_F	Clock Falling Time			5	ns
t_{SYS}	System Clock		t_{CYC}×2		ns
t_{RAS}	Read Address Set Up Time	90			ns
t_{RAH}	Read Address hold Time	5		50	ns
t_{RDS}	Read Data Set Up Time	50			ns
t_{RDH}	Read Data Hold Time	0			ns
t_{RDB}	Read Pulse Width	60	t_{CYC}		ns
t_{WAS}	Write Address Set Up Time	80			ns
t_{WAH}	Write Address Hold Time	5			ns
t_{WDD}	Write Data Delay Time			30	ns
t_{WDH}	Write Data Hold Time	5			ns
t_{WRB}	Write Pulse Width	60	t_{CYC}		ns

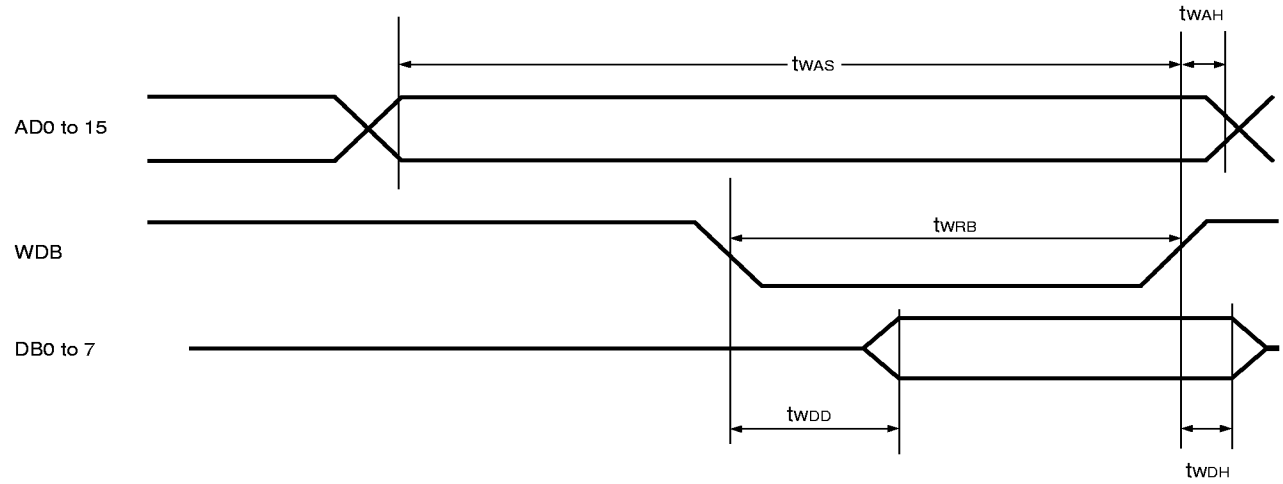
· Clock Timing



· **Data Read Bus Timing (0 Wait)**



· **Data Write Bus Timing (0 Wait)**

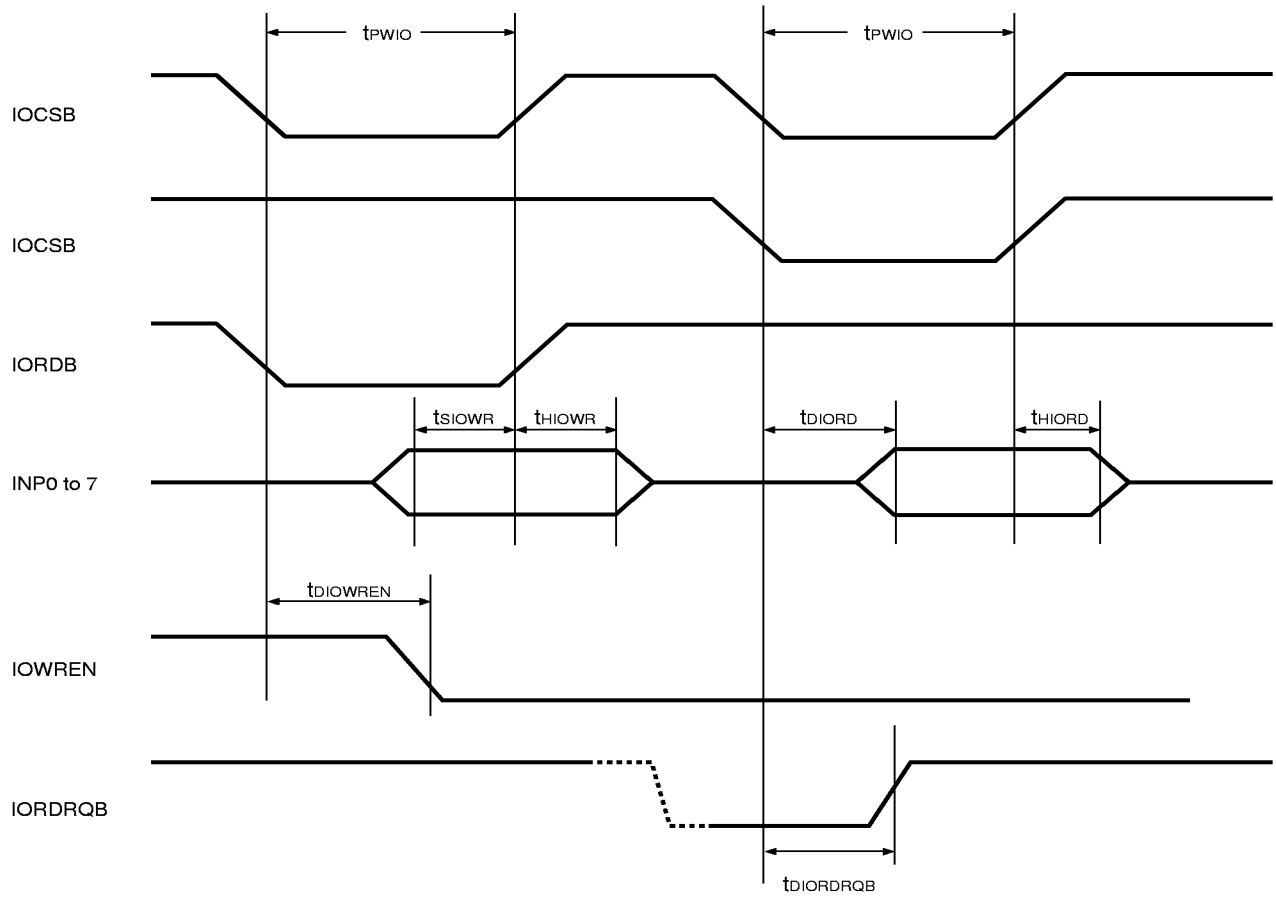


• AC Characteristics (I/O Part, when External Host Mode)

(Ta=0 to 70°C, V_{DD}=5.0V±10%)

Symbol	Item	Limits			Unit
		MIN.	TYP.	MAX.	
t_{PWIO}	I/O Control Signal Width	100			ns
t_{DIORD}	I/O Read Data Delay Time			50	ns
t_{HIORD}	I/O Read Data Hold Time	5			ns
t_{SIOWR}	I/O Write Data Setup Time	30			ns
t_{HIOWR}	I/O Write Data Hold Time	15			ns
$t_{DIORDRQB}$	IORDRQB Disable Delay Time			50	ns
$t_{DIOWREN}$	IOWREN Disable Delay Time			50	ns

• External Host Mode Control Signal Timing



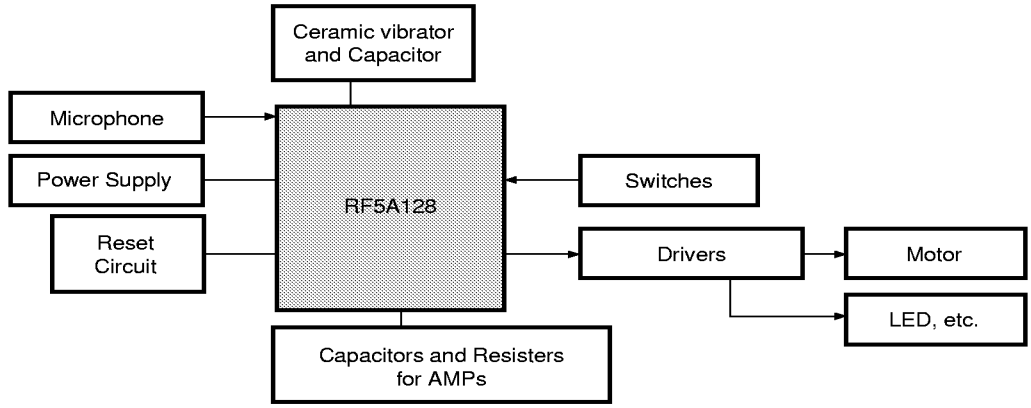
FUNCTION DESCRIPTION

(Contents of this section is about RF5A128's Standard Software.)

1. Stand Alone Mode (Switch Port Interface)

In Stand Alone Mode, INP terminals are used for Switch Input for Commands and OUTP terminals are used for Result Outputs. Switches can be directly connected because of internal pull up ability.

1.1 System Block Diagram (example)



1.2 Pin Function Description

Pin	Function (Recognition)	Function (Registration/Deletion)	Remarks
INP0	Dependent	Word Number bit0	Mode setting pins. These settings are referenced when Command pins are TRUE. "L" level is TRUE, Word Number should be Binary encoded.
INP1	Independent	Word Number bit1	
INP2	Invalid Rejection	Word Number bit2	
INP3	—	Registration	Command pins. (for momentary switch) "L" level is TRUE.
INP4	Single Recog.	—	
INP5	Repetitive Recog.	—	
INP6	—	Deletion	
INP7	Cluster	Cluster	Cluster setting pin. "H" is cluster 1, "L" is cluster 2.
OUTP0	Word Number bit0	Word Number bit0	"H" level is TRUE.
OUTP1	Word Number bit1	Word Number bit1	"H" level is TRUE.
OUTP2	Word Number bit2	Word Number bit2	"H" level is TRUE.
OUTP3	Word Number bit3	—	"H" level is TRUE. Word Number is Binary encoded.
OUTP4	Result Dependent	Error Status 1	"H" indicates that result is speaker dependent.*

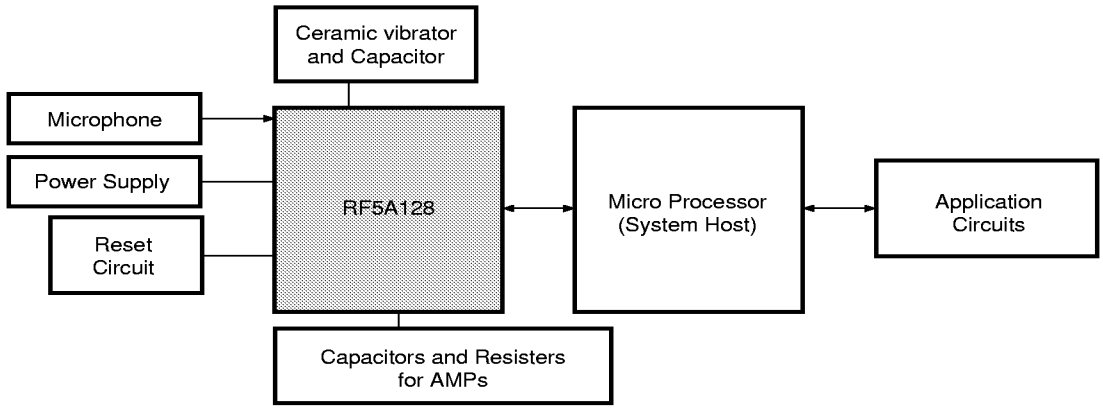
Pin	Function (Recognition)	Function (Registration/Deletion)	Remarks
OUTP5	Wait for Recog.	Error Status 2	"H" while waiting voice. "L" while utterance.*
OUTP6	No Result	—	"H" indicates that result invalid.
OUTP7	—	Waite for Register Error status 3	"H" while waiting voice. "L" while utterance. *
P80	Dictionary RAM setting input	Dictionary RAM setting input	"H" : Internal RAM "L" : External RAM
P81 to 87	—	—	Normally "L" output

*) If Error,These pins are set to "H" for a while.

2. External Host Mode (Micom Port Interface)

In External Host Mode, INP terminals are used for Data bus for Commands and Results. And OUTP terminals are used for BUS control signals.

2.1 System Block Diagram (example)



2.2 Pin Function Description

Pin	Function	Remarks
INP0	Data0	Bidirectional DATA bus. The direction is determined by the control signal combination.
INP1	Data1	
INP2	Data2	
INP3	Data3	
INP4	Data4	
INP5	Data5	
INP6	Data6	
INP7	Data7	
OUTP0	IOCSB Input	Chip select input. “L” true.
OUTP1	IORDB Input	Data read input. “L” true.
OUTP2	IOWRB Input	Data write input. “L” true.
OUTP3	IORDRQB Output	Read request output. It is “L” when read (by Host) data is valid.
OUTP4	IOWREN Output	Write request output. The Host can write data when it is “H”.
OUTP5	—	
OUTP6	—	
OUTP7	—	
P80	Dictionary RAM setting input	“H” : Internal RAM “L” : External RAM
P81 to 87	—	Normally “L” output

2.3 Commands

2.3-1 Communication Check Command (Host→RF5A128)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0

2.3-2 Voice Command (Host→RF5A128)

D7	D6	D5	D4	D3	D2	D1	D0
1							

Cluster Control*1	
00	All Cluster*2
01	Cluster 1
10	Cluster 2
11	reserved

Recognition Control*3		
Dependent	0	OFF
	1	ON
Independent	0	OFF
	1	ON
Reject Invalid	0	OFF
	1	ON

Registration / Detection Control*3	
000	reserved
001	Word Number 1
010	Word Number 2
011	Word Number 3
100	Word Number 4
101	Word Number 5
110	Word Number 6
111	Word Number 7

Command Identifier	
00	Registraction
10	Deletion
11	Recognition

*1) Cluster Control is valid when "Recognition" and "Registration"
*2) "All Cluster" is valid when "Recognition"
*3) Function of Bit D2 to D4 is different between Registration/Deletion mode and Recognition mode.

2.4 Responses

2.4-1 Communication Check Response (RF5A128→Host)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	0

means the communication is OK.

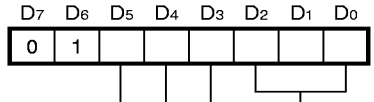
2.4-2 Recognition Results (RF5A128→Host)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1						

Recognition Result	
0000	No valid result
0001	Word Number 1
0010	Word Number 2
0011	Word Number 3
0100	Word Number 4
0101	Word Number 5
0110	Word Number 6
0111	Word Number 7
1000	Word Number 8
1001	Word Number 9
1010	Word Number 10
1011	reserved
1100	reserved
1101	reserved
1110	reserved
1111	reserved

Status		
Speaker Type	0	Independent
	1	Dependent
Error occured	0	NO
	1	YES

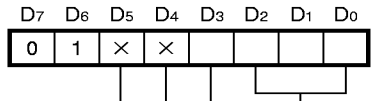
2.4-3 Registration Results (RF5A128→Host)



Registration Result	
000	reserved
001	Word Number 1
010	Word Number 2
011	Word Number 3
100	Word Number 4
101	Word Number 5
110	Word Number 6
111	Word Number 7

Status		
Complete	0	NO
	1	YES
Capacity Error	0	NO
	1	YES
Other Errors	0	NO
	1	YES

2.4-4 Deletion Results (RF5A128→Host)



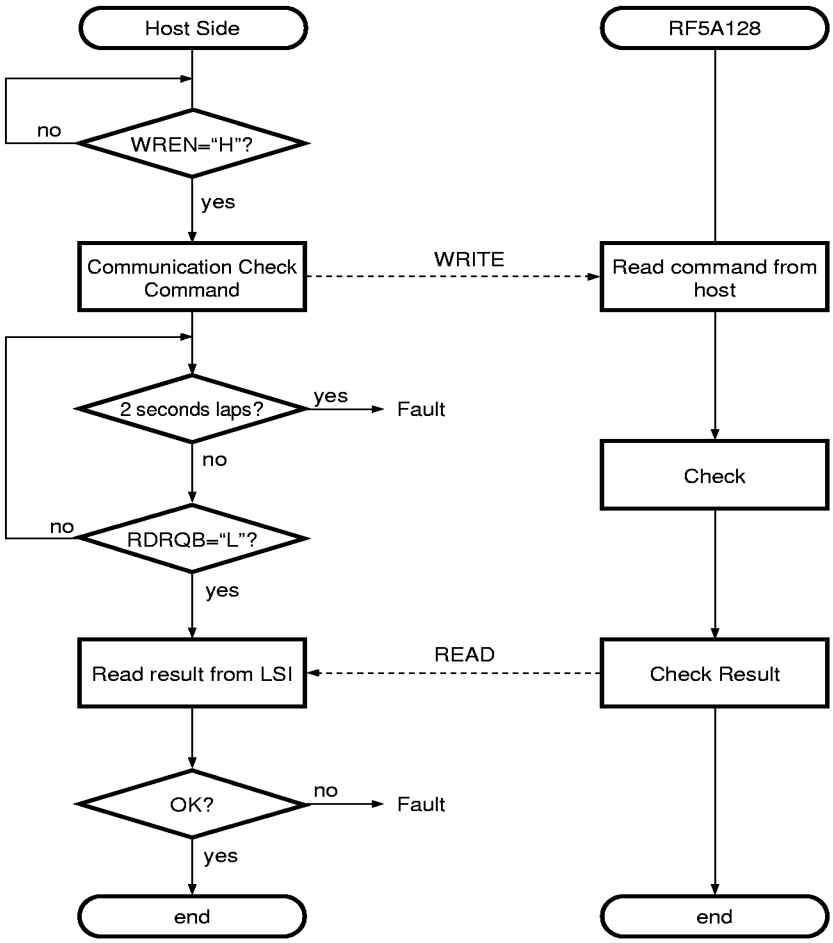
× : not used

Registration Result	
000	reserved
001	Word Number 1
010	Word Number 2
011	Word Number 3
100	Word Number 4
101	Word Number 5
110	Word Number 6
111	Word Number 7

Status		
Complete	0	NO
	1	YES
Capacity Error	0	NO
	1	YES
Other Errors	0	NO
	1	YES

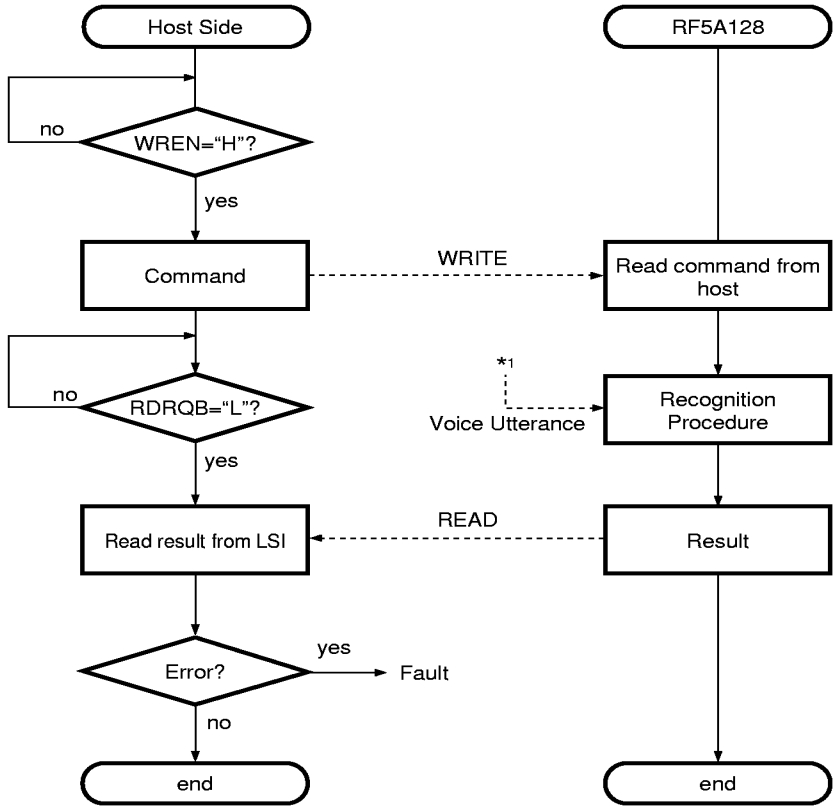
2.5 Control Flow Charts

2.5-1 Communication Check*1



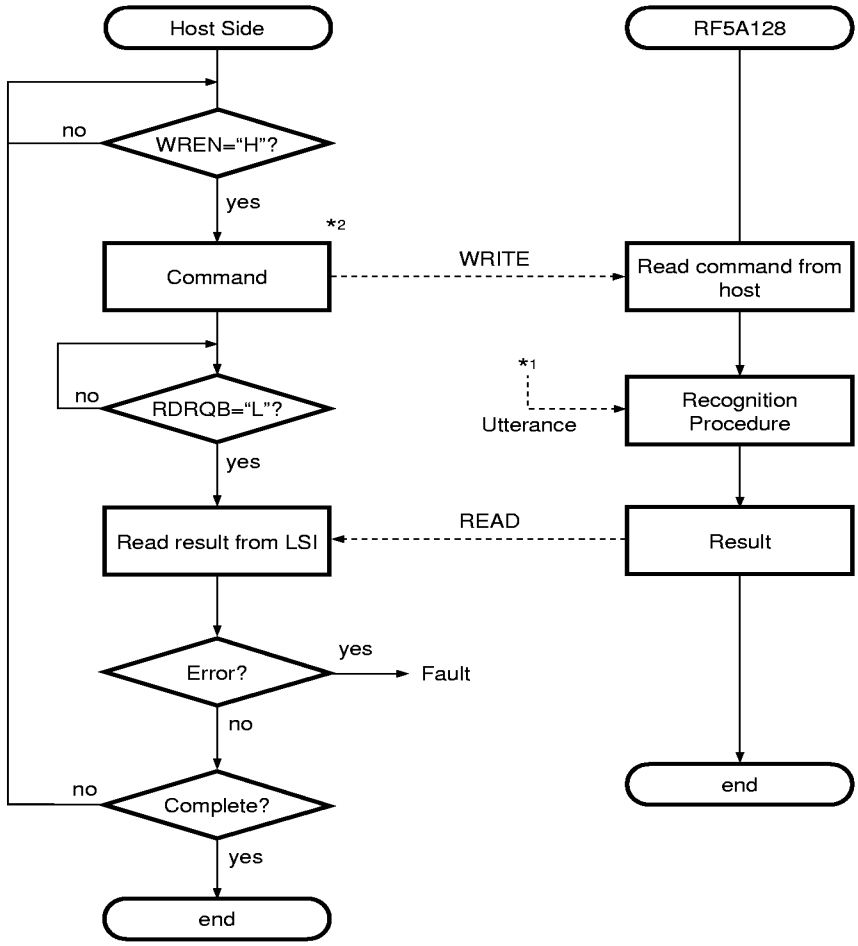
*1) Communication Check must be done at least 1 time after power on.

2.5-2 Recognition



*1) Usually the LSI requires 1utterance.
But 2 or more times of utterances can be required by the LSI because of voice or surrounding noise condition.

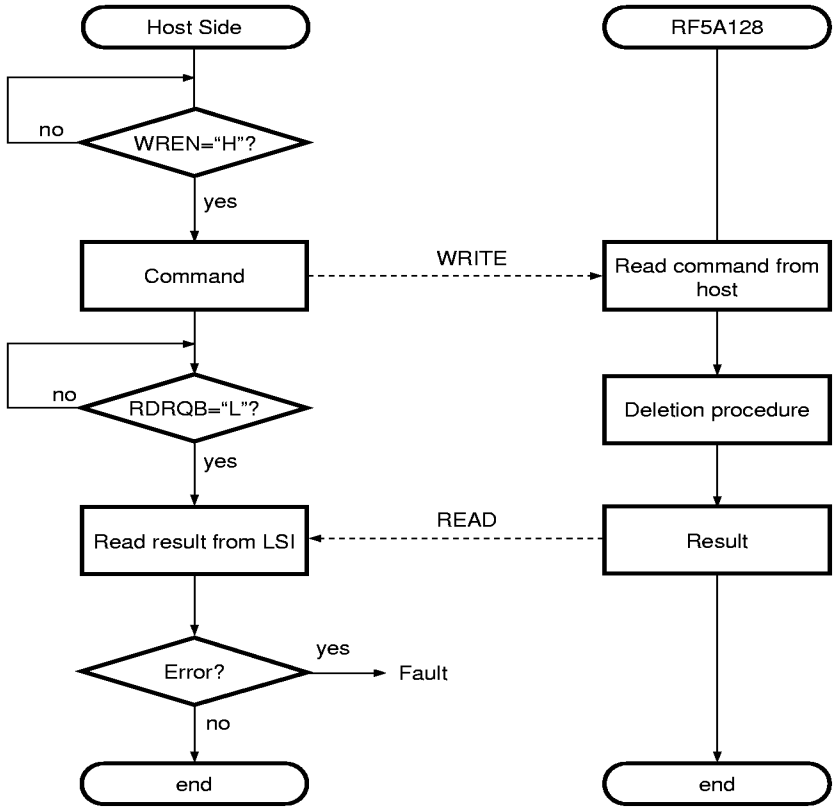
2.5-3 Registration



*1) Registration requires 3 times of utterance.
One registration command is necessary for every utterance.
But 4 or more times of utterances can be required by the LSI because of voice or surrounding noise condition.

*2) The control commands (words to register) must be the same each time.

2.5-4 Deletion



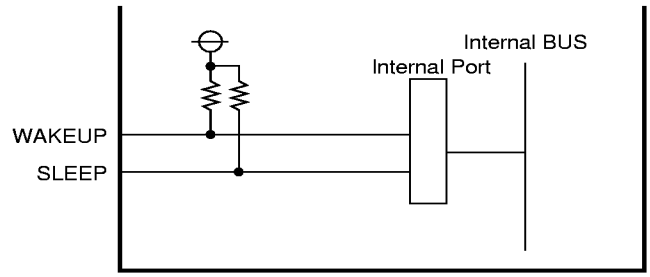
3. Sleep, Wakeup Function

To set the LSI to Stand-by mode, enter "L" pulse to the SLEEP pin. In this mode, the power consumption is minimized with internal Dependent-dictionary data being back up.

To resume the LSI to the normal mode, use the method listed below.

- Reset
- Enter "L" pulse to the WAKEUP pin.
- Write the DATA to the LSI (External Host mode).

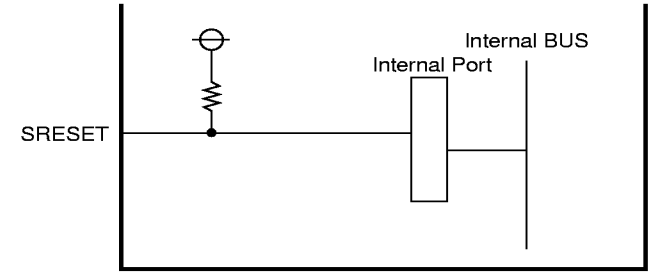
SLEEP and WAKEUP pins are internally pulled up.



4. Soft Reset Function

To reset the LSI to initial state (internal Dependent-dictionary is empty), enter "L" pulse to the SRESET pin.

SRESET is internally pulled up.

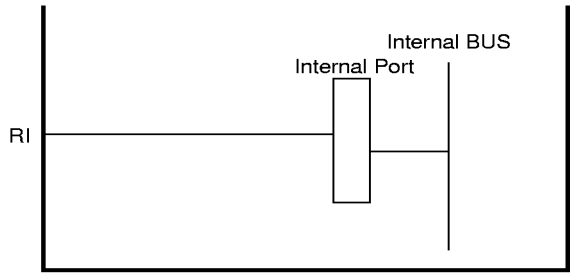


5. Reject Level Function

If the similarity of 1st candidate of recognition result is not high enough, the result should be REJECTED to avoid the error. And this threshold is called REJECT LEVEL.

To change the REJECT LEVEL, use RJ pin.

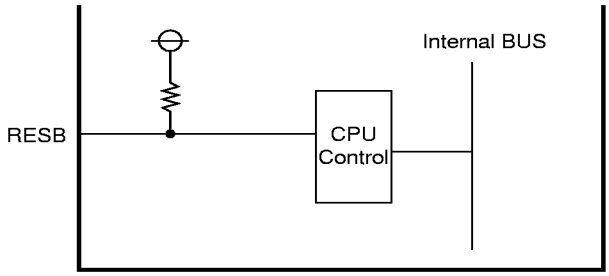
RJ pin	REJECT LEVEL	Recognition
"L"	0	Standard Level
"H"	1	Much rejected than Level "0"



6. Reset

When power on, to initiate the internal hardware and CPU, "L" level reset pulse is needed.
Reset pulse width should be longer than 2 micro seconds. (Clock 16MHz)

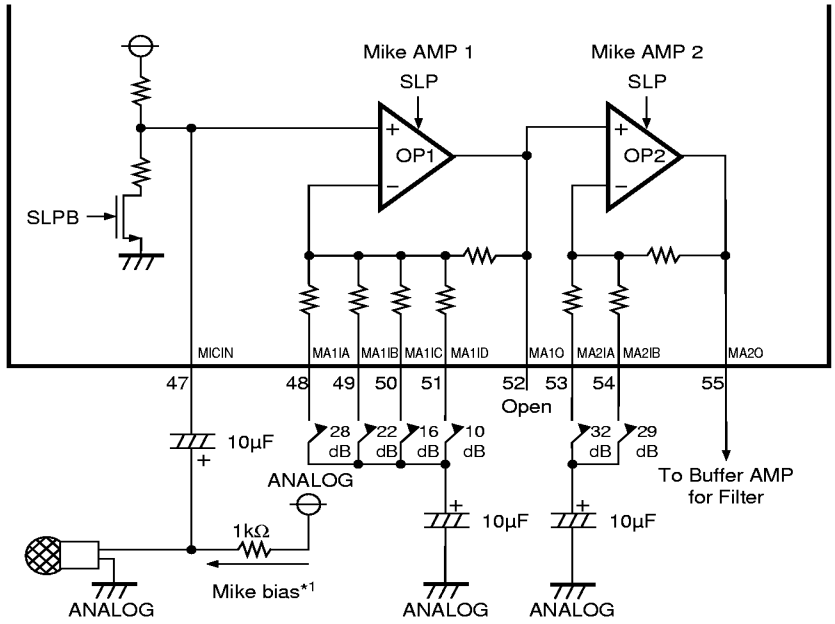
RESB is internally pulled up.



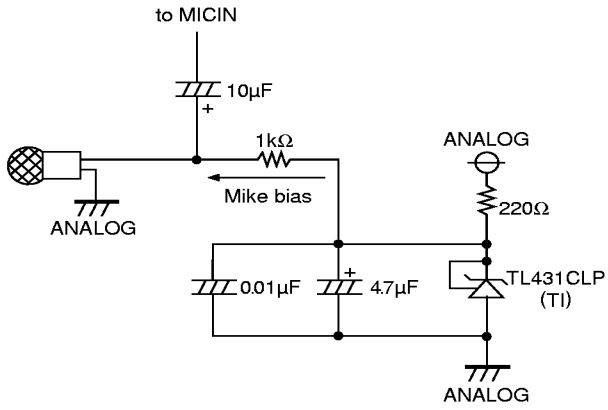
7. Voice Signal Pins

7.1 Mike AMP.

The Mike AMP consists of 2 stage non-inverting Operational Amplifiers.
The mike output should be connected via the AC coupling capacitor to the MICIN, to avoid the difference between the mike DC level and the internal DC reference level.
The gain of Mike AMP is set by choosing the pin that is connected to the ground.
The capacitor is necessary to reduce the DC offset.



*1) If using Electric Condenser Microphone, the DC bias is necessary.
And if the power source is very noisy or Mike gain is very high (over 50dB), Using regulator to this point is good to obtain better voice signal.



7.2 Combination of the Pins to Set the Mike Gain Level

The relation of gain and combination of the pins connected to the ground is listed below.
To obtain better results, the Voice signal voltage should be 1-4Vpp at the ADIN pin.
So, please choose the certain gain setting under the various conditions such as distance between mike and mouth or surrounding noise.
Changing gain or connecting/ disconnecting mike must be done while LSI's power off.

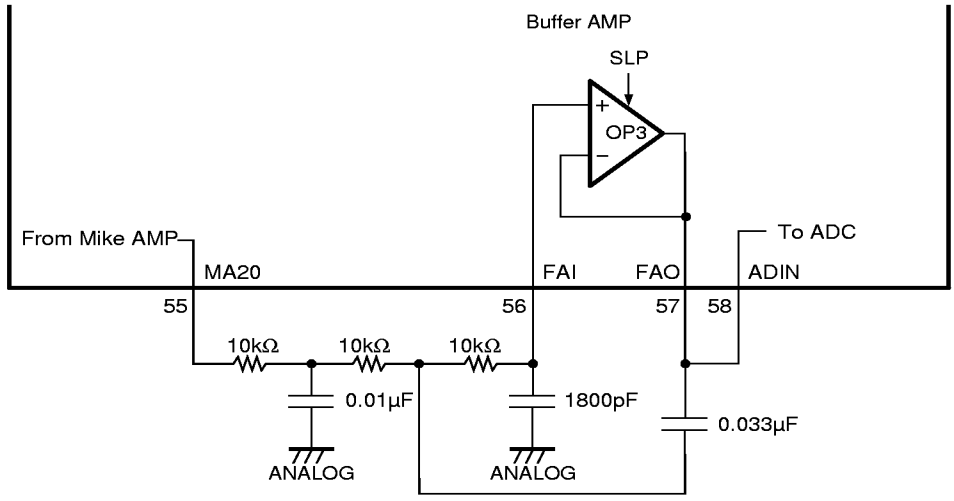
Mike AMP 1 / Mike AMP 2	MA1IA	MA1IB	MA1IC	MA1ID	no connection
MA2IA	60	54	48	42	32
MA2IB	57	51	45	39	29
No Connection	28	22	16	10	0

(dB)

For example, if 45dB of the gain is needed, MA1IC and MA2IB are connected to the ground, via the capacitor.

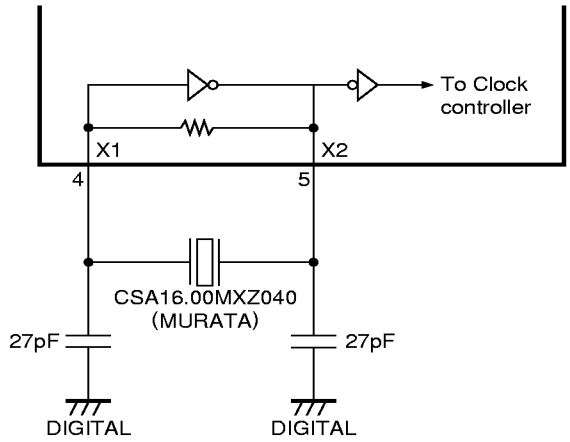
7.3 Buffer Amplifier (For Anti-alias Filter)

Buffer AMP for Anti-alias Filter is one voltage follower.
Shown below is an example of 3rd order Low pass Filter. The resistance or capacitance value are changeable due to other conditions.

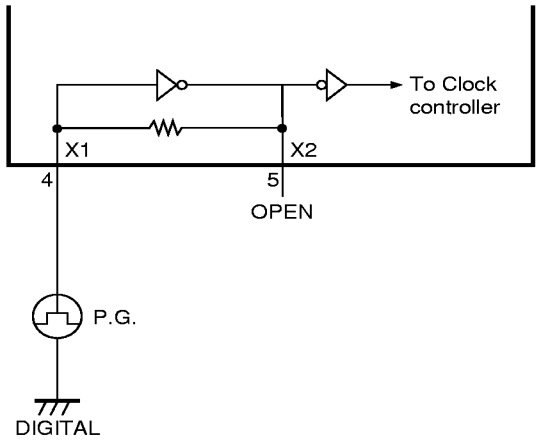


7.4 Clock Circuit

RF5A128/ 5S830 includes vibrator circuit suitable for both X'tal and ceramic vibrator.
It can work with connecting capacitors and vibrator to the X1, X2.
If using external oscillator, connect the signal to X1, and X2 opened.



(a) Internal circuit (16MHz)
[ceramic vibrator]



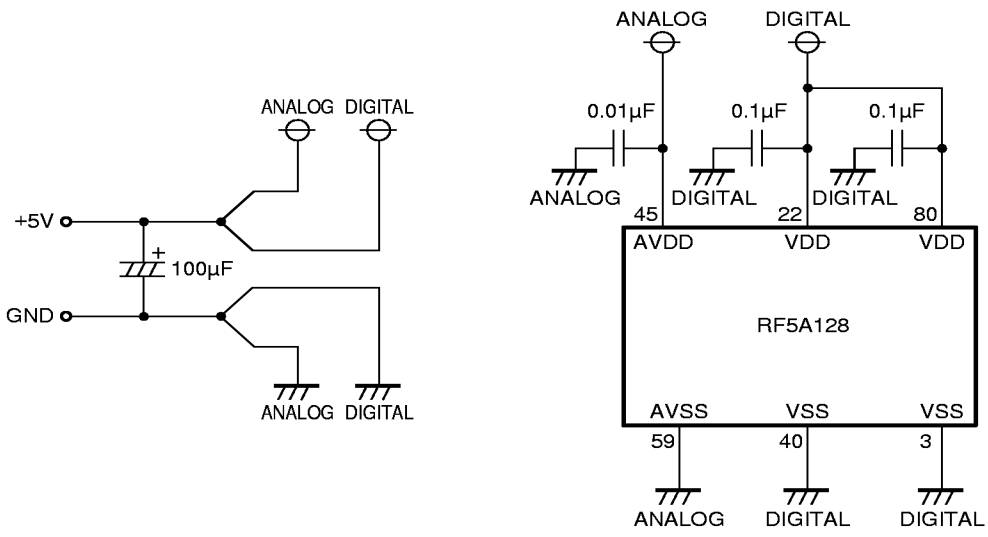
(a) External oscillator (16MHz)

7.5 Power Circuit

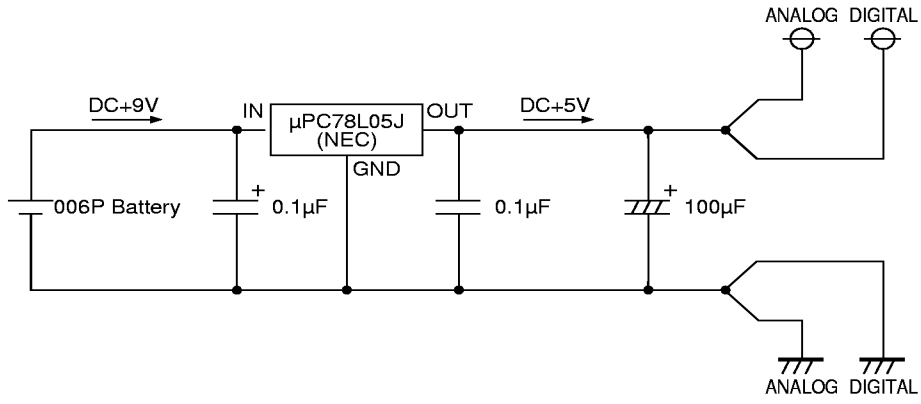
RF5A128/ 5S830 is Digital/ Analog hybrid LSI. So, the power line quality influences the efficiency of the LSI. The listed below are recommendations to obtain better result.

a. If using Switching regulator for the power source, please choose low ripple model.
b. Please divide analog power line and digital power line on the printed circuit board.
c. Please connect the each ground line at the one point.
And the point should be near the power line connector.
d. If using battery and voltage regulator IC, Please choose low ripple model.

Example :



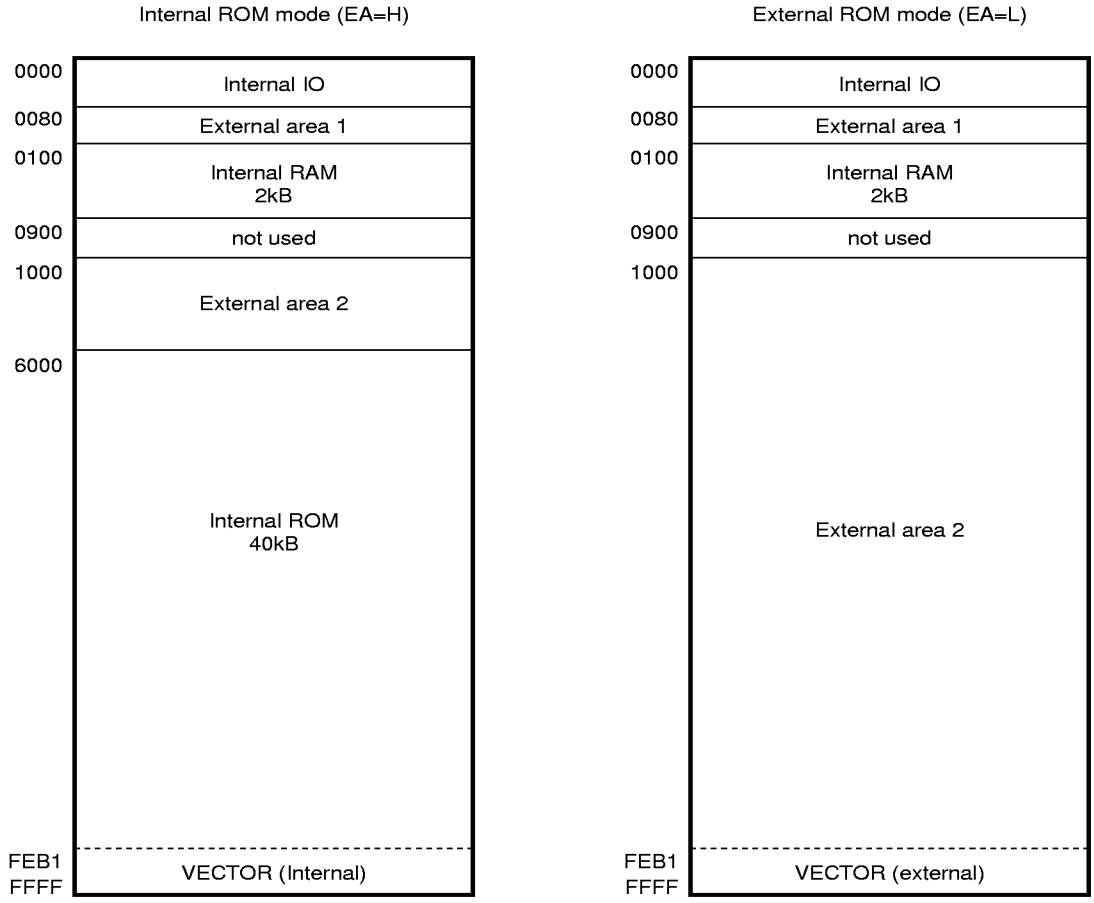
Example : 9V Battery with voltage regulator IC.



8. CPU Address space

8.1 From the view of hardware

External memories for dictionary or software can be connected to the "External area".



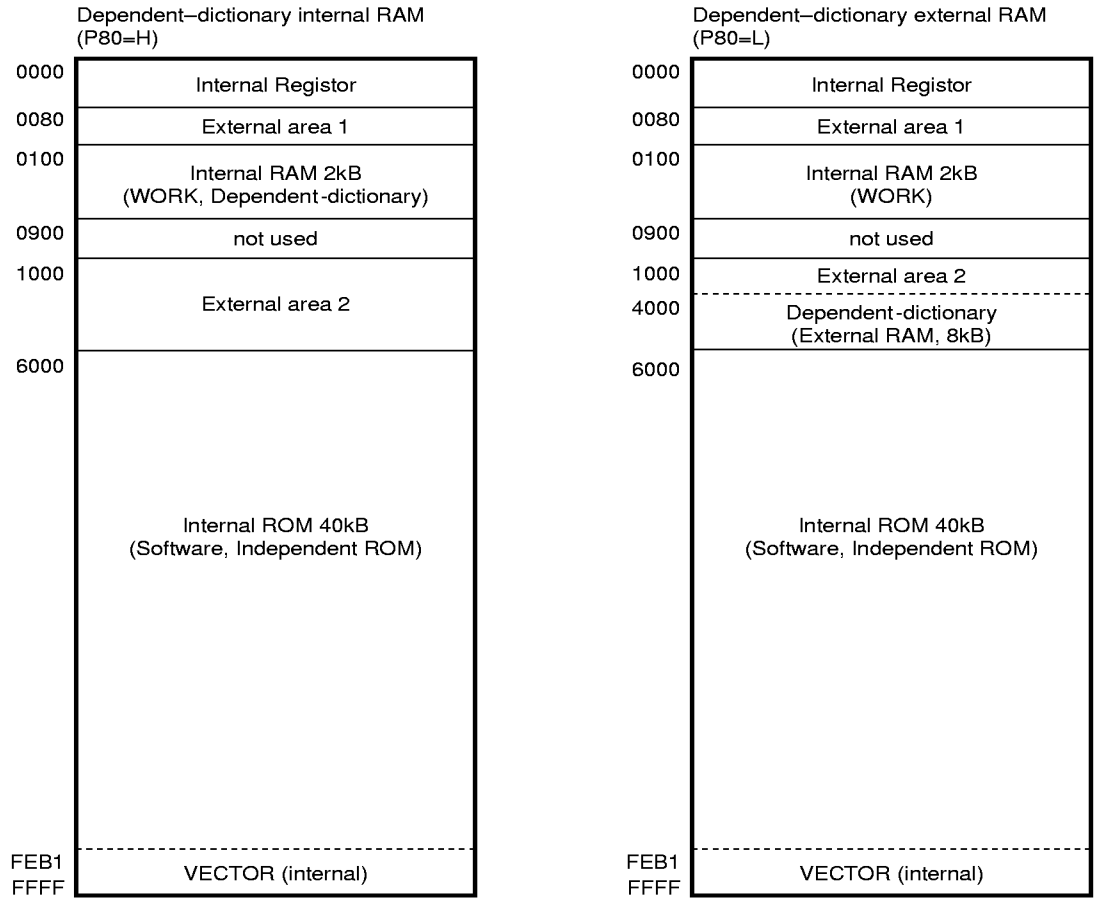
*) When accessing internal area, the output pulse of AD0 to 15, DB0 to 7 are "L", RDB, WRB are "H". These are activated when external area is accessed. (Both mode)

8.2 From the view of software

The area of dependent-dictionary can be allocated on either internal RAM or external RAM. To select this, change the level of P80. This level is referenced while reset state.

Internal : (P80=H) 700Byte, 3words (length total 2 seconds)

External : (P80=L) 8KByte, 7words (14 seconds) in this case, only 5Kbyte are used.



*) When accessing internal area, the output pulse of AD0 to 15, DB0 to 7 are "L", RDB, WRB are "H". These are activated when external area is accessed. (Both mode)

APPLICATION SOFTWARE

RF5A128/ 5S830 is a one chip micro computer from the construction view.
So, application software is available on the vacant memory space.
And also full customization of pin function/ usage is available.

1. List of Internal Registers

Register address	R/W	BLOCK	Symbol	Function
0C	R W	TIMER1	T1CNL	Current low-order value of the counter. Allows low-order setting of the counter.
0D	R W		T1CNH	Current high-order value of the counter. Allows high-order setting of the counter.
0E	W		T1RLL	Allows low-order setting of the reload register.
0F	W		T1RLH	Allows high-order setting of the reload register.
21	R W	WDT	TWCN	Current value of the counter. Allows setting of the counter.
22	R W	Common to all timers	TIMEN	Enabled or disabled condition value of each timer. Allows enabled or disabled condition setting of each timer.
23	W		TCLSL1	Allows selection of a clock source for the timer 1.
24	W		TCLSL2	Allows selection of a clock source for the WDT.
26	R W	Interrupt sensing (INT0 to INT3)	EXELS	Selected value for edge or level sensing. Allows edge or level sensing selection.
27	R W		EXIEG	Selected interrupt polarity value. Allows interrupt polarity setting.
30	R W	Interrupt servicing	IRENL	Interrupt enabled condition value of the INT0 to INT3 and the WDT. Allows interrupt enabled condition setting of the INT0 to INT3 and the WDT.
31	R W		IRENH	Interrupt enabled condition value of the timer 1. Allows interrupt enabled condition setting of the timer 1.
32	R W		IRSTL	Interrupt status of the INT0 to INT3 and the WDT. Allows interrupt resetting of the INT0 to INT3 and the WDT.
33	R W		IRSTH	Interrupt status of the timer 1. Allows interrupt resetting of the timer 1.
34	R W	ADC	ADMD	Mode status of the A/ D converter. Allows mode setting of the A/ D converter.
35	R W		ADDTL	Set value for A/ D conversion time (stored in bits 1 and 0). Allows A/ D conversion time setting.
36	R W		ADDTH	Set value for A/ D conversion time (stored in bits 9 to 2). Reserved.
37	R W		ADGA	Reserved. Allows threshold output setting of the A/ D converter.
3E	R W	External processor control mode	EXCT	Set value for external access control mode. Allows external access control mode setting.
3F	R W	CPU clock	PSCT	Set value for power saving control mode. Allows power saving control mode setting.

Register address	R/W	BLOCK	Symbol	Function
40	R W	Internal port 0*1	PD0	Input data. Output data.
41	W		PM0	Selects input/ output.
42	W		PP0	Selects pull-up (for INP0 to INP7).
43	R W	Internal port 1*2	PD1	Input data. Output data.
44	W		PM1	Selects input/ output.
45	W		PP1	Selects pull-up (for OUTP0 to OUTP7).
46	R W	Internal port 2*3	PD1	Input data. Reserved.
4E	R W	Internal port 7*4	PD7	Input data. Output data.
4F	W		PM7	Selects input/ output (only for P75, P76, and P77).
50	R W	Port 8	PD8	Input data. Output data.
51	W		PM8	Selects input/ output.
53	R W	Pin function	CBCT	Functional value of the port 8. Allows functional setting of the port 8.
54	R W	Multiplier/ divider	MDTEM	Status value of the multiplier and the divider. Allows multiplying term count setting.
55	W		MDSTA	Allows DMA start address setting.
56	W		MDMAL	Allows low-order multiplicand and divisor setting.
57	W		MDMAH	Allows high-order multiplicand and divisor setting.
58	W		MDMBL	Allows low-order multiplier setting.
59	W		MDMBH	Allows high-order multiplier setting.
5A	W		MDPSL	Allows low-order product sum multiplier setting.
5B	W		MDPSH	Allows high-order product sum multiplier setting.
5C	R W		MDRLL	Product (in bits 7 to 0) or low-order quotient. Allows dividend setting (in bits 7 to 0).
5D	R W		MDRLH	Product (in bits 15 to 8) or high-order quotient. Allows dividend setting (in bits 15 to 8).
5E	R W		MDRHL	Product (in bits 23 to 16) or low-order remainder . Allows dividend setting (in bits 23 to 16).
5F	R W		MDRHH	Product (in bits 31 to 24) or high-order remainder. Allows dividend setting (in bits 31 to 24).

*1) The internal port 0 is used for the following purposes:
Switch mode: Input/output to and from the INP0 to the INP7.
External processor control mode: Reading data (8bits) input (written) to the INP.

*2) The internal port 1 is used for the following purposes:
Switch mode: Input/output to and from the OUTP0 to the OUTP7.
External processor control mode: Reading data (8bits) output (read) from the INP.

*3) The internal port 2 is used for the following purposes:
P20/INT0: Reading the status of the WAKEUP interrupt input pin.
P21/INT1: Reading the status of the SLEEP interrupt input pin.
P22/INT2: Reading the status of the SRESET interrupt input pin.
P23/INT3: Reading the status of external write control signals (logical products of IOCSB and IOWRB) (in the external processor control mode).
P24: Reading the status of the IOMODE pin.
P25: Reading the status of the RJ pin.
P26 and P27: Unused.

*4) The internal port 7 is used as a port control register in the external processor control mode for the following purposes:
P70: Inputting an external read request status.
P71: Inputting an external write enable status.
P72: Outputting an external read request setting.
P73: Making an external write enable setting.
P74: Outputting an INP data direction setting.
P75: Input/output to and from the secondary port 0.
P76 Input/output to and from the secondary port 1
P77: Input/output to and from the secondary port 2.

2. Timers

The timers are available in two types: the 16bit reloadable timer (timer 1) and the 8bit watchdog timer (WDT).

2.1 Timer 1

The timer 1 is supplied with 1/ 1, 1/ 8, 1/ 32, or 1/ 128 of the system clock pulse, which can be selected by the settings of bits 3 and 2 in the timer 1 clock source selection register (TCLSL1 at address "23h") and whose cycle can be set in the range of 125ns to 1.04s when the X1 clock pulse has a cycle of 16MHz.
The timer 1 consists of the 16bit downward counter intended for both read and write operations and the 16bit reload registers intended for only writing operation.

The downward counter starts counting down from a value set in the counter setting registers (T1CNL (0Ch) and T1CNH (0Dh)). Upon setting of the downward counter to "1" , the next following count pulse causes loading of the contents of the reload registers (T1RLL at "0Eh" and T1RLH at "0Fh") to the timer 1 and output of an interrupt request to the interrupt controller. The timer 1 can read a current count value from the counter setting registers. Any count value written to the counter setting registers is set in the reload registers. Reading and writing operations should always be performed first on the low-order counter setting register and then on the high-order counter counter setting register. Similarly, writing operation should always be performed first on the low-order reload register and then on the high-order reload register.

*) In response to a word data transfer instruction, the CPU always makes read/write access first to the low-order registers and then to the high-order registers. At reset time, the downward counter is initialized to "FFFF" while the counter setting registers and the reload registers have indefinite states.

2.2 Watchdog Timer (WDT) (TWCN at "21h")

The watchdog timer (WDT) consists of the 8bit downward counter providing a means of recovering from abnormal loop execution due to program runaway. The downward counter is supplied with $1/2^{8}$, $1/2^{10}$, $1/2^{12}$, or $1/2^{14}$ of the system clock pulse, which can be selected by the settings of bits 7 and 6 in the timer clock source selection register (TCLSL2 at "24h") and whose cycle can be set to 4.1ms, 16ms, 66ms, and 262ms, respectively when the X1

clock pulse has a cycle of 16MHz. The WDT outputs an interrupt request to the interrupt controller upon switching the uppermost bit from "1" to "0" in the downward counter (when the reading of the downward counter is changed from "80h" to "7Fh") and is reset when "00" is set in the downward counter. Consequently, write operation should be performed on the WDT before "00" is set in the downward counter. The WDT is intended for both read and write operations. At read time, the WDT indicates the current reading of the downward counter. At write time, the WDT is reset to "FF" regardless of what data are written. At reset time, the WDT is also initialized to "FF".

2.3 Timer Enable Register (TIMEN at "22h")

The timer enable register (TIMEN at "22h") is used to enable or disable the timer 1 and the WDT. When set to "1", the counter corresponding to the each bit becomes active.

TIMEN [22h]

	7	6	5	4	3	2	1	0
BLOCK	WDT						Timer 1	
Bit name	TWEN						T1EN	
R/W	R/W							
Reset time	0							
Function	0 : Disables the timers. 1 : Enables the timers.							

2.4 Timer Clock Source Selection Registers (TCLSL1 at "23h" and TCLSL2 at "24h")

The timer clock source selection register (TCLSL1 at "23h") is used to select four types of the system clock pulses divided by the 8bit prescaler. The system clock pulse is equivalent to a divided-by-two clock pulse input from the X1 pin.

TCLSL1 [23h]

	7	6	5	4	3	2	1	0
BLOCK					Timer 1			
Bit name					T1CLK1	T1CLK0		
R/W	W							
Reset time	0							
Function	00 : 1/1 01 : 1/8 10 : 1/32 11 : 1/128							

TCLSL2 [24h]

	7	6	5	4	3	2	1	0
BLOCK	WDT							
Bit name	T1CLK1	T1CLK0						
R/W	W							
Reset time	0							
Function	00 : $1/2^{8}$ 01 : $1/2^{10}$ 10 : $1/2^{12}$ 11 : $1/2^{14}$							

3. External Interrupt Registers (EXELS at "26h" and EXIEG at "27h")

External interrupts are input from four pins (INT0 to INT3) and available in two modes (edge detection and level sensing). The edge detection mode permits selection of their rising and falling edges while the level sensing mode permits selection of their low and high levels. The edge detection mode and the level sensing mode can be selected by the D0 to D3 bits in the external interrupt register (EXELS at "26h"). A polarity for edge detection can be specified by the D0 to D3 bits in the external interrupt register (EXIEG at "27h").

EXELS [26h]

	7	6	5	4	3	2	1	0
BLOCK	External interrupt							
Bit name					INT3	INT2	INT1	INT0
R/W	R/W ("0" at read time)							
Reset time	0							
Function	0 : Specifies the edge detection mode. 1 : Specifies the level sensing mode.							

EXIEG [27h]

	7	6	5	4	3	2	1	0
BLOCK	External interrupt							
Bit name					INT3	INT2	INT1	INT0
R/W	R/W							
Reset time	0							
Function	Specifies a polarity for edge detection. 0 : Specifies the falling edge (edge detection mode) and the low level detection (level sensing mode). 1 : Specifies the rising edge (edge detection mode) and the high level detection (level sensing mode).							

*) 0 should be written in the bit 5 or bit 6 at write time.

External interrupts are input from the four pins below:

INT0 : WAKEUP
INT1 : SLEEP
INT2 : SRESET
INT3 : A negative logical products of the IOCSB and the IOWRB in the external processor control mode for use at rising edges in generating interrupts from external interrupt sources.

4. Interrupt Controller

The interrupt controller outputs interrupt requests (IRQs) to the CPU in response to the reset, NMI, TRAP, and BRK interrupts as well as four external interrupt sources and four internal interrupt sources.

4.1 Interrupt Vector Table

No.	Priority order	Address	Symbol	Interrupt source
1	High	1FFFCh	RESET	Reset
2	▲	1FFF9h	NMI	NMI
3		1FFF5h	TRAP	TRAP
4		1FFF1h	BRK	BRK
5		1FFEDh	EXINT0	External interrupt 0
6		1FFE9h	EXINT1	External interrupt 1
7		1FFE5h	EXINT2	External interrupt 2
8		1FFE1h	EXINT3	External interrupt 3
9		1FFDDh	ADINT	A/D conversion end interrupt
10				
11		1FFD5h	WDTINT	Watchdog timer interrupt
12				
13		1FFCDh	TM1INT	Timer 1 interrupt
14				
15				
16				
17				
18				
19	▼			
20	Low	1FFB1h	TINTB	Test interrupt

The individual interrupts to the CPU are cleared as follows: The external interrupts 0 to 3 (EXINT0 to EXINT3) (at vector numbers 5 to 8) are cleared by reading from the corresponding interrupt vectors and writing to the corresponding bits in the interrupt clear register (IRSTL at "32h"), the interrupt status register (IRSTH at "33h"), the external interrupt mode register (EXELS at "26h"), and the external interrupt polarity register (EXIEG at "27h"). The A/D conversion end interrupt (ADINT), the watchdog timer interrupt (WDTINT), and the timer 1 interrupt (TM1INT) (at vector numbers 9, 11, and 13, respectively) are cleared by reading from the corresponding interrupt vectors and writing to the corresponding bits in the interrupt clear register (IRSTL) and the interrupt status register (IRSTH). All the interrupts excluding the test interrupt (TINTB) can be masked by the settings of the interrupt enable registers (IRENL at "30h" and IRENH at "31h"). Note that the test interrupt (TINTB) is intended for only testing and not for application.

4.2 Interrupt Enable Register (IRENL at "30h" and IRENH at "31h")

The interrupt enable register (IRENL at "30h") is used to mask or enable the external interrupts 0 to 3 (EXINT0 to EXINT3), the A/D conversion end interrupt (ADINT), and the watchdog timer interrupt (WDTINT). Similarly, the interrupt enable register (IRENH at "31h") is used to mask or enable the timer 1 interrupt (TM1INT). These interrupts are enabled by setting the corresponding bits to "1" in the interrupt enable registers.

IRENL [30h]

	7	6	5	4	3	2	1	0
BLOCK	Interrupt							
Bit name		WDTIEN		ADIEN	EXI3EN	EXI2EN	EXI1EN	EXI0EN
R/W	R/W							
Reset time	0							
Function	0 : Masks interrupts. 1 : Enables interrupts.							

IRENH [31h]

	7	6	5	4	3	2	1	0
BLOCK	Interrupt							
Bit name								TM1IEN
R/W	R/W							
Reset time	0							
Function	0 : Masks interrupts. 1 : Enables interrupts.							

*) The undefined bits are always read as "0".

4.3 Interrupt Clear Register (IRSTL at "32h") and Interrupt Status Register (IRSTH at "33h")

The interrupt clear register (IRSTL at "32h") is used to specify generation of one-shot pulses for clearing interrupt requests upon setting the corresponding bits to "0" and performs no function upon setting them to "1".

At read time, the interrupt status register (IRSTH at "33h") indicates an interrupt status. Namely, it indicates interrupt enabled states upon setting the corresponding bits to "1". At write time, any bits corresponding to enabled interrupts in the interrupt status register are set to "1" regardless of the settings of the interrupt enable registers (IRENL at "30h" and IRENH at "31h").

IRSTL [32h]

	7	6	5	4	3	2	1	0
BLOCK	Interrupt							
Bit name		WDTIST		ADIST	EXI3ST	EXI2ST	EXI1ST	EXI0ST
R/W	R/W							
Reset time	0							
Function	At write time: 0 : Clears interrupt requests. 1 : Performs no function. At read time: 0 : Indicates absence of interrupts. 1 : Indicates presence of interrupts.							

	7	6	5	4	3	2	1	0
BLOCK	Interrupt							
IRSTH Bit name								TM1IST
[33h] R/W	R/W							
Reset time	0							
Function	At write time 0 : Clears interrupt requests. 1 : Performs no function. At read time 0 : Indicates absence of interrupts. 1 : Indicates presence of interrupts.							

5. External Access Control Register (EXCT at "3Eh")

In the external memory mode, the external access control register (EXCT at "3Eh") switches between the internal and external ROMs, indicates the presence or absence of the bus monitor during access to the internal ROM area, and specifies the number of waits during access to external areas.

	7	6	5	4	3	2	1	0
BLOCK	External memory mode							
EXCT Bit name	IE	MON				EW2	EW1	EW0
[3Eh] R/W	R/W							
Reset time	×	0				1	1	1
Function	0 : External ROM. 1 : Internal ROM.	0 : Bus monitor absence. 1 : Bus monitor presence.				External area 2 0 : 0 wait. 1 : 1 wait.	External area 1 00 : 0 wait. 01 : 1 wait. 10 : 2 wait. 11 : 3 wait.	

*) The undefined bits are always read as "0".

The initial value of the IE bit indicates the state of the EA pin during reset time (until the completion of start-up).

6. Power Saving Control Register (PSCT at "3Fh")

There are four power saving control modes as listed below :

- Variable clock mode : Selects clock rates between 1/8 and 1/32 of the system clock pulse.
- Sleep mode : Stops the operation of the CPU only.
- Digital stop mode : Stops the operation of crystal oscillator, the digital units, and the A/D converter, and keeps the operation of only the operational amplifiers.
- Full stop mode : Stops the operation of all units including the analog units.

The power saving control register (PSCT at "3Fh") is used to set the variable clock mode, the digital stop mode, and the full stop mode. The sleep mode can be set by the SLP instruction from the CPU.

6.1 Variable Clock Mode

In the variable clock mode, clock rates can be selected between 1/ 8 and 1/ 32 of the system clock pulse. Clock rates can be specified by the CK1 bit (bit 1) and the CK0 bit (bit 0) in the power saving control register (PSCT). This mode slows down overall operational speeds (including the speeds of the timers, the CPU, and A/ D converter).

6.2 Sleep Mode (Stand-by mode)

The sleep mode can be set by the SLP instruction from the CPU. This mode stops the operation of the CPU only and keeps the operation of the peripheral input/ output equipment (including the timers). The CPU can be returned to operation by external or internal interrupts or the NMI interrupt.

6.3 Digital or Full Stop Mode

In the digital or full stop mode, all operations including oscillation can be stopped by setting the STP bit (bit 3) to "1" in the power saving control register (PSCT). When the MOD bit (bit 4) is set to "1" in this register, however, the operational amplifiers (the microphone amplifier and the filter amplifier) are kept in operation (continues to be supplied with power).

Stopped units can be returned to operation by the reset interrupt, the NMI interrupt, or the external interrupts. Upon input of the NMI interrupt or the external interrupts in particular, the WDT will start operating to output the WDT interrupt, starting supply of clock pulses to the CPU and other units. For the WDT interrupt time, see "2. 2. Watchdog Timer (WDT) (TWCN at "21h")".

Setting the digital or full stop mode requires setting the WDT interrupt time and setting external interrupt pins, if any, in edge-triggered states in advance.

When stopped units are returned to operation by the NMI interrupt or the external interrupts, their conditions prevailing prior to their stopped states are fully preserved.

Upon input of the reset interrupt to return stopped units to operation, however, the WDT will not start operating. Consequently, the reset pins should be held low for a sufficient time period to stabilize oscillation.

When stopped units are returned to operation by the reset interrupt, all the registers excluding the internal RAM are initialized.

		7	6	5	4	3	2	1	0
	BLOCK	Clock pulse to CPU							
PSCT	Bit name	0	0	0	MOD	STP	0	CK1	CK0
[3Fh]	R/W	R/W							
	Reset time	0							
	Function				Stop mode 0 : The full stop mode 1: The digital stop mode	Stop mode 1 : Stop		Clock rate selection 0 : Normal clock 10 : 1/8 of the system clock 11:1/32 of the system clock	

*) The undefined bits are always read as "0".

At write time, the power saving control register should have bits 2, 5, 6, and 7 set to "0" without exception. At read time, it indicates current bit settings.

Note that setting the STP bit to "1" will not stop any operation during the progress of A/D conversion, which, in turn, leads to the progress of program execution.

7. Internal Ports

The internal ports 0, 1, 2, 7, and 8 are used to exert indirect control over the 29 external ports (INP0 to INP7, P80 to P87, WAKEUP, SLEEP, SRESET, IOMODE, and RJ) performing varying functions depending on the control mode.

• Functions of Internal Ports

P00 to P07 : Read data input to the INP0 to the INP7 (externally written data). (8bit ports)

P10 to P17 : Write output data to the INP0 to the INP7 (externally read data). (8bit ports)

P70 : Reads the state of the IORDRQB and requests external reading at the low level.

P71 : Reads the state of the IOWREN and requests external writing at the high level.

P72 : Sets the IORDRQB to TRUE (the low level) when subjected to the positive pulse (causing transition from 0 to 1 and then to 0). Keep this bit at "0" in any other case (for the SR flip-flop).

P73 : Sets the IOWREN to TRUE (the high level) when subjected to the positive pulse (causing transition from 0 to 1 and then to 0). Keep this bit at "0" in any other case (for the SR flip-flop).

P74 : Forces the INP0 to the INP7 into the output mode when set to the positive value ("1"). Sets them to the output mode only at external read time (I.D. the IOCSB ∩ the IORDB) in response to external control signals in any other case.

P75 to P77 : Correspond to the OUTP5 to the OUTP7 and function as general-purpose input/output ports.

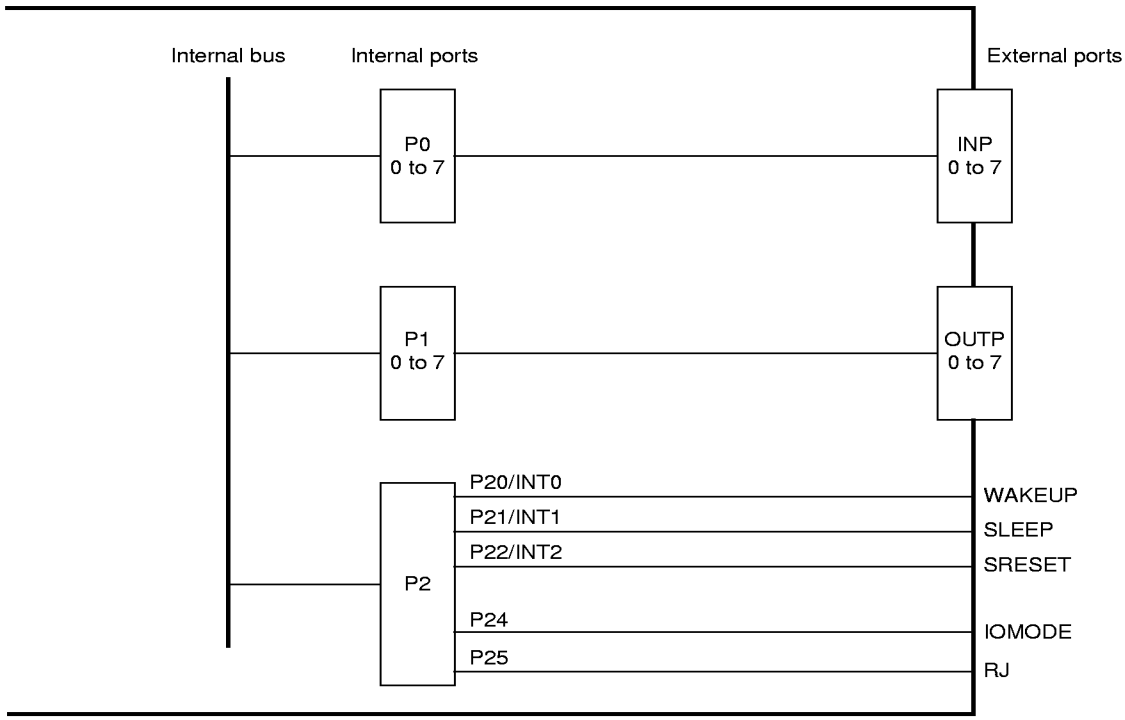
P23 : Reads the states of external control signals (I.D. the IOCSB ∩ the IOWRB) and generates the external interrupt 3 (INT3) from interrupt sources at rising edges.

• **Switch Modes**

7.1 Correspondence between Internal and External Ports (in Switch Mode)

External ports	Internal ports	Function	Main application
INP0 to INP7	P00 to P07	General-purpose input/ output	Switch input
OUTP to OUTP7	P10 to P17	General-purpose input/ output	Result output
WAKEUP	P20	Input/ INT0	Wake-up interrupt
SLEEP	P21	Input/ INT1	Stop interrupt
SRESET	P22	Input/ INT2	Soft reset interrupt
IOMODE	P24	Input	Control mode setting
RJ	P25	Input	Reject level setting
P80 to P87	P80 to P87	General-purpose input/ output	General-purpose input/ output

7.2 Internal Port Connection Diagram (in Switch Mode)



7.3 Internal Port Control Register (in Switch Mode)

7.3-1 Port 0 (PD0 at "40h", PM0 at "41h", and PP0 at "42h")
Port 1 (PD1 at "43h", PM1 at "44h", and PP1 at "45h")

The port 0 and the port 1 are switchable between input/ output operations in units of bits. The INPs and the OUTPs are 8bit input/ output pins each with soft pull-up which can be turned on and off in units of bits.

7.3-2 Data Registers (PD0 at "40h" for Port 0 and PD1 at "43h" for Port 1)

The data registers (PD0 at "40h" and PD1 at "43h") are used to set output data at write time and indicates the levels of the individual pins at read time.

		7	6	5	4	3	2	1	0
PD0[40h] PD1[43h]	BLOCK	Ports 0 and 1							
	Bit name	PD07	PD06	PD05	PD04	PD03	PD02	PD01	PD00
		PD17	PD16	PD15	PD14	PD13	PD12	PD11	PD10
	R/ W	R/ W							
	Setting at Reset time	Indefinite output data							

7.3-3 Input/output Selection Registers (PM0 at "41h" for Port 0 and PM1 at "44h" for Port 1)

		7	6	5	4	3	2	1	0
PM0[41h] PM1[44h]	BLOCK	Ports 0 and 1							
	Bit name	PM07	PM06	PM05	PM04	PM03	PM02	PM01	PM00
		PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10
	R/ W	W							
	Setting at Reset time	O							
	Function	0 : Input 1 : Output							

7.3-4 Pull-up Selection Register (PP0 at "42h" for INP and PP1 at "45h" for OUTP)

		7	6	5	4	3	2	1	0
	BLOCK	Ports 0 and 1							
PP0[42h] PP1[45h]	Bit name	PP07	PP06	PP05	PP04	PP03	PP02	PP01	PP00
		PP17	PP16	PP15	PP14	PP13	PP12	PP11	PP10
	R/W	W							
	Setting at Reset time	O							
	Function	0 : Turns off pull-up. 1 : Turns on pull-up.							

7.3-5 Port 2 (PD2 at "46h") (in Switch Mode)

The port 2 is an input port with six pins (P20 to P25). These pins have the following functions:

P20/ INT0 : Input port/ external interrupt 0
P21/ INT1 : Input port/ external interrupt 1
P22/ INT2 : Input port/ external interrupt 2
P23 : Unusable
P24 : IOMODE pin monitoring (unusable for any other application)
P25 : Input port

The data register (PD2 at "46h") is used to read data input to the port 2.

7.3-6 Data Register (PD2 at "46h")

The data register (PD2 at "46h") indicates the levels of the pins P20 to P25 at read time. These pins correspond to the external port pins as follows:

P20 WAKEUP
P21 SLEEP
P22 SRESET
P24 IOMODE
P25 RJ

		7	6	5	4	3	2	1	0
	BLOCK	Port 2							
PD2 [46h]	Bit name	0	0	P25	P24	1	P22	P21	P20
	R/W	R							
	Setting at reset time	—							

7.3-7 Port 8 (PD8 at "50h" and PM8 at "51h") (in Switch Mode)

The port 8 is a 8bit input/ output port. It serves the dual functions as the 8bit input/ output pin and the RDYB or NMIB pin.

The functions of the port 8 can be selected by the CPU bus input/ output selection register (CBCT at "53h").

The data register (PD8 at "50h") is used to set output data from the port 8 and read data input to the port 8.

The input/ output selection register (PM8 at "51h") is used to switch the port 8 between input and output operations.

7.3-8 Data Register (PD8 at "50h")

The data register (PD8 at "50h") is used to set output data at write time and indicates the levels of the individual pins at read time.

PD8[50h]

	7	6	5	4	3	2	1	0
BLOCK	Port8							
	PD87	PD86	PD85	PD84	PD83	PD82	PD81	PD80
R/ W	R/ W							
Setting at Reset time	Indefinite							
Function	At write time : Sets output data. At read time : Reads input data.							

7.3-9 Input/output Selection Register (PM8 at "51h")

PM8[51h]

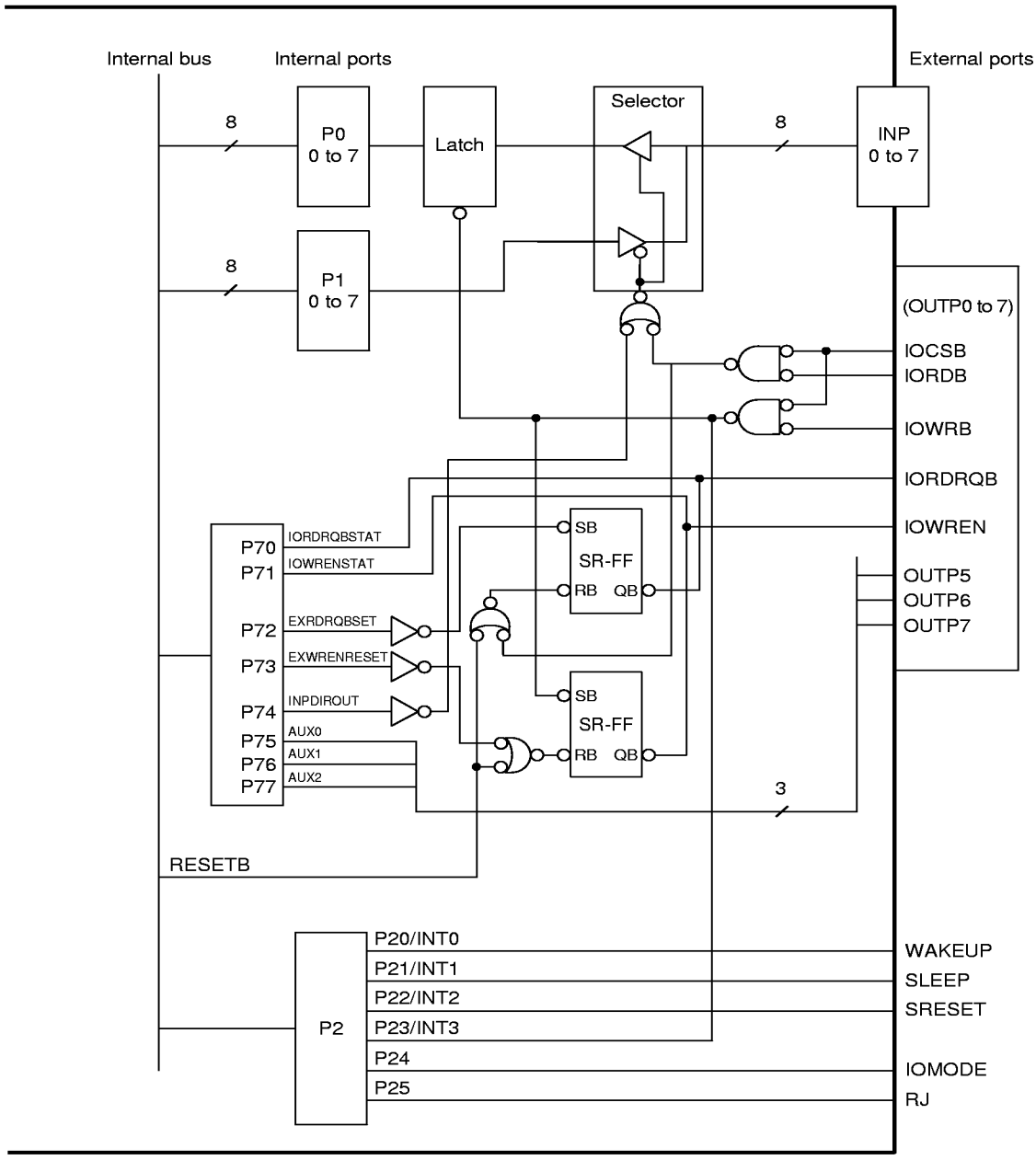
	7	6	5	4	3	2	1	0
BLOCK	Port8							
	PM87	PM86	PM85	PM84	PM83	PM82	PM81	PM80
R/ W	W							
Setting at Reset time	"00" (All input)							
Function	0 : Selects input. 1 : Selects output.							

• **External Processor Control Mode**

7.4 Correspondence between Internal and External Ports in External Processor Control Mode

External ports	Internal ports	Function	Main application
INP0 to INP7	P00 to P07/ P10 to P17	Bidirectional data bus	Command/ data transmission/ reception
OUTP to OUTP7	P70 to P77/ P23	Bus control input/ output	Read/ write control and write interrupt
WAKEUP	P20	Input/ INT0	Wake-up interrupt
SLEEP	P21	Input/ INT1	Stop interrupt
SRESET	P22	Input/ INT2	Soft reset interrupt
IOMODE	P24	Input	Control mode setting
RJ	P25	Input	Reject level setting
P80 to P87	P80 to P87	Geral-purpose input/ output	General-purpose input/ output

7.5 Internal Port Connection Diagram (in External Processor Control Mode)



7.6 Internal Port Control Register (in External Processor Control Mode)

7.6-1 Port 0 (PD0 at "40h" and PP0 at "42h")
Port 1 (PD1 at "43h" and PP1 at "45h")

The port 0 and the port 1 are fixed at input and output operations, respectively. The INPs and the OUTPs are 8bit input/ output pins each with soft pull-up which can be turned on and off in units of bits.

7.6-2 Data Registers (PD0 at "40h" for Port 0 and PD1 at "43h" for Port 1)

The data registers (PD0 at "40h" and PD1 at "43h") are used to set output data at write time and indicates the levels of the individual pins at read time.

		7	6	5	4	3	2	1	0
	BLOCK	Ports 0 and 1							
PD0[40h]	Bit name	PD07	PD06	PD05	PD04	PD03	PD02	PD01	PD00
PD1[43h]		PD17	PD16	PD15	PD14	PD13	PD12	PD11	PD10
	R/W	R (P0) / W (P1)							
	Setting at Reset time	Indefinite output data							

7.6-3 Pull-up Selection Register (PP0 at "42h" for INP and PP1 at "45h" for OUTP)

		7	6	5	4	3	2	1	0
	BLOCK	Ports 0 and 1							
PP0[42h]	Bit name	PP07	PP06	PP05	PP04	PP03	PP02	PP01	PP00
PP1[45h]		PP17	PP16	PP15	PP14	PP13	PP12	PP11	PP10
	R/W	W							
	Setting at Reset time	O							
	Function	0 : Turns off pull-up.			1 : Turns on pull-up.				

7.6-4 Port 2 (PD2 at "46h") (in External Processor Control Mode)

The port 2 is an input port with six pins (P20 to P25). These pins have the following functions:

P20 / INT0 : Input port/ external interrupt 0
P21 / INT1 : Input port/ external interrupt 1
P22 / INT2 : Input port/ external interrupt 2
P23 / INT3 : Externally written signal monitoring / external interrupt 3
P24 : IOMODE pin monitoring (unusable for any other application)
P25 : Input port

The data register (PD2 at "46h") is used to read data input to the port 2.

7.6-5 Data Register (PD2 at "46h")

The data register (PD2 at "46h") indicates the levels of the pins P20 to P25 at read time. These pins correspond to the external port pins as follows:

P20 WAKEUP
P21 SLEEP
P22 SRESET
P23 Externally written control signal monitoring (when the IOCSB the IOWRB)
P24 IOMODE
P25 RJ

		7	6	5	4	3	2	1	0
PD2 [46h]	BLOCK	Port 2							
	Bit name	0	0	P25	P24	P23	P22	P21	P20
	R/W	R							
	Setting at reset time	—							

7.6-6 Port 7 (PD7 at "4Eh" and PM7 at "4Fh") and Port 8 (PD8 at "50h" and PM8 at "51h") (in External Host Mode)

The ports 7 and 8 are 8bit input/ output ports. The port 7 functions as a control line port while the port 8 serves the dual functions as the 8bit input/ output pin and the RDYB or NMIB pin.

The functions of the port 8 can be selected by the CPU bus input/ output selection register (CBCT at "53h").

The data registers (PD7 at "4Eh" and PD8 at "50h") are used to set output data from the ports 7 and 8 and read data input to the ports 7 and 8.

The input/ output selection registers (PM7 at "4Fh" and PM8 at "51h") are used to switch the ports 7 and 8 between input and output operations.

7.6-7 Data Register (PD7 at "4Eh" and PD8 at "50h")

The data registers (PD7 at "4Eh" and PD8 at "50h") are used to set output data at write time and indicate the levels of the individual pins at read time.

		7	6	5	4	3	2	1	0
	BLOCK	Ports 7 and 8							
PD7[4Eh]		PD77	PD76	PD75	PD74 (W)	PD73 (W)	PD72 (W)	PD71 (R)	PD70 (R)
PD8 [50h]		PD87	PD86	PD85	PD84	PD83	PD82	PD81	PD80
	R/ W	R/ W (or either one indicated in each parenthesis)							
	Setting at Reset time	Indefinite							
	Function	At write time : Sets output data. At read time : Reads input data.							

*) (W) : Write only, (R) : Read only

7.6-8 Input/output Selection Register (PM7 at "4Fh" and PM8 at "51h")

		7	6	5	4	3	2	1	0
	BLOCK	Ports 7 and 8							
PM7[4Fh]		PM77	PM76	PM75					
PM8 [50h]		PM87	PM86	PM85	PM84	PM83	PM82	PM81	PM80
	R/ W	W							
	Setting at Reset time	"00" (Input)							
	Function	0 : Selects input. 1 : Selects output.							

8. Pin Function Control Register (CBCT at "53h")

The pin function control register (CBCT at "53h") is used to specify the functions of the pins P83 and P86.

8.1 Pin Function Control Register (CBCT at "53h")

		7	6	5	4	3	2	1	0
	BLOCK	Pin function							
CBCT	Bit name	—	NMI	RDY	—	—	—	—	—
[53h]	R/W	R/W							
	Reset time		0	0					
	Function		0 : P86 pin. 1 : NMIB pin.	0 : P83 pin. 1 : RDYB pin.					

*) The undefined bits are always read as "0".

The NMIB and RDYB pins are internally held high when functioning as the input ports.

9. Multiplier/Divider

The multiplier/ divider provides three multiplication modes and one division mode as listed below:

- Single multiplication mode : $16 \times 16 = 32$ bits (Signed)
- Product sum operation mode : $16 \times 16 + 32 = 32$ bits (Signed)
- Memory table product sum operation mode : $\underbrace{16 \times 16 + 16 \times 16 + \cdots + 16 \times 16}_{\text{Maximum of 15 terms}} = 32$ bits (Signed)
- Division mode : $32 \div 16 = 16 \cdots 16$ bits (Unsigned)

9.1 Single Multiplication Mode

In the single multiplication mode, the multiplier/ divider performs multiplying operation only once.

The multiplier/ divider starts multiplying operation upon writing multiplicand data to the low-order and high-order multiplicand registers (MDMAL at "56h" and MDMAH at "57h") and then writing multiplier data to the low-order and high-order multiplier registers (MDMBL at "58h" and MDMBH at "59h"). After the interval of the 4 system clock pulses (each one of which is equivalent to a divided-by-two clock pulse input from the X1 pin), the multiplier/ divider sets the result of multiplying operation in the low-order and high-order operation result registers (MDRLL at "5Ch", MDRLH at "5Dh", MDRHL at "5Eh", and MDRHH at "5Fh"). The multiplier/ divider then resets the OF flag (bit 6) to "0" in the status register (MDTEM at "54h").

Write operation must always be performed first on the low-order and high-order multiplicand registers and then on the low-order and high-order multiplier registers in this order.

*) In response to a word data transfer instruction, the CPU always makes read/write access first to the low-order registers and then to the high-order registers.

During the progress of multiplying operation, the ACT flag (bit 7) is kept at "1" in the status register.

When reading the operation result registers before the completion of multiplying operation, the CPU remains in the wait state until the completion of multiplying operation. In this event, therefore, the CPU can always obtain the correct result of multiplying operation by reading the operation result registers immediately after the settings of the multiplier registers.

Multiplicand		Multiplier		Product
MDMA	×	MDMB	→	MDR
16 bits		16 bits		32 bits

9.2 Product Sum Operation Mode

In the product sum operation mode, the multiplier/ divider performs multiplying and adding operations once each.

The multiplier/ divider starts multiplying operation upon writing multiplicand data to the low-order and high-order multiplicand registers (MDMAL at "56h" and MDMAH at "57h") and then writing multiplier data to the low-order and high-order product sum multiplier registers (MDPSL at "5Ah" and MDPSH at "5Bh"). After the interval of the 5 system clock pulses, the multiplier/ divider adds the result of multiplying operation to the previous result of multiplying operation (overwrite-protected) preset in the low-order and high-order operation result registers (MDRLL at "5Ch", MDRLH at "5Dh", MDRHL at "5Eh", and MDRHH at "5Fh") to set the resulting sum in the operation result registers. The multiplier/ divider then sets the OF flag (bit 6) to "1" in the status register (MDTEM at "54h") if any overflow occurs as a result of adding operation or if the OF flag is set to "0" before the start of product sum operation.

Write operation must always be performed first on the low-order and high-order multiplicand registers and then on the low-order and high-order product sum multiplier registers in this order.

*In response to a word data transfer instruction, the CPU always makes read/ write access first to the low-order registers and then to the high-order registers.

During the progress of product sum operation, the ACT flag (bit 7) is kept at "1" in the status register.

When reading the operation result registers before the completion of product sum operation, the CPU remains in the wait state until the completion of product sum operation. In this event, therefore, the CPU can always obtain the correct result of product sum operation by reading the operation result registers immediately after the settings of the product sum multiplier registers.

MDMA	×	MDPS	+	MDR	→	MDR
16 bits		16 bits		32 bits		32 bits

In the single multiplication mode or the product sum operation mode, the settings of the multiplicand registers are retained after the completion of the initial round of multiplying operation or product sum operation and can therefore be reused for the subsequent rounds only by changing the settings of the multiplier registers or the product sum multiplier registers. Further, the settings of the multiplicand registers can also be updated before the completion of multiplying or product sum operation.

9.3 Memory Table Product Sum Operation Mode

In the memory table product sum operation mode, the multiplier/ divider performs product sum operation several times (once to 15 times).

The multiplier/ divider receives multiplicand and multiplier data which are transferred through direct memory access (DMA) from the internal RAM area specified by the start address register (MDSTA at "55h").

The multiplier/ divider starts product sum operation upon writing the desired number of product terms (1 to 15) and the high-order address ("1" to "3") of the internal RAM area storing multiplier data to the product term count register (MDTEM at "54h") and then writing multiplicand data and the low-order address ("00h" to "F0h") of the internal RAM to the start address register. After the interval of 6 times the specified number of product terms plus the 3 system clock pulses, the multiplier/ divider sets the result of product sum operation in the low-order and high-order operation result registers (MDRLL at "5Ch", MDRLH at "5Dh", MDRHL at "5Eh", and MDRHH at "5Fh").

In the memory table product sum operation mode, DMA restricts the CPU in such a manner as to run in a cycle equivalent to the number of product terms times two plus three during the progress of product sum operation.

In the memory table product sum operation mode, the setting of the product term count register is retained after the completion of the initial round of product sum operation and can therefore be reused for the subsequent rounds only by changing the setting of the start address register.

During the progress of product sum operation, the ACT flag (bit 7) is kept at "1" in the status register (MDTEM at "54h"). Upon occurrence of any one overflow during the progress of product sum operation, the OF flag (bit 6) is set to "1" in the status register; otherwise, it is set to "0".

For example, when the desired number of product terms is specified as "3" :

[STA + 1]	[STA]	×	[STA + 3]	[STA + 2]	→	MDR (1)	
[STA + 5]	[STA + 4]	×	[STA + 7]	[STA + 6]	+	MDR (1) →	MDR (2)
[STA + 9]	[STA + 8]	×	[STA + 11]	[STA + 10]	+	MDR (2) →	MDR

(The "STA" stands for data stored at the address specified by the start address register.)

In the above example, the multiplier/ divider completes a product sum operation after the interval of the 21 system clock pulses ($6 \times 3 + 3$) while the CPU runs in 9 cycles ($3 \times 2 + 3$).

9.4 Product Term Count/Status Register (MDTEM at "54h")

At write time, the product term count/ status register (MDTEM at "54h") functions as the product term count register to specify the number of product terms for use in the memory table product sum mode, specify the high-order address of the internal RAM area from which multiplicand and multiplier data are to be transferred through DMA, and control forced completion of product sum operation. Setting the four low-order bits to "0" in the product term count register performs no function. Similarly, setting the STP bit (bit 7) to "0" in the product term count register stops product sum operations in the memory table product sum mode after the interval of, at most, the 5 system clock pulses.

At read time, the product term count/ status register functions as the status register to indicate the progress of product sum operation or the occurrence of overflow.

9.5 Product Term Count Register (MDTEM at "54h")

		7	6	5	4	3	2	1	0
	BLOCK	Multiplication and division							
MDTEM	Bit name	STP	—	A9	A8	T3	T2	T1	T0
[54h]	R/ W	W							
	Setting at Reset time	Indefinite							
	Function	Completion		High-order address of internal RAM area		Desired number of product terms			
		0 : Specifies forced completion of product sum operation in the memory table product sum operation mode.		00 : Unused. 01 : "0100h" to "01FFh" 10 : "0200h" to "02FFh" 11 : "0300h" to "03FFh"		0001 : Specifies "1" 0010 : Specifies "2" 1111 : Specifies "15"			

9.6 Status Register (MDTEM at "54h")

		7	6	5	4	3	2	1	0
	BLOCK	Multiplication and division							
MDTEM	Bit name	ACT	OF	0	0	0	0	0	0
[54h]	R/W	R							
	Setting at Reset time			0					
	Function	1:The progress of product sum operation.	1:The occurrence of overflow.						

9.7 Start Address Register (MDSTA at "55h")

The start address register (MDSTA at "55h") is used to specify the eight low-order bits of a start address for DMA transfer. Note that the start address can be specified only in units of 16 bytes. Any value written to the four low-order bits (A3 to A0) of the start address is set to "0000". The start address register cycles its setting in the range of 256 bytes as shown below:

Start of cycle:

00F0h → 00F1h → 00F2h → ··· → 00FEh → 00FFh → 0000h

		7	6	5	4	3	2	1	0
	BLOCK	Multiplication and division							
MDSTA	Bit name	A7	A6	A5	A4	—	—	—	—
[55h]	R/W	W							
	Setting at reset time	Indefinite							
	Function	Low-order start address for DMA transfer.							

- Multiplicand/ Divisor Registers (MDMAL at "56h" and MDMAH at "57h")
- Multiplier Registers (MDPSL at "5Ah" and MDPSH at "5Bh")
- Product Sum Multiplier Registers (MDPSL at "5Ah" and MDPSH at "5Bh")
- Dividend/ Operation Result Register (MDRLL at "5Ch", MDRLH at "5Dh", MDRHL at "5Eh", and MDRHH at "5Fh")

The multiplicand registers, the multiplier registers, and the product sum multiplier registers are intended for only write operation while the operation result registers are intended for both write and read operations. At reset time, these registers have indefinite states.

9.8 Division Mode

In the division mode, the multiplier/ divider performs dividing operation on unsigned 32bit dividend data by 16bit divider data to yield 16bit quotient data and 16bit remainder data.

The multiplier/ divider starts dividing operation upon writing divider data to the low-order and high-order divider registers (MDMAL at "56h" and MDMAH at "57h") and then writing dividend data to the low-order and high-order dividend registers (MDRLL at "5Ch", MDRLH at "5Dh", MDRHL at "5Eh", and MDRHH at "5Fh"). After the interval of the 8 system clock pulses, the multiplier/ divider sets resulting quotient data and remainder data in the operation result registers (MDRLL at "5Ch" and MDRLH at "5Dh") and the operation result registers (MDRHL at "5Eh" and MDRHH at "5Fh").

Write operation must always be performed first on the low-order and high-order divider registers and then on the low-order and high-order dividend registers (MDRLL, MDRLH, MDRHL, and MDRHH) in this order.

*) In response to a word data transfer instruction, the CPU always makes read/write access first to the low-order registers and then to the high-order registers.

When reading the operation result registers before the completion of dividing operation, the CPU remains in the wait state until the completion of dividing operation. In this event, therefore, the CPU can always obtain the correct result of dividing operation by reading the operation result registers immediately after the settings of the dividend registers.

Dividend		Divider	→	Quotient		Remainder
MDR	÷	MDMA		MDRLH and MDRLL	···	MDRHH and MDRHL
32 bits		16 bits		16 bits		16 bits

If any overflow occurs as a result of dividing operation, the OF flag (bit 6) is set to "1" in the status register (MDTEM at "54h"), causing both quotient and remainder data to have no significance. During the progress of dividing operation, the ACT flag (bit 7) is kept at "1" in the status register.

In the dividing mode, the settings of the divider registers are retained after the completion of the initial round of dividing operation and can therefore be reused for the subsequent rounds only by changing the settings of the dividend registers. Further, the settings of the divider registers can also be updated before the completion of dividing operation.

Note that the multiplier/ divider cannot perform multiplying and dividing operations simultaneously.

10. Analog-to-digital (A/D) Converter

The 10bit A/ D converter performs sequential A/ D conversion with a maximum conversion time of 21.0µs. It converts an input analog signal (ADIN) into digital form upon setting the ST bit (bit 7) to "1" in the mode/ status register (ADMD at "34h").

The input ADIN signal is sampled after the interval of the 2 A/ D conversion clock pulses, converted into digital form after the interval of the 21 A/ D conversion clock pulses, and ready for readout upon the lapse of the next A/ D conversion clock pulse.

The A/ D converter performs A/ D conversion only once. During the progress of A/ D conversion, the TR bit (bit 7) is kept at "1" in the mode/ status register.

Upon the completion of A/ D conversion, the A/ D conversion end interrupt (ADINT) is generated, automatically setting the power saving mode.

10.1 Mode/Status Register (ADMD at "34h")

At write time, the mode/ status register (ADMD at "34h") functions as the mode register to control A/ D conversion. At read time, it functions as the status register to indicate the status of A/ D conversion.

10.1-1 Mode Register (ADMD at "34h")

		7	6	5	4	3	2	1	0
ADMD [34h]	BLOCK	A/ D converter							
	Bit name	ST	—	—	—	—	—	—	—
	R/ W	W							
	Setting at Reset time	0	0	0	0	0	0	0	0
	Function	Start of A/ D conversion 1:The start of A/ D conversion							

The A/ D converter starts A/ D conversion upon setting the ST bit to "1" in the mode register.

Note that bits 0 to 6 must always be set to "0" in the mode register.

10.1-2 Status Register (ADMD at "34h")

		7	6	5	4	3	2	1	0
ADMD [34h]	BLOCK	A/ D converter							
	Bit name	ST	—	—	—	—	—	—	—
	R/ W	R							
	Setting at Reset time	0	0						
	Function	Start of A/ D conversion 1:The progress of A/ D conversion							

After the ST bit is set to "1" in the mode register to specify the start of A/ D conversion, a delay occurs for the maximum duration of the 2 A/ D conversion clock pulses until the TR bit is set to "1" in the status register to indicate the progress of A/ D conversion. Note that the stop modes (digital and full) cannot be set during the progress of A/ D conversion.

10.2 Conversion Time Selection/Data Registers (ADDTL at "35h" and ADDTH at "36h")

At write time, the conversion time selection/ data registers (ADDTL at "35h" and ADDTH at "36h") function as the conversion time selection registers to specify the frequency division ratio of the A/ D conversion clock pulse. At read time, they function as the data registers to indicate A/ D conversion data.

10.2-1 Conversion Time Selection Registers (ADDTL at "35h")

		7	6	5	4	3	2	1	0
ADDTL [35h]	BLOCK	A/ D converter							
	Bit name	ST	—	—	—	T3	T2	T1	T0
	R/ W	W							
	Setting at Reset time	Indefinite							
	Function					Frequency division ratio 0000 : Disables the A/ D conversion clock pulse. 0001 : 1/ 2 of the A/ D conversion clock pulse. 0010 : 1/ 3 of the A/ D conversion clock pulse. 1111 : 1/ 16 of the A/ D conversion clock pulse.			

The frequency division ratio of the A/ D conversion clock pulse can be specified by the T3 to T0 bits (bits 3 to 0) relative to the system clock pulse (a divided-by-two clock pulse input from the X1 pin). For example, when the system clock pulse is set to 8 MHz with the X1 pin set to 16 Mhz, the A/ D conversion clock pulse can be set to 1 MHz by specifying its frequency division ratio of 1/ 8 (setting the T3 to T0 bits to "0111").

The A/ D conversion clock pulse must not exceed its maximum frequency rating of 1 MHz and must always have the setting of "0001" or more. Note that the setting of "0000" disables the A/ D conversion clock pulse.

10.2-2 Low-order Data Registers (ADDTL at "35h")

		7	6	5	4	3	2	1	0
ADDTL [35h]	BLOCK	A/ D converter							
	Bit name	D1	D0	0	0	0	0	0	0
	R/ W	R							
	Setting at reset time	Indefinite		0					
	Function	Low-order A/ D conversion data.							

10.2-3 High-order Data Registers (ADDTH at "36h")

		7	6	5	4	3	2	1	0
ADDTH [36h]	BLOCK	A/ D converter							
	Bit name	D9	D8	D7	D5	D5	D4	D3	D2
	R/ W	R							
	Setting at reset time	Indefinite							
	Function	Low-order A/ D conversion data.							

10.3 A/D Converter Output Threshold Setting Register (ADGA at "37h")

The A/ D converter output threshold setting register (ADGA at "37h") is used to specify the threshold output value of the A/ D converter so that its input voltage may be clipped in order to prevent its faulty output due to distortion resulting from excessive amplification by the internal operation amplifiers. A clipping level above or below the specified threshold results in the A/ D converter output equivalent to the positive maximum peak- "FFC0h"and the negative minimum peak- "0000h", respectively. Of the 16bits of this register, the high-order 10bits are significant while the low-order 6bits are "0".

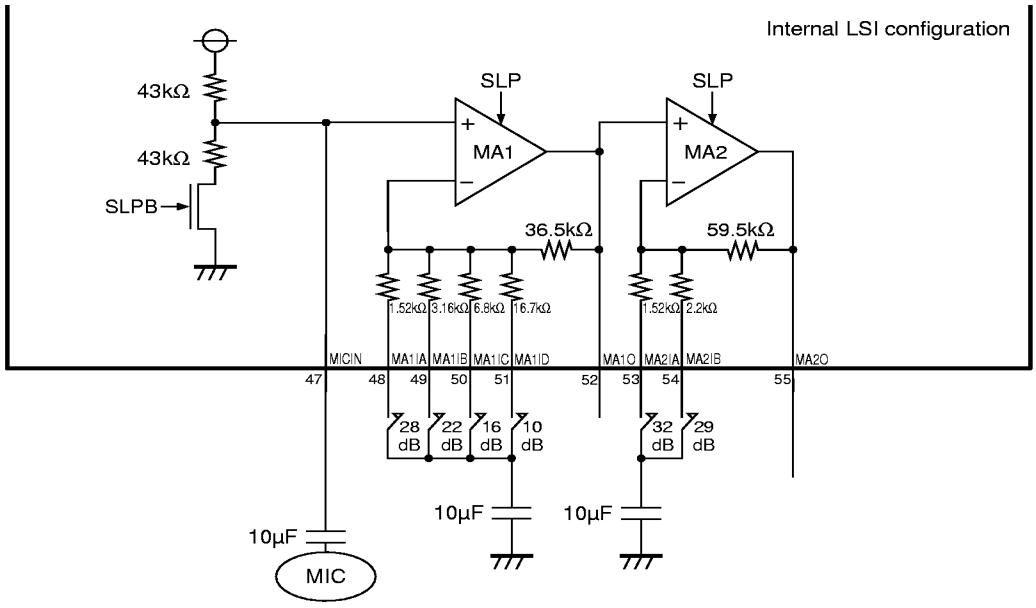
		7	6	5	4	3	2	1	0
	BLOCK	A/ D converter							
ADGA	Bit name	—	—	—	—	H1	H0	L1	L0
[37h]	R/ W	R/ W							
	Setting at Reset time	00							
	Function					Threshold output value H1 H0 L1 L0 : Threshold (High-order 10bits) X X 0 0 : None X X 0 1 : 0000XXXXXX X X 1 0 : 000XXXXXXX X X 1 1 : 00XXXXXXXX 1 1 X X : None 0 1 X X : 1111XXXXXX 1 0 X X : 111XXXXXXX 1 1 X X : 11XXXXXXXX			

*) The symbol "X" indicates a bit having no significance.

The high-order bits (H1 and H0) and the low-order bits (L1 and L0) can be set independently of each other.

11. Microphone Amplifier

The microphone amplifier is configured as shown in the diagram below:



The microphone amplifier consists of two non-inverting amplifiers (MA1 and MA2), each incorporating a resistor for determining a signaling midpoint, which requires decoupling capacitors for the microphone output intended for input to the amplifier.

The gain of the microphone amplifier can be set with the gain setting taps connected to the ground, provided that the decoupling capacitors must be connected in series for the purpose of eliminating offset current.

The microphone amplifier can be deactivated by cutting its power supply with the SLP signal from the digital units.

11.1 Correspondence between Gain Settings and Pin Connections

The gain settings of the microphone amplifier correspond to the combinations of the pins to be grounded via the gain setting taps as shown in the table below:

Mike AMP 1 / Mike AMP 2	MA1IA	MA1IB	MA1IC	MA1ID	No Connection
MA2IA	60	54	48	42	32
MA2IB	57	51	45	39	29
No Connection	28	22	16	10	0

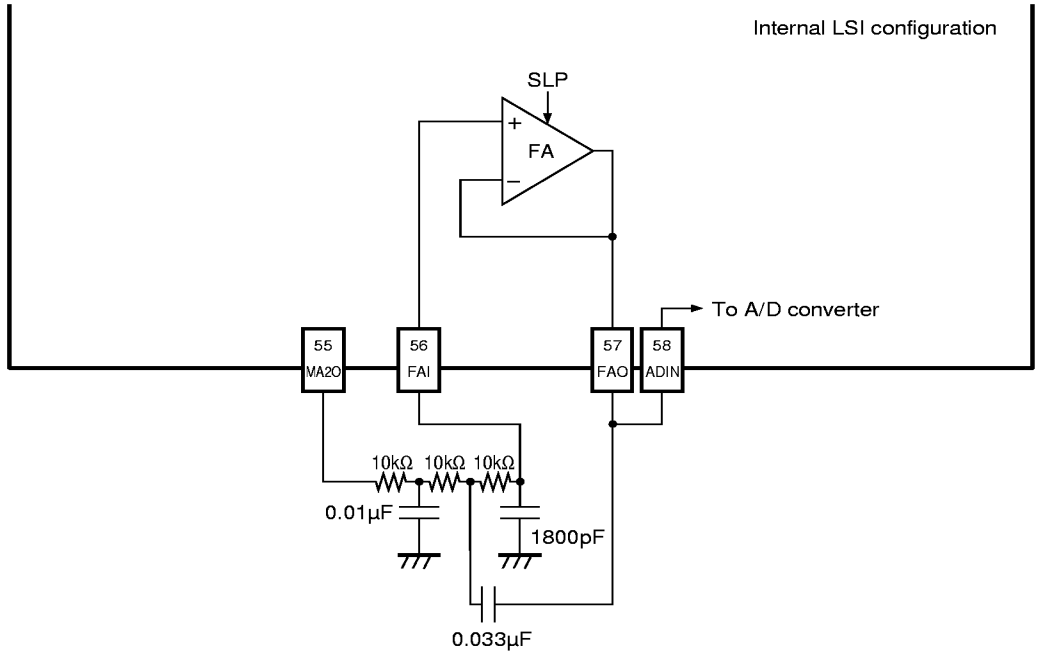
(dB)

For example, a gain of 45dB can be obtained by connecting the MA1IC and MA2IB pins to the ground via the decoupling capacitors.

As shown in the above table, the microphone amplifier can be set to a maximum gain of 60dB. For lower gain setting on the order of 30dB, the gain on the second amplifier (MA2) should be larger than the gain on the first amplifier (MA1). The gain settings are available in steps of 3dB in the range of 39dB to 60dB and 6dB in the range of 10dB to 28dB.

12. Filter Amplifier (for Antialiasing)

The filter amplifier is configured as shown in the diagram below:

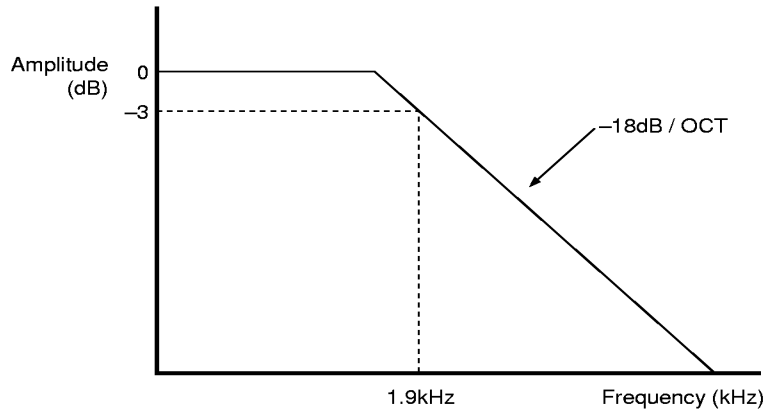


The filter amplifier incorporates the buffer to configure an antialiasing filter. The above diagram exemplifies the configuration of the third low-pass filter, which achieves filtering in response to the second amplifier (MA2O) output. The FAO output should be connected to the ADIN input.

The filter amplifier can be deactivated by cutting its power supply with the SLP signal from the digital units.

Note that the the number and settings of the external units shown in the above diagram represent standard values and vary depending on the expected rate of voice recognition and the degree of perfection of independent dictionaries.

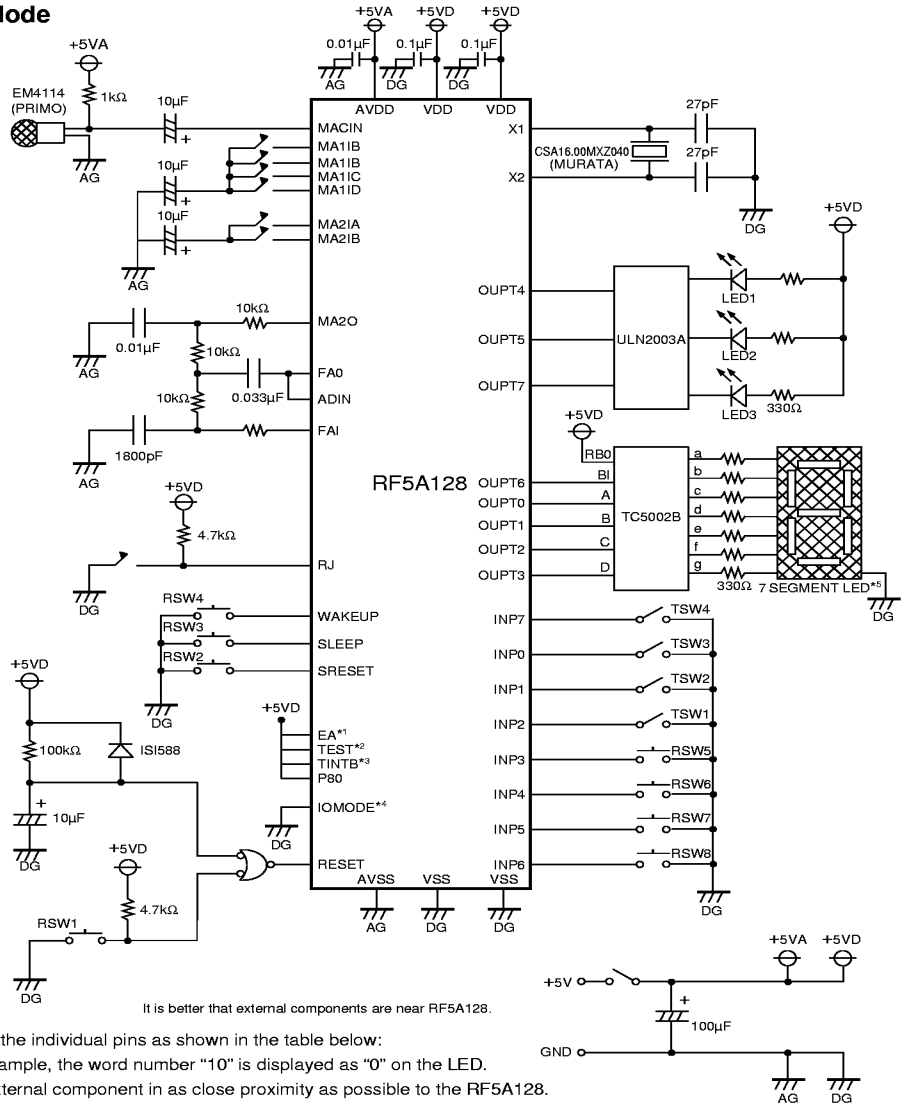
Filter Characteristics under Settings Shown in Above Diagram



TYPICAL SYSTEM CONFIGURATION

(The following description applies to those features which are implemented by software supplied as standard.)

• Stand Alone Mode

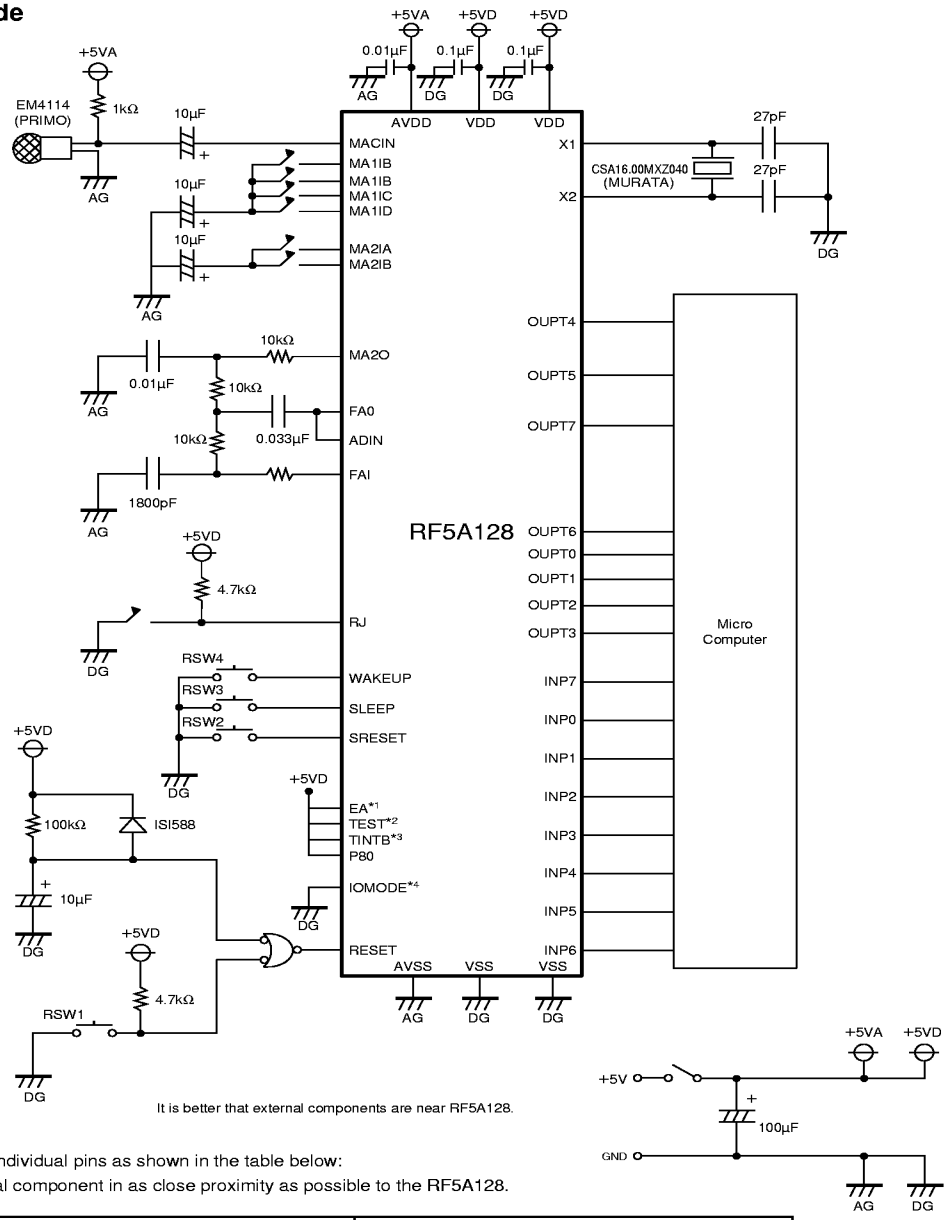


It is better that external components are near RF5A128.

∗1) to ∗4) : Connect the individual pins as shown in the table below:
∗5) : In the circuit example, the word number "10" is displayed as "0" on the LED.
∗6) : Connect any external component in as close proximity as possible to the RF5A128.

Pin Name	Switch mode				External processor mode			
	ROM setting		RAM setting		ROM setting		RAM setting	
	Internal	External	Internal	External	Internal	External	Internal	External
EA	H	L	—	—	H	L	—	—
TEST	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD
TINTB	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD
P80	—	—	H	L	—	—	H	L
IOMODE	L	L	L	L	H	H	H	H

• **External Host Mode**



It is better that external components are near RF5A128.

∗1) to ∗4) : Connect the individual pins as shown in the table below:
∗5) : Connect any external component in as close proximity as possible to the RF5A128.

Pin Name	Switch mode				External processor mode			
	ROM setting		RAM setting		ROM setting		RAM setting	
	Internal	External	Internal	External	Internal	External	Internal	External
EA	H	L	—	—	H	L	—	—
TEST	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD
TINTB	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD
P80	—	—	H	L	—	—	H	L
IOMODE	L	L	L	L	H	H	H	H

RF5A128 EVALUATION BOARD EXPLANATION

RF5A128 provides a evaluation board.
The circuit of the board has same configuration as of the Typical System of Stand Alone Mode.

• Switch description of evaluation board

Push SW	Function	Action
RSW1	Reset	Reset the LSI. And stop the repetitive recognition.
RSW2	SRESET	Reset the LSI. Also Dependent-dictionary is cleared.
RSW3	SLEEP	Set the LSI to Stand-by mode.
RSW4	WAKEUP	Resume the LSI.
RSW5	Registration	Registration of the Dependent dictionary.
RSW6	Recognition one time	Recognize Voice one time.
RSW7	Repetitive Recognition	Recognize repetitive. To stop this, push reset.
RSW8	Deletion	Delete the Dependent dictionary (one word at time)

Toggle SW	in Recognition	in Registration or Deletion
TSW1	Rejection Invalid	Word number bit2 (ON : 1, OFF : 0)
TSW2	Independent	Word number bit1 (ON : 1, OFF : 0)
TSW3	dependent	Word number bit0 (ON : 1, OFF : 0)
TSW4	Cluster (ON : C2, OFF : C1)	· Cluster in registration (ON : C2, OFF : C1) · N/A in Deletion

LED	Function
LED1	LIT : Result is Dependent Not LIT : Result is Independent
LED2	LIT : Waiting voice for recognition Not LIT : Detecting utterance
LED3	LIT : Waiting voice for registration Not LIT : Detecting utterance
7 SEGMENT LED	Recognition result word number Display. (1 to 9, 0), Word number 10 is displayed [0].

1. Voice Recognition for Unspecified Speakers

• Vocabulary

A voice dictionary must be customized for voice recognition for unspecified speakers. For details, feel free to make a separate inquiry.

• Single-step Recognition Mode

Turn on the "Voice Recognition for Unspecified Speakers" switch, press the "Cluster Selection" switch to select a cluster to be recognized, and press the "Single-shot Recognition" switch. Then, the single-step recognition mode will be set in which only one voice input is recognized in a single step. Input a voice after confirming that the "Wait for Voice Input for Recognition" LED comes on.

Upon completion of voice input, the "Result of Voice Recognition for Specified Speakers" LED goes off while the result of voice recognition is displayed on the "Recognition Result Number Indication" LED.

If the "Recognition Result Number Indication" LED remains off, it indicates failure in voice recognition.

The "Wait for Voice Input for Recognition" LED also remains off during voice input. If the "Wait for Voice Input for Recognition" LED remains on, it indicates voice input in an excessively low tone or at an excessively great distance from the microphone or an improper gain of the amplifier for the microphone.

• Continuous Recognition Mode

Turn on the "Voice Recognition for Unspecified Speakers" switch, press the "Cluster Selection" switch to select a cluster to be recognized, and press the "Continuous Recognition" switch. Then, the successive recognition mode will be set in which several voice inputs are recognized in succession.

Upon completion of every voice input, the result of voice recognition is displayed on the "Recognition Result Number Indication" LED to wait for the next voice input.

To end the successive recognition mode, press the "Reset" switch. (It can also be ended by pressing the "Super Reset" switch provided that voice dictionaries for all registered words are cleared.)

• Disabling Reject Feature

The reject feature can be disabled by turning on the "Voice Recognition for Unspecified Speakers" switch and the "Reject Disable" switch simultaneously.

2. Voice Recognition for Specified Speakers

• Registration*1

Press the "Register Word Bits 0 to 2" switch to specify a word number assigned to a word to be registered and press the "Cluster Selection" switch to select a cluster to be registered.

At this time, pressing the "Specified Registration" switch turns on the "Wait for Voice Input for Registration" LED to wait for voice input.

The "Wait for Voice Input for Registration" LED goes off upon commencement of every voice input and comes on upon completion of every voice input. Upon completion of registration of three input words, the initial state is restored with the "Wait for Voice Input for Registration" LED going off and the specified word number displayed momentarily on the "Recognition Result Number Indication" LED. This ends the process of word registration.

Note here that more than three voice inputs may be required depending on their conditions.

If registration of any word is terminated with the "Wait for Voice Input for Registration" LED on, a voice dictionary for that word will not be created, assuming that its registration has been suspended. If the "Wait for Voice Input for Registration" LED, the "Wait for Voice Input for Recognition" LED, and the "Result of Voice Recognition for Specified Speakers" LED come on during registration of any word, they indicate occurrence of an error in creation of a voice dictionary for that word. In this event, reattempt registration of that word.

Word number	Bit 2	Bit 1	Bit 0	Cluster
1	OFF	OFF	ON	C1/ 2
2	OFF	ON	OFF	C1/ 2
3	OFF	ON	ON	C1/ 2
4	ON	OFF	OFF	C1/ 2
5	ON	OFF	ON	C1/ 2
6	ON	ON	OFF	C1/ 2
7	ON	ON	ON	C1/ 2

Available word numbers range from 1 to 7 and should be specified in binary notation.

A maximum of 7 words can be registered each with a total duration of 2 seconds. Any attempt to register a word with a total duration of more than 2 seconds will turn on the "Wait for Voice Input for Registration" LED and the "Wait for Voice Input for Recognition" LED as a warning.

In this event, no more word can be registered.

Meanwhile, two clusters "C1" and "C2" are available for selection for each word.

Note 1) All voice dictionaries are cleared upon power-off.

*1) All voice dictionaries are cleared upon power-off.

• Deletion

Press the "Register Word Bits 0 to 2" switch to specify a word number assigned to a word to be deleted and press the "Specified Deletion" switch. Then, a voice dictionary for that specified word will be cleared.

Note that overwriting a newly registered word on a previously registered word clears a voice dictionary for the latter automatically. Also note that pressing the "Super Reset" switch clears the voice dictionaries for all registered words.

If the "Wait for Voice Input for Registration" LED, the "Wait for Voice Input for Recognition" LED, and the "Result of Voice Recognition for Specified Speakers" LED come on during deletion of any word, they indicate occurrence of an error in clearance of a voice dictionary for that word (i.e. an attempt to delete an unregistered word).

In this event, check the correct word to be deleted and reattempt its deletion.

• Single-step Recognition Mode

Turn on the "Voice Recognition for Specified Speakers" switch, press the "Cluster Selection" switch to select a cluster to be recognized, and press the "Single-shot Recognition" switch. Then, the single-step recognition mode will be set in which only one voice input is recognized in a single step.

Input a voice after confirming that the "Wait for Voice Input for Recognition" LED comes on.

Upon completion of voice input, the "Result of Voice Recognition for Specified Speakers" LED goes off while the result of voice recognition is displayed on the "Recognition Result Number Indication" LED.

If the "Result of Voice Recognition for Specified Speakers" LED fails to come on and if the "Recognition Result Number Indication" LED remains off, they indicate failure in voice recognition.

The "Wait for Voice Input for Recognition" LED also remains off during voice input.

If the "Wait for Voice Input for Recognition" LED remains on, it indicates voice input in an excessively low tone or at an excessively great distance from the microphone or an improper gain of the amplifier for the microphone.

• Continuous Recognition Mode

Turn on the "Voice Recognition for Specified Speakers" switch, press the "Cluster Selection" switch to select a cluster to be recognized, and press the "Continuous Recognition" switch. Then, the successive recognition mode will be set in which several voice inputs are recognized in succession.

Upon completion of every voice input, the result of voice recognition is displayed on the "Recognition Result Number Indication" LED to wait for the next voice input.

To end the successive recognition mode, press the "Reset" switch. (It can also be ended by pressing the "Super Reset" switch provided that voice dictionaries for all registered words are cleared.)

• Disabling Reject Feature

The reject feature can be disabled by turning on the "Voice Recognition for Unspecified Speakers" switch and the "Reject Disable" switch simultaneously.

Combined Voice Recognition for Specified and Unspecified Speakers

Turn on both the "Voice Recognition for Specified Speakers" switch and the "Voice Recognition for Unspecified Speakers" switch.

For voice recognition for specified speakers:

The "Result of Voice Recognition for Specified Speakers" LED comes on while the result of voice recognition is displayed on the "Recognition Result Number Indication" LED.

For voice recognition for unspecified speakers:

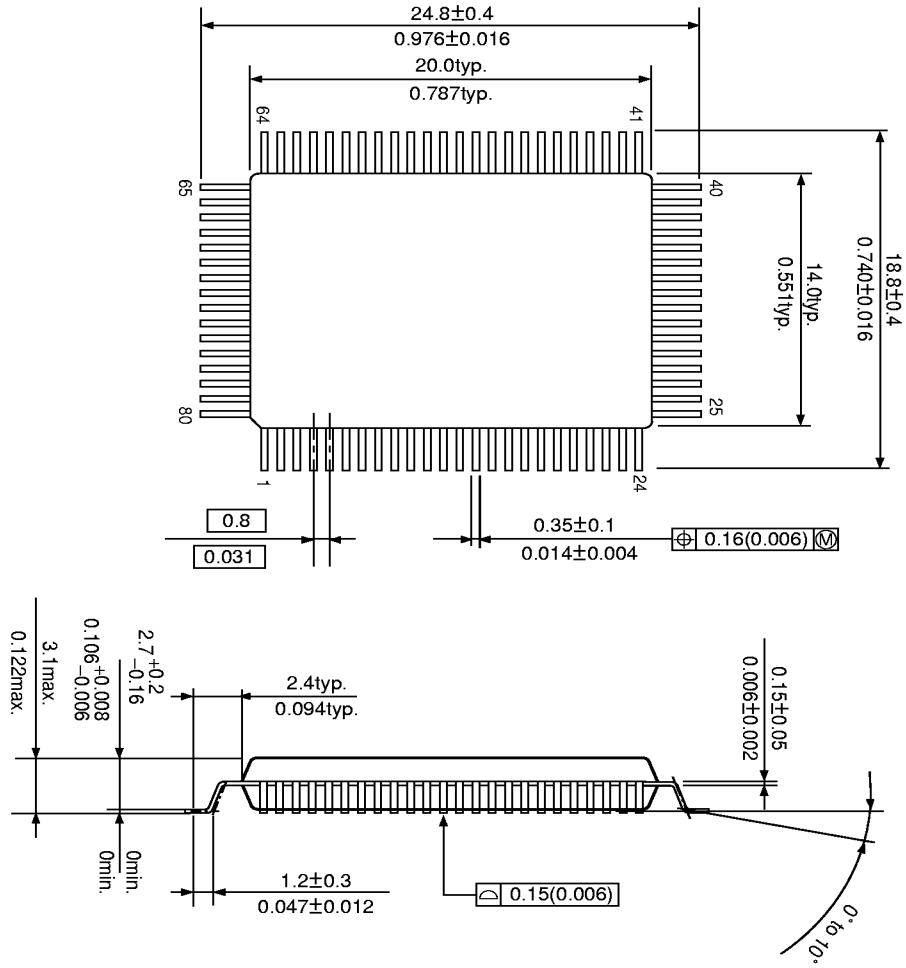
The "Result of Voice Recognition for Specified Speakers" LED goes off while the result of voice recognition is displayed on the "Recognition Result Number Indication" LED.

For failure in voice recognition:

The "Recognition Result Number Indication" LED remains off.

PACKAGE DIMENSIONS

• **80pin QFP**



UNIT : mm / inch