Interfacing Motorola's MPC56x Microcontroller to AMD's Am29BDD160G Flash Memory

Application Note

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The following document refers to Spansion memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

Continuity of Specifications

There is no change to this document as a result of offering the device as a Spansion product. Any changes that have been made are the result of normal documentation improvements and are noted in the document revision summary, where supported. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

Continuity of Ordering Part Numbers

AMD and Fujitsu continue to support existing part numbers beginning with "Am" and "MBM". To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local AMD or Fujitsu sales office for additional information about Spansion memory solutions.

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Introduction

This document describes how to connect AMD's 16 megabit Am29BDD160GB Flash memory to the MPC56x series of processors from Motorola without glue logic. Topics include: two interface options, the synchronous mode enable sequence, and the register configuration for the Flash and processor.

The Am29BDD160GB is a 16 megabit, 66 MHz high-performance burst flash that can be organized in either 512 Kb by 32-bit or 1 Mb by 16-bit memory array. If the 1 Mb by 16-bit memory array is chosen, two Am29BDD160G flash memory devices can be connected to the processor to provide up to a total of 1 Mb by 32-bit of Flash memory. The Am29BDD160GB features include: 2.5-Volt single power supply, Burst Mode, Bottom Boot, and Simultaneous Read/Write Operations.

The MPC56x family of processors is designed for advanced applications in the automotive market and currently has a maximum operation frequency of 56 MHz. MPC56x series of processors operates with 2.6-Volt Power Supply across the full automotive temperature range and support functions such as single read or write and burst read operations.

Power Supply Requirements

The internal logic of the processor requires 2.6 volts. The Flash can operate between 2.3 and 2.75 volts. A 2.6-volt power supply can be connected to V_{DD} and routed to the following power pins on the processor, which are V_{DDF}, QV_{DDL}, NV_{DLL} and KAPWR. The V_{CC} and V_{CCQ} pins of the flash memory can interface directly to the V_{DD} pin of the microprocessor as long as the supply is regulated within 5% in order not to exceed the 2.75 V maximum that the Flash can handle. The ground pins V_{SS} and V_{SSF} pins on the microprocessor can be connected directly to V_{SS} of the flash memory.

Table 1. Power and Ground Interface

CPU	Flash
V_{DD}, V_{DDF}, QV_{DDL}, NV_{DLL}, KAPWR	V_{CC}, V_{CCQ}
V_{SS}, V_{SSF}	V_{SS}

Hardware Reset

The H_{RESET}# pin of the microprocessor must be connected to the RESET# pin of the flash memory to reset the MPC56x and Am29BDD160G devices during unexpected power down situations as V_{DD} and V_{CC} voltages drops and to ensure that the Flash is ready to read boot code following any system reset.

Table 2. Reset Interface

CPU	Flash
HRESET#	RESET#

Data Bus Interface

Since the MPC56x processor typically has its data order configured as most significant bit to least significant bit and the Am29BDD160G flash memory least significant bit to most significant bit, the address and data pins connections must be bit number reversed. In x32 mode for the flash memory, D0 of the microprocessor must be connected to D31 of the flash memory, and vice versa. For x16 mode, two flash devices are used in parallel to still provide the 32 bit wide data and increase the memory size. The microprocessor D0 to D15 is connected to the high order Flash D15 to D0 and the microprocessor D16 to D31 is connected to the low order Flash D15 to D0.

Table 3. Data Bus Interface

Mode	CPU	Flash
32-bit	D0–D31	D31–D0 (Note)
16-bit	D0–D15	D15–D0 Flash 1 (Note)
	D16– D31	D15– D0 Flash 2 (Note)

Where F1 and F2 each represent a 16-bit flash device (i.e. 2 Flash at x16 = x32).

Note: Observe bit order reversal between CPU and Flash.

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Address Bus Interface

When the flash memory array is used in by 32-bit mode, 19 address lines are required to address the 512 Kb by 32-bit memory array. Address pins A0 to A18 of the flash memory are connected to A29 to A11 of the microprocessor. For by 16-bit mode, 20 address lines are required and Address pins A-1 (A minus 1) to A18 are connected to A30 to A11 of the microprocessor.

Table 4. Address Bus Interface

Mode	CPU	Flash
32-bit	A29 - A11	A0 - A18
16-bit	A30	A-1 (A minus 1 pin)
	A29 - A11	A0 - A18 (Note)

Note: Observe bit order reversal between CPU and Flash.

To select 16-bit and 32-bit modes, the WORD# pin must be tied to V_{SS} or V_{CC} respectively. It is recommended that the A-1 pin of the flash memory be either tied to V_{CCQ} or V_{SS} when the device is in the 32-bit mode to reduce potential noise injection to the flash.

Control Bus Interface

The CLK, CE#, OE#, WE#, and ADV# control signals from the flash memory must be connected to CLK, CSx#, OE#, WE#, and TS# of the microprocessor.

Table 5. Control Bus Interface

CPU	Flash
CLK	CLK
CSx# (Note)	CE#
OE#	OE#
WE#	WE#
TS#	ADV#
WE0# (32-bit mode)	WE#
WE0# (16-bit mode)	WE# (Flash 1)
WE2# (16-bit mode)	WE# (Flash 2)

Note: CSx# can be any of the MPC56x chip select signals; however, if botting from Flash then CS0# must be used.

Bus Operations and Timings

Configuration Before Reset

To select either one flash memory with 32-bit data bus or two flash memories with 16-bit data buses, the Port Size field in the microprocessor MPC56x BR0 Configuration Register must be set to 00 or 10 respectively.

Boot-up From Flash

The signal timings of the flash memory and the processor are compatible to a burst frequency of at least 56 MHz. Upon boot-up, asynchronous read is on the default mode of the flash memory. The MPC56x microprocessors come out of reset in sequential mode with its default setting of 15 wait states, which meets all of the timing requirements for single access in asynchronous mode of the Flash.

Synchronous Burst Mode

To enter synchronous burst mode after initial boot code execution in asynchronous read mode, the following steps are required:

1. Make sure the boot code is already programmed into the flash memory
2. Boot up the system and copy (shadow) the burst mode configuration code into internal SRAM
3. Exit MPC56x Serialized Mode by modifying the ISCT_SER field in the ICTRL Register to 10b
4. Branch to the mode changing code copy in the SRAM
5. Program Am29BDD160GB Configuration Register
6. Program MPC56x BR0 Register for burst mode
7. Program MPC56x OR0 Register for burst mode
8. Set Burst Enable (BE) and (BURST_EN) bits in the MPC56x BBCMCR and SIUMCR Registers
9. After the code has been executed, branch back to the code in flash

Enabling Burst Sequence

To enable burst mode for the flash memory, the Am29BDD160GB Flash Configuration

Register is written with the sequence as follows in Table 6.

Table 6. Am29BDD160GB Configuration Register Write Definition

Clock	Cycle 1	Cycle 2	Cycle 3	Cycle 4
Addr	555h	2AAh	555h	XX
Data	AAh	55h	D0h	WD

Note: The MPC56x uses byte addresses whereas the AMD Flash uses 32-bit word addresses. Pins 30:31 are not connected. Therefore, address CPU A29 is attached to Flash A0, instead of CPU A31. This results in an address shift left by 2 bits.

'WD' represents the 16-bit Flash Configuration Register settings. Please examine Table 1 in the Am29BDD160GB datasheet for information on device bus operations.

The bit settings for the Flash Configuration register after boot-up are shown in Table 7.

Table 7. Am29BDD160GB Flash Configuration Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RM	**DS**	**IAD3**	**IAD2**	**IAD1**	**IAD0**	**DOC**	**WC**	**BS**	**CC**	**—**	**—**	**—**	**BL2**	**BL1**	**BL0**
1	0	0	1	0	1	0	X	X	X	1	0	0	0	X	X

The following parameters need to be modified in the Configuration Register by using Configuration Register write commands while the Embedded Algorithm (a program or erase operation) is not active. The RM bit must be set to zero to enable synchronous burst operations. Bits BS and BL needs to be set accordingly for linear or interleaved burst and to determine the number of cycles per burst respectively. Bit definitions that need to be modified are as follows:

RM	0 for Sync. Burst Reads 1 for Async. Reads
IAD[3:0]	0010b for data valid after 4th rising edge on next rising edge of clock
BS	0 for Interleaved Burst 1 for Linear Burst
BL[2:0]	Determines the number of consecutive burst cycles: 001 = 8 byte burst 010 = 16 byte burst 011 = 32 byte burst 100 = 64 byte burst 111 = continuous burst
IAD[3:0]	0000 = 2 CLK Cycle 0001 = 3 CLK Cycle 0010 = 4 CLK Cycle 0011 = 5 CLK Cycle 0100 = 6 CLK Cycle 0101 = 7 CLK Cycle 0110 = 8 CLK Cycle 0111 = 9 CLK Cycle

For example, assume that a controller is in Continuous Linear Burst with a Burst Initial Access Delay (from the Flash perspective) of 5 clock cycles and a subsequent burst access of 1 clock cycle. Also assume that burst starts from the rising clock edge and the IND/WAIT# output is asserted during the delay. The Configuration Register settings are shown in Table 8.

Table 8. Am29BDD160GB Flash Configuration Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RM	**DS**	**IAD3**	**IAD2**	**IAD1**	**IAD0**	**DOC**	**WC**	**BS**	**CC**	**—**	**—**	**—**	**BL2**	**BL1**	**BL0**
0	0	0	0	1	1	0	0	1	1	0	0	0	1	1	1

The MPC56x generates 15 wait states by default for either a random access read or the initial read of a burst access. Similarly, the Am29BDD160G has a default Burst Initial Access Delay of 9 clock cycles. This means that both the MPC56x Memory Controller Option Register (ORx[24-27]) and the AM20BDD160G Configuration Register (IAD[3:0]) must be modified to insure correct operation. It is important to note here that the number of MPC56x wait states may differ from the number of clock cycles comprising the Burst Initial Access delay. The first wait state (clock cycle) for the MPC56x is the CLK cycle that puts the address on the bus and then latches it with the falling edge of both the CLK and ADV#. However, the first clock cycle for the Burst Initial Access Delay is the clock with either the first valid clock edge after ADV# assertion or the rising edge of ADV#. See Figure 1 for a graphic of Burst Initial Access Delay. The Burst Initial Access Delay is defined as the number of CLK cycles that must elapse from the first valid clock edge after ADV# assertion (or the rising edge of ADV#) until the first valid CLK edge when the data is valid. See Table 1 for a breakdown of Configuration Register settings and the corresponding Burst initial Access Delay.

Figure 1 and Table 1 are valid for the majority of applications, and have the following operating conditions.

- Burst initial access starts with the first CLK rising edge after ADV# assertion.
- Configuration Register 6 is set to 1 (CR[6] = 1). Burst starts and data outputs on rising CLK edge.

With these operating conditions valid for Table 1 and Table 1, there is a one cycle (wait state) difference between the flash and the controller, with the controller being one cycle greater.

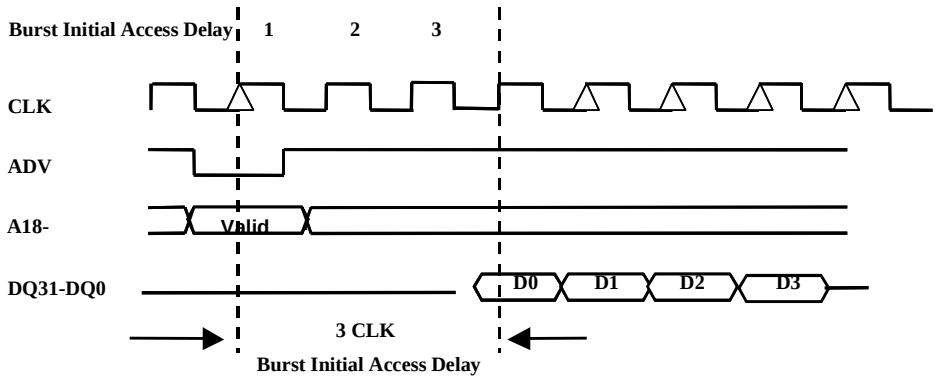

Figure 1. Burst Initial Access Delay

Table 9. Burst Initial Access Delay

Configuration Register Setting				Burst Initial Access Delay (CLK cycles)
CR13	**CR12**	**CR11**	**CR10**	
0	0	0	0	2
0	0	0	1	3
0	0	1	0	4
0	0	1	1	5
0	1	0	0	6
0	1	0	1	7
0	1	1	0	8
0	1	1	1	9

Table 10. Am29BDD160G and MPC56x Access Delays

	Am29BDD160G		MCP65x	
System Clock Speed	**Configuration Register IAD[3:0]**	**Burst Initial Access Delay**	**Total Wait States**	**ORx Configuration Register ORx[24-27]**
56 MHz	0010b	4	5	**0011b**
66 MHz	0001b	3	4	**0010b**

Table 11. MPC56x BRx Configuration Register

Bit	Name	Value	Comment
0–16	Base Address	User Defined	Flash Base Address
17–19	Address Type	User Defined	User assign the flash to any address space
20–21	Port Size	00b	00 – 32 bit Port Size 10 – 16 bit Port Size
22		0	Reserved
23	Write Protect	User Defined	0 – for flash programming 1 – for flash reading only
24		0	Reserved
25	Burst Length	User Defined	0 – Burst Access up to 4 words 1 – Burst Access up to 8 words
26	WEBS	0	
27	TBDIP	0	Do not toggle BDIP
28	LBDIP	0	No late BDIP
29	SETA	0	No external TA
30	Burst Inhibit	User Defined	0 – Enable burst access 1 – Disable burst access
31	Valid	1	Activate current bank

Table 12. MPC56x ORx Configuration Register

Bit	Name	Value	Comment
0–15	Address Mask	User Defined	0xFFE0 for mask in 16 bit setup 0xFFC0 for mask in 32 bit setup
16	Address Mask	0	Bit 16 must be on always
17–19	Address Type Mask	User Defined	User Defined
20	CSNT	0	
21–22	ACS	00b	No delay needed
23	EHTR	0	Not needed
24–27	SCY	011b	Initialize 3 wait states + 2 cycles
28–30	BSCY	000b	Initialize 1 clock period per beat
31	TRLX	0	Not needed

The MPC56x operates in Serialized Mode where instructions are executed serialized after boot-up. It is recommended for the MPC56x to exit the Sequential Mode immediately after boot-up since reading in synchronous burst mode with the default CPU configuration will degrade flash memory performance. By modifying the ISCT_SER field in the ICTRL Register to 0b1xxh (0b101, 0b110, or 0b111h) for “an indirect change of flow”, system performance can be enhanced by allowing the CPU to suspend serialized mode. For best results, the register should be set to 0b111h, since the RCPU wil output a show cycle on branches with settings of 0b101 or 0b110h.

Calculating Bus Timings

To calculate the bus timings for the CPU to flash interface, the following parameters need to be considered:

- Time for Address to become valid on to the Address Bus
- Time for Flash Memory Access
- Time for CPU Data Setup
- Time for System Margin that includes Clock Skew, Slew, and Propagation Delay
- Time for Burst Access

As an example, a 56 MHz CPU will be illustrated.

Table 13. Timing Parameters Obtained From Datasheets

Frequency	56 MHz	Source
Cycle Time	17.86 ns	1/Freq.
Data Setup	6.0 ns	MPC56x
System Margin	1.0 ns	MPC56x
Initial Access Time	< 60 ns	Am29BDD160G
Burst Access Time	< 10.0 ns	Am29BDD160G

Example: 56 MHz Operation

Initial Access Time ≤
(n + 1) * CLK period – Data Setup – System Margin
where n is the Burst Initial Access Delay

4 * (17.86–6–1) ns ≤ 64.44 ns

Burst Access Time ≤
CLK period – Data Setup – System Margin

Burst Access Time ≤
(17.86 – 6 – 1) ns ≤ 10.86 ns

Taking into account the cycle in which the address is presented by the controller, a 5-1-1-1 system is possible for 56 MHz operation. The “5” represents the total number of cycles the MPC56x must wait before the initial data can be read in a non-serialized operation. The “1”s represent the cycles needed for each additional

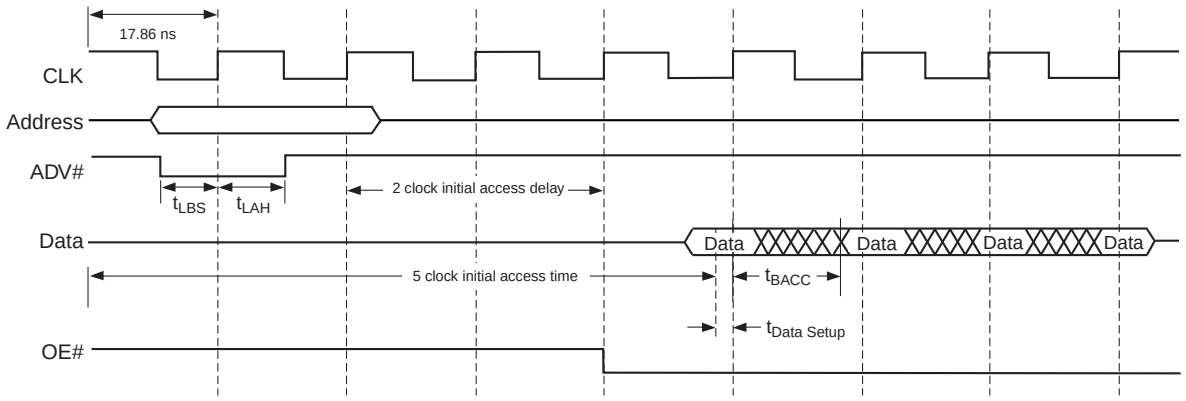

Figure 2. 56 MHz 5-1-1-1 Burst Read

Hardware Interface

The following two figures depicts the Flash CPU interfaces.

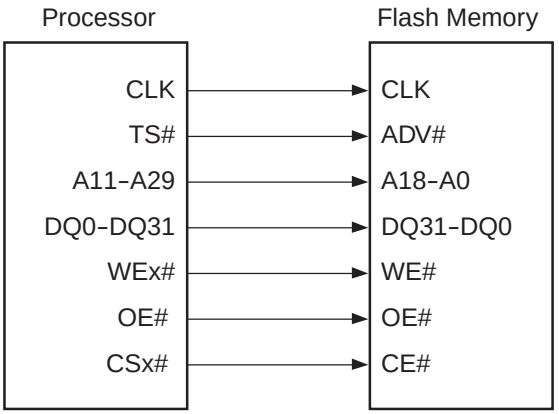

Figure 3. One x32 Flash Device Connected to the Microprocessor with the Flash WORD# Pin Tied to V_{DD}

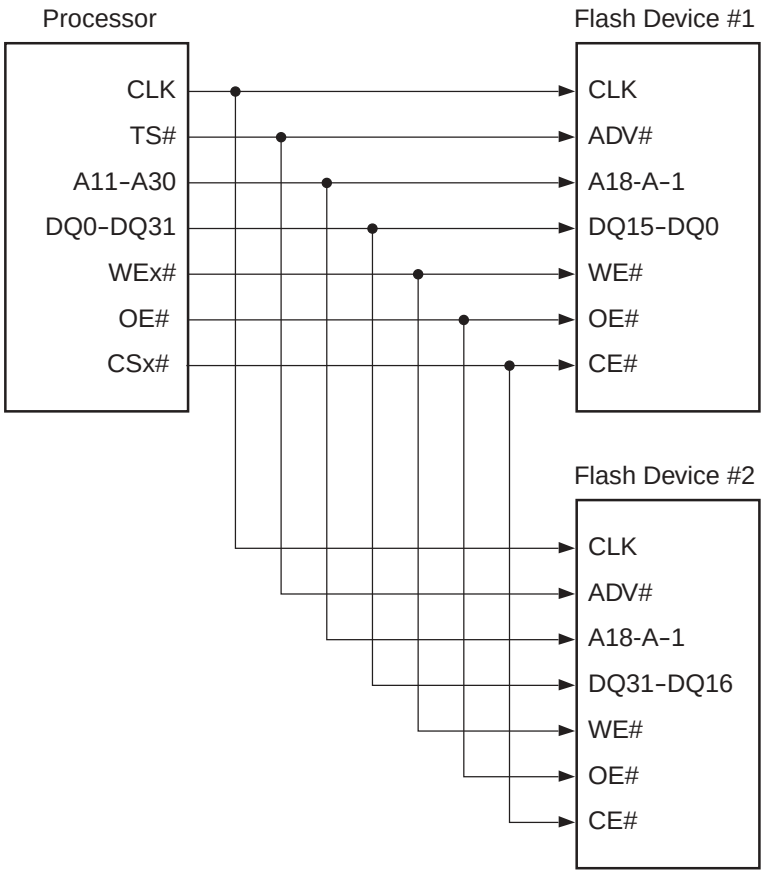

Figure 4. Two x16 Flash Devices Connected to the Microprocessor with the Flash WORD# Pin Tied to V_{SS}

APPENDIX A

Valid Part Numbers are for Revision 4a. All other Part Numbers for Revision 4 and earlier are obsolete.

Valid Combinations for PQFP Packages	
Order Number	
AM29BDD160GT54D, AM29BDD160GB54D	KI, KE
AM29BDD160GT65D, AM29BDD160GB65D	
AM29BDD160GT64C, AM29BDD160GB64C	
AM29BDD160GT65A, AM29BDD160GB65A	

Valid Combinations for Fortified BGA Packages	
Order Number	**Package Marking**
AM29BDD160GT54D, AM29BDD160GB54D	BD160GT54D BD160GB54D
AM29BDD160GT65D, AM29BDD160GB65D	BD160GT65D BD160GB65D
AM29BDD160GT64C, AM29BDD160GB64C	BD160GT64C BD160GB64C
AM29BDD160GT65A, AM29BDD160GB65A	BD160GT65A BD160GB65A

Obsolete Combinations for PQFP Packages	
Order Number	
AM29BDD160GT80C, AM29BDD160GB80C	KI, KE
AM29BDD160GT90A, AM29BDD160GB90A	

Obsolete Combinations for Fortified BGA Packages	
Order Number	**Package Marking**
AM29BDD160GT80C, AM29BDD160GB80C	BD160GT80C BD160GB80C
AM29BDD160GT90A, AM29BDD160GB90A	BD160GT90A BD160GB90A

REVISION SUMMARY

Revision A (January 17, 2002)

Initial release.

Revision B (April 14, 2003)

Table 3. Data Bus Interface

Updated table, added note.

Table 4. Address Bus Interface

Updated table, added note.

Table 5. Control Bus Interface

Updated table, added note.

Bus Operations and Timings

Modified Step 3 under Synchronous Burst Mode.

Updated Table 6, Am29BDD160G Configuration Register Write Definition, added note.

Updated Table 7, Am29BDD160GB Flash Configuration Register.

Added Table 8, Configuration Register Settings Example.

Added Table 9, Burst Initial Access Delay.

Added Table 10, Am29BDD160G and MPC56x Access Delays.

Calculating Bus Timings

Updated calculations for Example: 56 MHz Operation.

Appendix A

New section.

Trademarks