Am7942

Subscriber Line Interface Circuit

Legerity™

DISTINCTIVE CHARACTERISTICS

- ■ **Programmable constant-current feed**
- ■ **Receive current gain = 200**
- ■ **Programmable loop-detect threshold**
- ■ **Low standby power**
- ■ **Performs polarity reversal**
- ■ **Ground-key detector**
- ■ **Pin for external ground-key noise filter capacitor**
- ■ **Test relay driver option**

- ■ **Tip Open state for ground-start lines**
- ■ **–19 V to –58 V battery operation**
- ■ **Ideal for PBX and KTS applications**
- ■ **On-chip switching regulator for low-power dissipation**
- ■ **Can be used with or without the on-chip switching regulator**
- ■ **Two-wire impedance set by single external impedance**
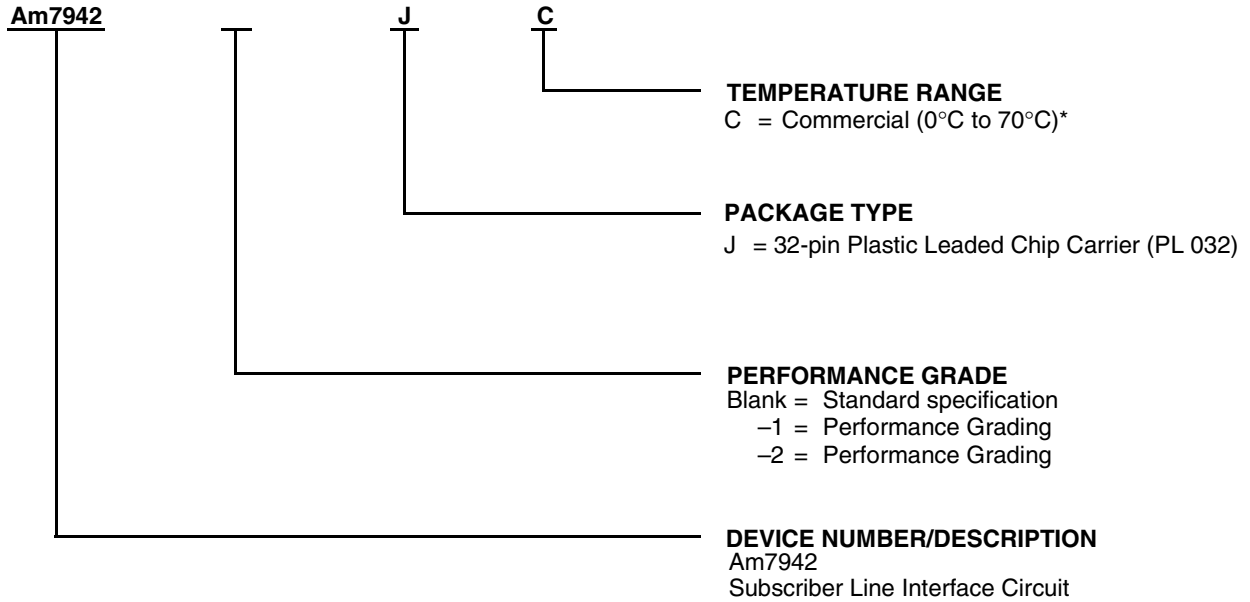- ■ **On-hook transmission**

BLOCK DIAGRAM
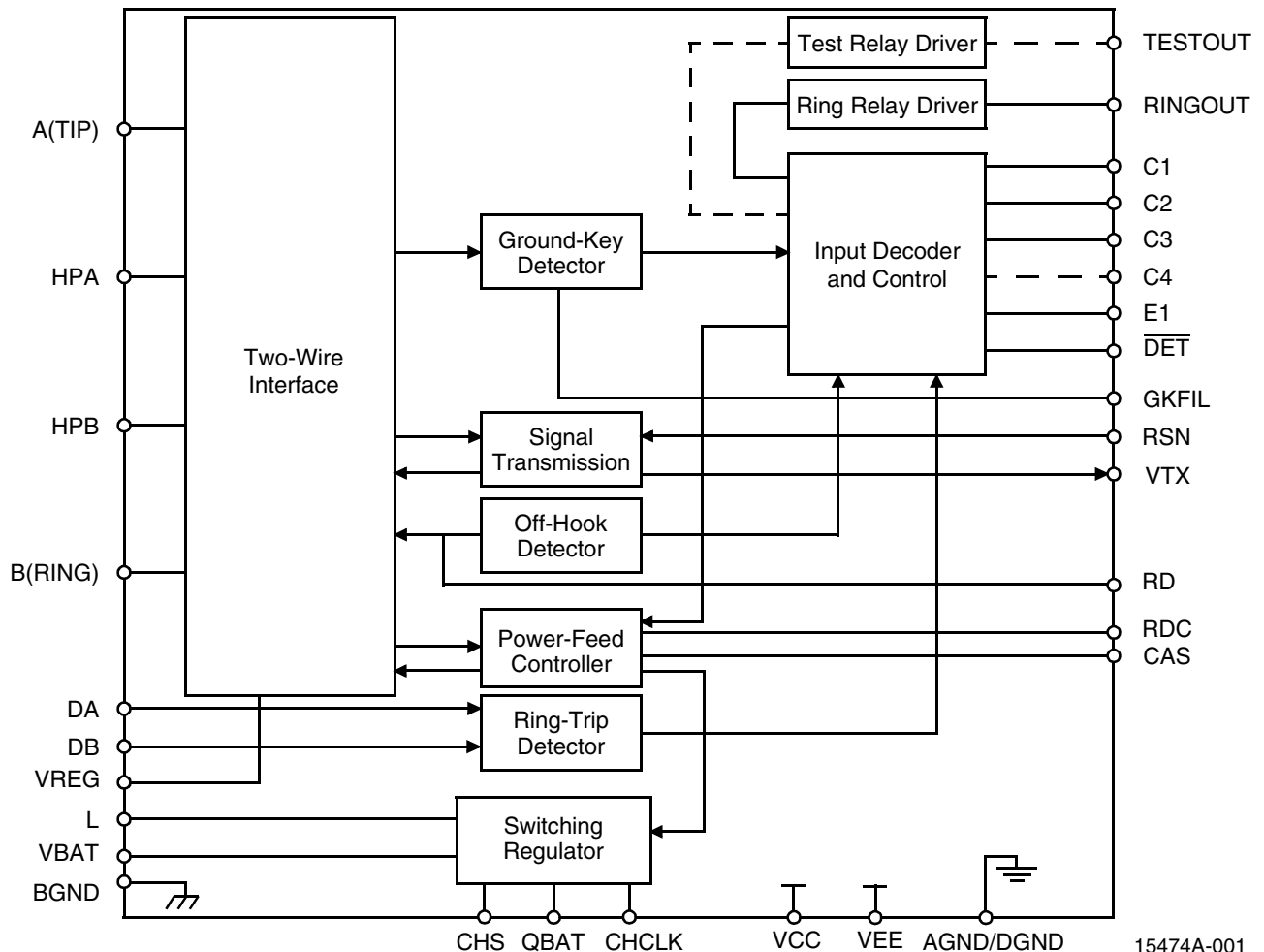
15474A-001

ORDERING INFORMATION

Standard Products

Legerity standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.

Am7942   **J**   **C**

TEMPERATURE RANGE
C = Commercial (0°C to 70°C)*

PACKAGE TYPE
J = 32-pin Plastic Leaded Chip Carrier (PL 032)

PERFORMANCE GRADE
Blank = Standard specification
   −1 = Performance Grading
   −2 = Performance Grading

DEVICE NUMBER/DESCRIPTION
Am7942
Subscriber Line Interface Circuit

Valid Combinations		
Am7942	−1 −2	JC

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local Legerity sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on Legerity's standard military–grade products.
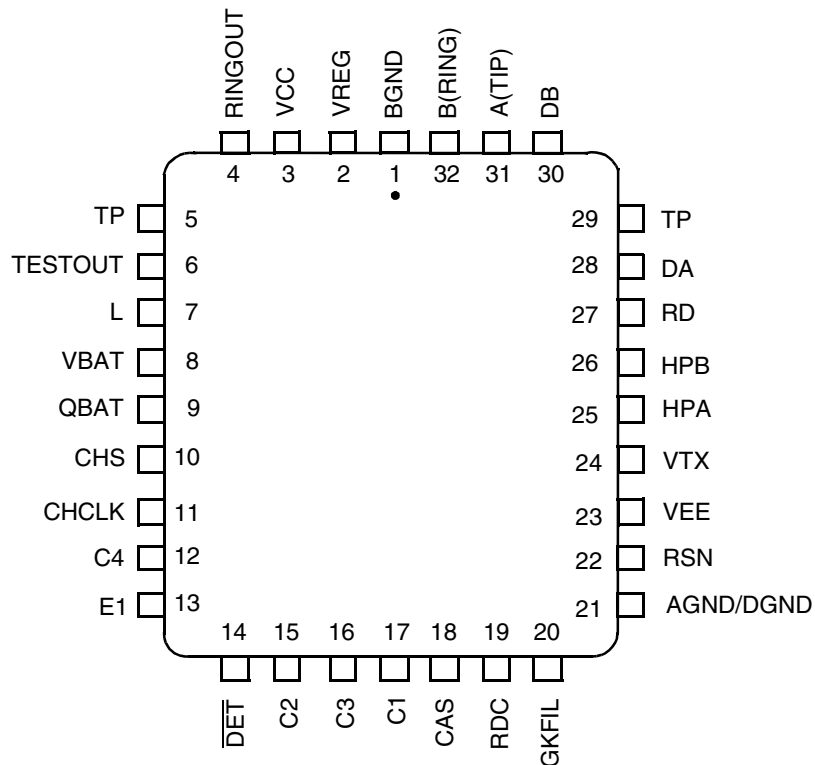
Note:
* Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from −40°C to +85°C is guaranteed by characterization and periodic sampling of production units.

CONNECTION DIAGRAMS

Top View

32-Pin PLCC

Notes:

1. Pin 1 is marked for orientation.

2. TP is a thermal conduction pin tied to substrate (QBAT).

PIN DESCRIPTIONS

Pin Names	Type	Description
AGND/DGND	Gnd	Analog and Digital ground.
A(TIP)	Output	Output of A(TIP) power amplifier.
BGND	Gnd	Battery (power) ground.
B(RING)	Output	Output of B(RING) power amplifier.
C3–C1	Input	Decoder. TTL compatible. C3 is MSB and C1 is LSB.
C4	Input	Test Relay Driver Command. TTL compatible. A logic Low enables the driver.
CAS	Capacitor	Anti-saturation pin for capacitor to filter reference voltage when operating in anti-saturation region.
CHCLK	Input	Chopper Clock. Input to switching regulator (TTL compatible). Freq = 256 kHz (typ). See Note 1.
CHS	Input	Chopper Stabilization. (See Note 1) Connection for external chopper stabilizing components.
DA	Input	Ring-trip negative. Negative input to ring-trip comparator.
DB	Input	Ring-trip positive. Positive input to ring-trip comparator.
$\overline{\text{DET}}$	Output	Switchhook detector. When enabled, a logic Low indicates the selected detector is tripped. The detector is selected by the logic inputs (C3–C1, E1). The output is open-collector with a built-in 15 kΩ pull-up resistor.
E1	Input	Ground-Key Enable. E1 = High connects the ground-key detector to $\overline{\text{DET}}$. E1 = Low connects the off-hook or ring-trip detector to $\overline{\text{DET}}$.
GKFIL	—	Connection for external ground-key, noise-filter capacitor. See Note 2.
HPA	Capacitor	High-Pass Filter Capacitor. A(TIP) side of high-pass filter capacitor.
HPB	Capacitor	High-Pass Filter Capacitor. B(RING) side of high-pass filter capacitor.
L	Output (See Note 1)	Switching Regulator Power Transistor. Connection point for filter inductor and anode of Switching Regulator Power Transistor. Connection point for filter inductor and anode of catch diode. Has up to 60 V of pulse waveform on it and must be isolated from sensitive circuits. Keep the diode connections short because of the high currents and high di/dt.
QBAT	Battery	Quiet Battery. (See Note 1). Filtered battery supply for the signal processing circuits.
RD	Resistor	Detector resistor. Detector threshold set and filter pin.
RDC	Resistor	DC feed resistor. Connection point for the DC feed current programming network. The other end of the network connects to the receiver summing node (RSN).
RINGOUT	Output	Ring Relay Driver. Open-collector driver with emitter internally connected to BGND.
RSN	Input	Receive Summing Node. The metallic current (AC and DC) between A(TIP) and B(RING) is equal to 500 x the current into this pin. The networks that program receive gain, two-wire impedance, and feed current all connect to this node.
TESTOUT	Output	Test Relay Driver. Open collector driver with emitter internally connected to BGND.
TP	Thermal	Thermal pin. Connection for heat dissipation. Internally connected to substrate (QBAT). Leave as open circuit or connected to QBAT. In both cases, the TP pins can connect to an area of copper on the board to enhance heat dissipation.
VBAT	Battery	Battery supply.
VCC	Power	+5 V power supply.
VEE	Power	–5 V power supply.
VREG	Input	Regulated Voltage. (See Note 1.) Provides negative power supply for power amplifiers. Connection point for inductor, filter capacitor, and chopper stabilization.
VTX	Output	Transmit Audio. This output is a unity gain version of the A(TIP) and B(RING) metallic voltage. VTX also sources the two-wire input impedance programming network.

Notes:

1. *All pins, except CHCLK, connect to VBAT when using SLIC without a switching regulator. CHCLK is connected to AGND/ DGND.*

2. *To prevent noise pickup by the detection circuits when using Ground-Key Detect state (E1 = logical 1), a 3300 pF minimum bypass capacitor is recommended between the GKFIL pin and ground.*

ABSOLUTE MAXIMUM RATINGS

Storage temperature . . . . –55°C to +150°C

V_{CC} with respect to AGND/DGND . . . –0.4 V to +7.0 V

V_{EE} with respect to AGND/DGND . . . +0.4 V to –7.0 V

V_{BAT} with respect to AGND/DGND. . . +0.4 V to –70 V

Note: *Rise time of V_{BAT} (dv/dt) must be limited to 27 V/μs or less when Q_{BAT} bypass = 0.33 μF.*

BGND with respect to AGND/DGND . +1.0 V to –3.0 V

A(TIP) or B(RING) to BGND:
    Continuous . . . . –70 V to +1.0 V
    10 ms (f = 0.1 Hz) . . . . –70 V to +5.0 V
    1 μs (f = 0.1 Hz) . . . .–90 V to +10 V
    250 ns (f = 0.1 Hz) . . . .–120 V to +15 V

Current from A(TIP) or B(RING). . . . .±150 mA

Voltage on RINGOUT. . . . .BGND to 70 V above Q_{BAT}

Voltage on TESTOUT. . . . .BGND to 70 V above Q_{BAT}

Current through relay drivers . . . . 60 mA

Voltage on ring-trip inputs
    (DA and DB) . . . . V_{BAT} to 0 V

Current into ring-trip inputs . . . .±10 mA

Peak current into regulator
    switch (L pin). . . . . 150 mA

Switcher transient peak off
    voltage on L pin. +1.0 V

C4–C1, E1, CHCLK to
    AGND/DGND . . . .–0.4 V to V_{CC} + 0.4 V

Maximum power dissipation, T_A (see note) . . . . .70°C

    In 32-pin PLCC package. . . . . 1.74 W

Note: *Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165°C. The device should never be exposed to this temperature. Operation above 145°C junction temperature may degrade device reliability. See the SLIC Packaging Considerations for more information.*

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient temperature . . . . .0°C to +70°C*

V_{CC} . . . . 4.75 V to 5.25 V

V_{EE} . . . . –4.75 V to –5.25 V

V_{BAT}. . . . .–19 V to –58 V◆

AGND/DGND . . . . 0 V

BGND with respect to
    AGND/DGND. . . . . –100 mV to +100 mV

Load Resistance on VTX to ground . . . . . . 10 kΩ min

The Operating Ranges define those limits between which the functionality of the device is guaranteed.

* Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units.

◆*Can be used without switching regulator components in this range of battery voltages, provided maximum power dissipation specifications are not exceeded.*

ELECTRICAL CHARACTERISTICS

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Analog (V_{TX}) output impedance			3		Ω	4
Analog (V_{TX}) output offset	0°C to +70°C −1* −2	−35 −35 −30		+35 +35 +30	mV	
	−40°C to +85°C −1* −2	−40 −40 −35		+40 +40 +35		4
Analog (RSN) input impedance	300 Hz to 3.4 kHz		1	20	Ω	
Longitudinal impedance at A or B				35		
Overload level	4-wire 2-wire	−2.5		+2.5	Vpk	2
Transmission Performance, 2-Wire Impedance (See Test Circuit D)						
2-wire return loss	300 Hz to 3400 Hz	26			dB	4, 10
Longitudinal Balance (2-Wire and 4-Wire, See Test Circuit C); R_L = 600 Ω						
Longitudinal to metallic L-T, L-4	200 Hz to 1 kHz normal polarity 0°C to +70°C normal polarity −40°C to +85°C reverse polarity	52 63 58 54			dB	1, 2 1, 2, 4 1, 2
	1 kHz to 3.4 kHz normal polarity 0°C to +70°C normal polarity −40°C to +85°C reverse polarity	52 58 54 54				1, 2 1, 2, 4 1, 2
Longitudinal signal generation 4-L	300 Hz to 800 Hz −1* Reverse polarity −2	40 40 42				
Longitudinal current capability per wire	Active state all* OHT state all		28 18		mArms	
Insertion Loss (2- to 4-Wire and 4- to 2-Wire, See Test Circuits A and B) **BAT = −48 V, R_{LDC} = R_{LAC} = 600 Ω; BAT = −24 V, R_{LDC} = 300 Ω, R_{LAC} = 600 Ω**						
Gain accuracy	0 dBm, 1 kHz 0°C to +70°C −1* −2	−0.15 −0.15 −0.10		+0.15 +0.15 +0.10	dB	
	0 dBm, 1 kHz −40°C to +85°C −1* −2	−0.20 −0.20 −0.15		+0.20 +0.20 +0.15		— 4 —
Variation with frequency	300 Hz to 3400 Hz Relative to 1 kHz −1* 0°C to +70°C −2	−0.15 −0.15 −0.10		+0.15 +0.15 +0.10		
	300 Hz to 3400 Hz Relative to 1 kHz −1* −40°C to +85°C −2	−0.20 −0.20 −0.15		+0.20 +0.20 +0.15		— — 4

Note:
P.G. = Performance Grade

ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions (See Note 1)		Min	Typ	Max	Unit	Note
Gain tracking	0°C to +70°C +7 dBm to −55 dBm Reference: −0 dBm		−0.10		+0.10	dB	
	−40°C to +85°C +7 dBm to −55 dBm Reference: −0 dBm		−0.15		+0.15		4 4 —
Balance Return Signal (4- to 4-Wire, See Test Circuit B) **BAT = −48 V, R$_{LDC}$ = R$_{LAC}$ = 600 Ω; BAT = −24 V, R$_{LDC}$ = 300 Ω, R$_{LAC}$ = 600 Ω**							
Gain accuracy	0 dBm, 1 kHz 0°C to +70°C	 −1* −2	−0.15 −0.15 −0.10		+0.15 +0.15 +0.10	dB	— 3 —
	0 dBm, 1 kHz −40°C to +85°C	 −1* −2	−0.20 −0.20 −0.15		+0.20 +0.20 +0.15		— 3, 4 3, 4
Variation with frequency	300 Hz to 3400 Hz Relative to 1 kHz 0°C to +70°C		−0.10		+0.10		3
	300 Hz to 3400 Hz Relative to 1 kHz −40°C to +85°C		−0.15		+0.15		3 3 3, 4
Gain tracking	0°C to +70°C +3 dBm to −55 dBm Reference: 0 dBm		−0.10		+0.10		3
	−40°C to +85°C +3 dBm to −55 dBm Reference: 0 dBm		−0.15		−0.15		3, 4
Group delay	f = 1 kHz			5.3		µs	4, 12
Total Harmonic Distortion (2- to 4-Wire and 4- to 2-Wire, See Test Circuits A and B) **BAT = −48 V, R$_{LDC}$ = R$_{LAC}$ = 600 Ω**							
Harmonic distortion	0 dBm			−64	−50	dB	
300 Hz to 3400 Hz	+7 dBm			−55	−40		
Idle Channel Noise **BAT = −48 V, R$_{LDC}$ = R$_{LAC}$ = 600 Ω; BAT = −24 V, R$_{LDC}$ = 300 Ω, R$_{LAC}$ = 600 Ω**							
C-message weighted noise	2-wire, 0°C to +70°C 2-wire, −40°C to +85°C			+7	+10 +12	dBrnC	4 4
	4-wire, 0°C to +70°C 4-wire, −40°C to +85°C			+7	+10 +12		4 4
Psophometric weighted noise	2-wire, 0°C to +70°C 2-wire, −40°C to +85°C			−83	−80 −78	dBmp	— 4
	4-wire, 0°C to +70°C 4-wire, −40°C to +85°C			−83	−80 −78		— 4

Note:
*P.G. = Performance Grade

ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Single Frequency Out-of-Band Noise (See Test Circuit E)						
Metallic	4 kHz to 9 kHz 9 kHz to 1 MHz 256 kHz and harmonics**		−76 −76 −63		dBm	4 4, 5, 8 4, 5
Longitudinal	1 kHz to 15 kHz Above 15 kHz 256 kHz and harmonics**		−70 −85 −57			4 4, 5, 8 4, 5
Line Characteristics (See Figures 1a, 1b, 1c)						
Short loops, Active state	Battery = −24 V, R_{LDC} = 300 Ω Battery = −43 V, R_{LDC} = 600 Ω Battery = −48 V, R_{LDC} = 600 Ω	32.4	35.0	37.6	mA	4, 9 4 —
Long loops, Active state	Battery = −24 V, R_{LDC} = 640 Ω Battery = −43 V, R_{LDC} = 1300 Ω Battery = −48 V, R_{LDC} = 1900 Ω	20.0 23.0 18.0				4, 9 4 —
OHT state	Battery = −24 V, R_{LDC} = 600 Ω Battery = −48 V, R_{LDC} = 600 Ω	15.5	17.5	19.5		4, 9 —
Loop current	Tip Open state, R_L = 0 Disconnect state, R_L = 0			1.0		
I_LLIM (ITip and IRing)	Tip and ring shorted to GND		70	105		
Power Dissipation Battery, Normal Loop Polarity						
On-hook Open Circuit state	Battery = −24 V, w/o switching reg. Battery = −48 V, with switching reg.		30 35	75 100	mW	9 —
On-hook OHT state	Battery = −24 V, w/o switching reg. Battery = −48 V, with switching reg.	100	175 135	225		9 —
On-hook Active state	Battery = −24 V, w/o switching reg. Battery = −48 V, with switching reg.		135 180	225 300		9 —
Off-hook OHT state R_L = 50 Ω	Battery = −24 V, w/o switching reg. Battery = −48 V, with switching reg.		500 400	800 750		9 —
Off-hook Active state R_L = 50 Ω	Battery = −24 V, w/o switching reg. Battery = −48 V, with switching reg.		800 800	1100 1000		9 —
Supply Currents, Battery = −24 V or −48 V						
V_{CC} on-hook supply current	Open Circuit state OHT state Active state		3.0 6.0 7.5	4.5 10.0 12.0	mA	9
V_{EE} on-hook supply current	Open Circuit state OHT state Active state		1.0 2.2 2.7	2.3 3.5 6.0		
V_{BAT} on-hook supply current	Open Circuit state OHT state Active state		0.4 3.0 4.0	1.0 5.0 6.0		

Note:

**Applies only when switching regulator is used.

ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Power Supply Rejection Ratio (V$_{RIPPLE}$ = 50 mVrms)						
V$_{CC}$	50 Hz to 3.4 kHz 3.4 kHz to 50 kHz	25 22	45 35		dB	6
V$_{EE}$	50 Hz to 3.4 kHz 3.4 kHz to 50 kHz	20 10	40 25			
V$_{BAT}$	50 Hz to 3.4 kHz 3.4 kHz to 50 kHz	27 20	45 40			
Effective int. resistance	CAS to GND	85	170	255	kΩ	4
Off-Hook Detector						
Current threshold	I$_{DET}$ = 365/R$_D$	−20		+20	%	
Ground-Key Detector Thresholds, Active State						
Ground-key resistance threshold	Battery = −24 V, B(RING) to GND Battery = −48 V, B(RING) to GND	1.0 2.0	2.2 5.0	4.5 10.0	kΩ	9 —
Ground-key current threshold	B(RING) to GND Midpoint to GND		9 9		mA	7
Effective internal resistance	GKFIL to AGND/DGND	18	36	54	kΩ	4
Ring-Trip Detector Input						
Bias current		−5	−0.05		µA	
Offset voltage	Source resistance = 0 to 2 MΩ	−50	0	+50	mV	11
Logic Inputs (C4–C1, E0, E1, and CHCLK)						
Input High voltage		2.0			V	
Input Low voltage				0.8		
Input High current	All inputs except E1	−75		40	µA	
Input High current	Input E1	−75		45		
Input Low current		−0.4			mA	
Logic Output ($\overline{DET}$)						
Output Low voltage	I$_{OUT}$ = 0.8 mA			0.4	V	
Output High voltage	I$_{OUT}$ = −0.1 mA	2.4				
Relay Driver Outputs (RINGOUT, TESTOUT)						
On voltage	25 mA sink			+1.5	V	
Off leakage	V$_{OH}$ = +15 V			100	µA	

![Legerity logo]

RELAY DRIVER SCHEMATICS

RINGOUT

BGND

TESTOUT

BGND

15474A-002

**ON Voltage
at RINGOUT or TESTOUT
(V)**

$T_A = 70°C$

$T_A = 25°C$

Current into RINGOUT or TESTOUT (mA)
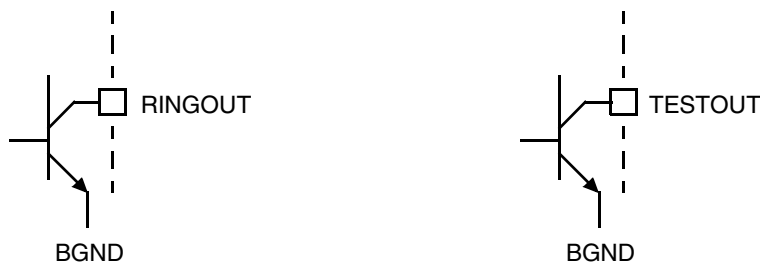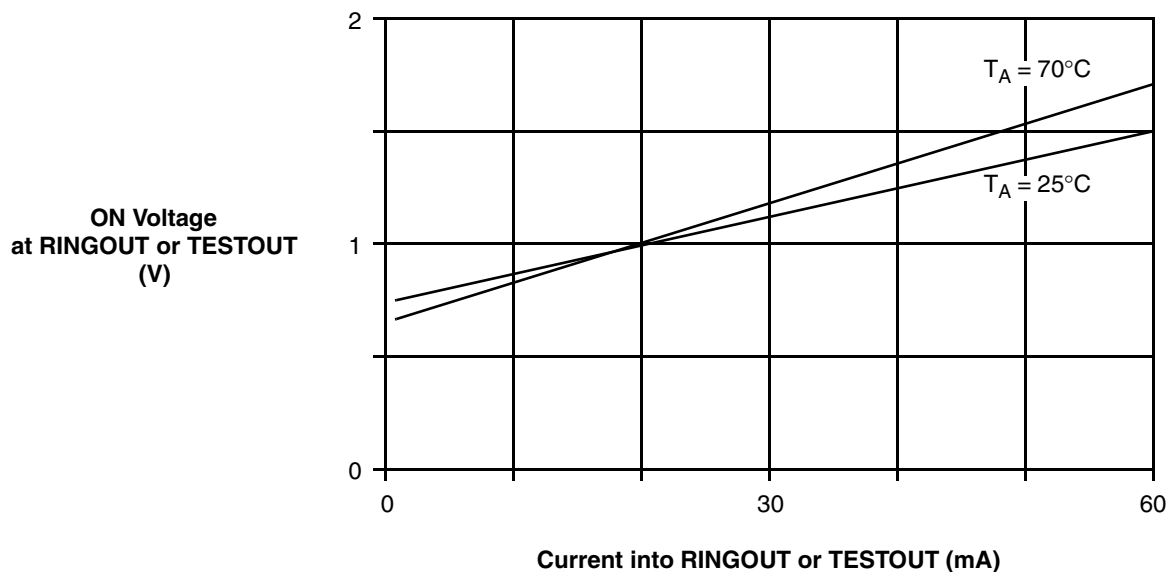
SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Conditions	Temperature Range	Min	Typ	Max	Unit	Note
tgkde	E1 Low to $\overline{DET}$ High (E0 = 1)	Ground-Key Detect state R_L open, R_G connected (See Figure H)	0°C to +70°C −40°C to +85°C			3.8 4.0		
	E1 Low to $\overline{DET}$ Low (E0 = 1)		0°C to +70°C −40°C to +85°C			1.1 1.6	µs	4
tshde	E1 High to $\overline{DET}$ Low (E0 = 1)	Switchhook Detect state R_L = 600 Ω, R_G open (See Figure G)	0°C to +70°C −40°C to +85°C			1.2 1.7		
	E1 High to $\overline{DET}$ High (E0 = 1)		0°C to +70°C −40°C to +85°C			3.8 4.0		

SWITCHING WAVEFORMS

E1 to $\overline{DET}$

E1

$\overline{DET}$

tgkde   tshde   tgkde   tshde
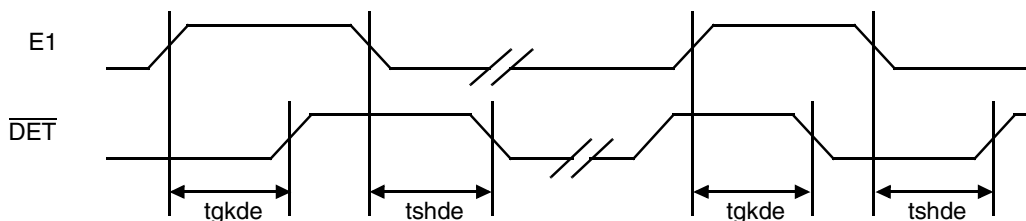
Note:
All delays measured at 1.4 V levels.

15474A-003

Notes:

1. *Unless otherwise noted, test conditions are BAT = –48 V, V_{CC} = +5 V, V_{EE} = –5 V, R_L = 600 Ω, C_{HP} = 0.33 μF, R_{DC1} = R_{DC2} = 7.14 kΩ, C_{DC} = 0.47 μF, R_D = 35.4 kΩ, C_{CAS} = 0.47 μF, no fuse resistors, R_T =120 kΩ, and R_{RX} = 60 kΩ. Switching regulator components: L = 1 mH, C_{FIL} = 0.47 μF (see Application Circuit).*

2. *Overload level is defined when THD = 1%.*

3. *Balance return signal is the signal generated at V_{TX} by V_{RX}. This specification assumes the two-wire AC load impedance matches the programmed impedance.*

4. *Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.*

5. *For frequencies below 12 kHz, these tests are performed with a longitudinal impedance of 90 Ω and metallic impedance of 300 Ω. For frequencies greater than 12 kHz, a longitudinal impedance of 90 Ω and a metallic impedance of 135 Ω is used. These tests are extremely sensitive to circuit board layout. Please refer to application notes for details.*

6. *This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.*

7. *"Midpoint" is defined as the connection point between two 300 Ω series resistors connected between A(TIP) and B(RING).*

8. *Fundamental and harmonics from 256 kHz switch regulator chopper are not included.*

9. *For –24 V battery, switching regulator is disabled. L, CHS, and VREG pins connected to VBAT pin; CHCLK pin connected to AGND/DGND.*

10. *Assumes the following Z_T network:*
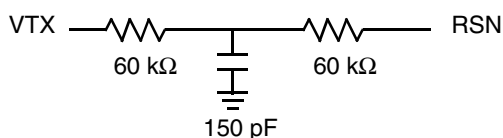
11. *Tested with 0 Ω source impedance. 2 MΩ is specified for system design purposes only.*

12. *Group delay can be considerably reduced by using a Z_T network such as that shown in Note 10 above. The network reduces the group delay to less than 2 μs. The effect of group delay on linecard performance may be compensated for by using the QSLAC™ or DSLAC™ device.*

Table 1. SLIC Decoding

State	C3	C2	C1	Two-Wire Status	$\overline{DET}$ Output E1 = 0	$\overline{DET}$ Output E1 = 1
0	0	0	0	Open Circuit	Ring trip	Ring trip
1	0	0	1	Ringing	Ring trip	Ring trip
2	0	1	0	Active	Loop detector	Ground key
3	0	1	1	On-Hook TX (OHT)	Loop detector	Ground key
4	1	0	0	Tip Open	Loop detector	—
5	1	0	1	Reserved	Loop detector	—
6	1	1	0	Active Polarity Reversal	Loop detector	Ground key
7	1	1	1	OHT Polarity Reversal	Loop detector	Ground key

Table 2.   User-Programmable Components

$Z_T = 200(Z_{2WIN} - 2R_F^*)$	Z_T is connected between the VTX and RSN pins. The fuse resistors are R_F, and Z_{2WIN} is the desired 2-wire AC input impedance. When computing Z_T, the internal current amplifier pole and any external stray capacitance between VTX and RSN must be taken into account.
$Z_{RX} = \dfrac{Z_L}{G42_L} \bullet \dfrac{200Z_T}{Z_T + 200(Z_L + 2R_F)}$	Z_{RX} is connected from V_{RX} to the R_{SN}. Z_T is defined above, and G_{42L} is the desired receive gain.
$R_{DC1} + R_{DC2} = \dfrac{500}{I_{LOOP}}$ $C_{DC} = 1.5 \text{ ms} \bullet \dfrac{R_{DC1} + R_{DC2}}{R_{DC1} \; R_{DC2}}$	R_{DC1}, R_{DC2}, and C_{DC} form the network connected to the RDC pin. R_{DC1} and R_{DC2} are approximately equal. I_{LOOP} is the desired loop current in the constant-current region.
$R_D = \dfrac{365}{I_T}, \quad C_D = \dfrac{0.5 \text{ ms}}{R_D}$	R_D and C_D form the network connected from RD to –5 V, and I_T is the threshold current between on hook and off hook.
$C_{CAS} = \dfrac{1}{3.4 \bullet 10^5 \pi f_c}$	C_{CAS} is the regulator filter capacitor, and f_c is the desired filter cut-off frequency.

Note:
R_{FUSE} = 20 Ω–50 Ω, user selectable.

DC FEED CHARACTERISTICS
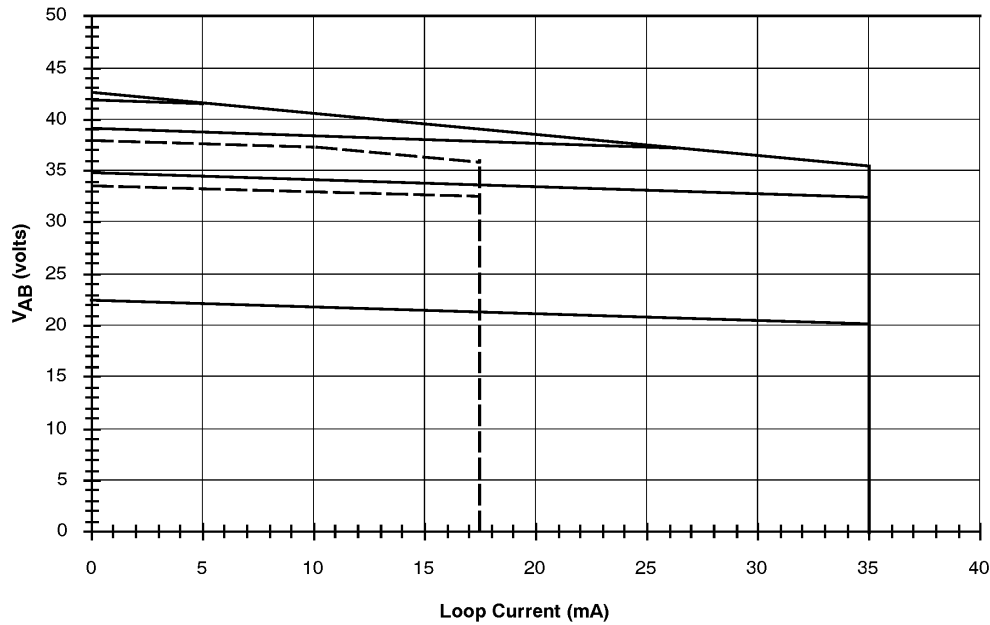
$R_{DC1} + R_{DC2} = R_{DC} = 14.28\ k\Omega$

—————— Active state

- - - - - - - OHT state

Notes:

1. *Constant-current region:*

   Active state: $\qquad I_L = \dfrac{500}{R_{DC}}$

   OHT state: $\qquad I_L = \dfrac{250}{R_{DC}}$

2. *Anti-saturation turn-on (Active state):*

   a. Battery independent: $\quad V_{AB} = 35.5\ V,\qquad\qquad (|V_{BAT}| > 46.2\ V)$

   b. Battery tracking: $\qquad V_{AB} = 1.1\ |V_{BAT}| - 15,\qquad (|V_{BAT}| \geq 46.2\ V)$
   $\qquad\qquad\qquad\qquad\quad V_{AB} = 0.7\ |V_{BAT}| + 3.5,\qquad (|V_{BAT}| < 46.2\ V)$

3. *Open circuit voltage:*

   Active state: $\qquad V_{AB} = 42.6,\qquad\qquad\qquad (|V_{BAT}| > 53\ V)$
   $\qquad\qquad\qquad\quad V_{AB} = 0.7\ |V_{BAT}| + 5.89,\qquad (|V_{BAT}| \leq 53\ V)$

   OHT state, $\qquad V_{AB} = 39.1,\qquad\qquad\qquad (|V_{BAT}| > 49.8\ V)$
   $\qquad\qquad\qquad\quad V_{AB} = 0.7\ |V_{BAT}| + 4.7,\qquad (|V_{BAT}| \leq 49.8\ V)$

4. *Anti-saturation 1 region:*

   Active state: $\qquad V_{AB} = 46.2 - I_L\left(\dfrac{R_{DC}}{70.4}\right)$

   OHT state: $\qquad V_{AB} = 39.1 - I_L\left(\dfrac{R_{DC}}{70.4}\right)$

5. *Anti-saturation 2 region:*

   Active state: $\qquad V_{AB} = 0.7|V_{BAT}| + 5.89 - I_L\left(\dfrac{R_{DC}}{210}\right)$

   OHT state: $\qquad V_{AB} = 0.7|V_{BAT}| + 4.7 - I_L\left(\dfrac{R_{DC}}{210}\right)$

a. V_A–V_B (V_{AB}) Voltage vs. Loop Current (Typical)

DC FEED CHARACTERISTICS (continued)
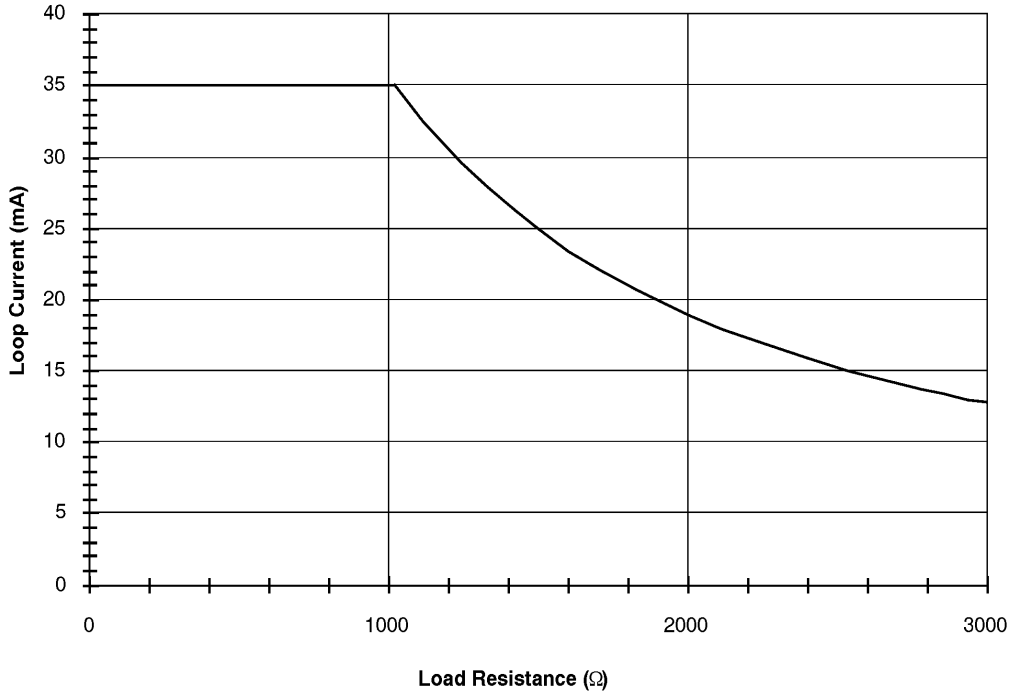
$R_{DC1} + R_{DC2} = R_{DC} = 14.28$ kΩ

$V_{BAT} = 47.3$ V

b. Loop Current vs. Load Resistance (Typical)
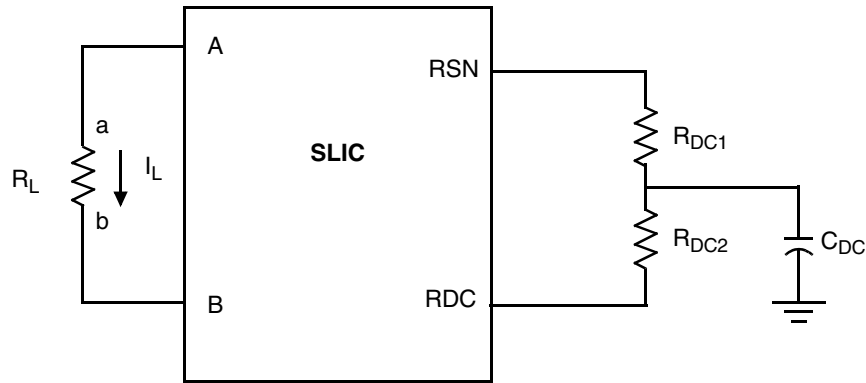
Feed current programmed by R_{DC1} and R_{DC2}

c. Feed Programming

15474A-004

Figure 1. DC Feed Characteristics

TEST CIRCUITS

$$I_{L2\text{-}4} = -20 \log (V_{TX} / V_{AB})$$
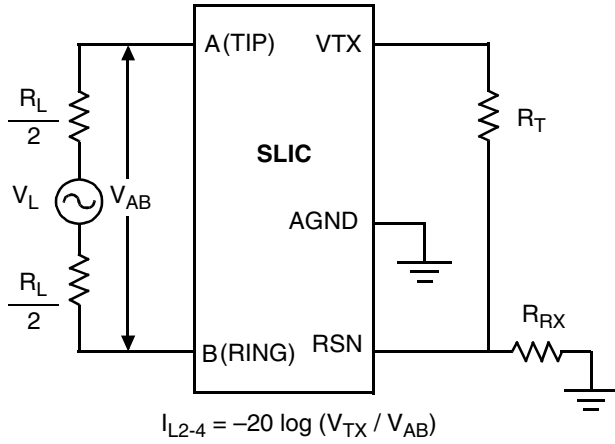
A. Two- to Four-Wire Insertion Loss

$$I_{L4\text{-}2} = -20 \log (V_{AB} / V_{RX})$$
$$BRS = 20 \log (V_{TX} / V_{RX})$$
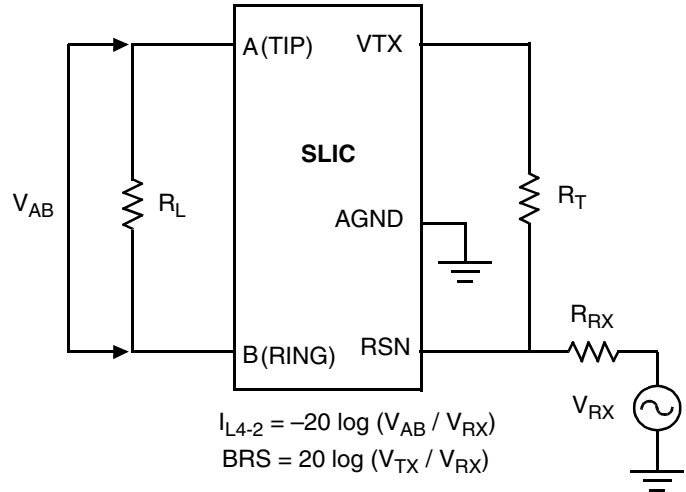
B. Four- to Two-Wire Insertion Loss and Balance Return Signal

S2 Open, S1 Closed:

L-T Long. Bal. = $20 \log (V_{AB} / V_L)$

L-4 Long. Bal. = $20 \log (V_{TX} / V_L)$

S2 Closed, S1 Open:

4-L Long. Sig. Gen. = $20 \log (V_L / V_{RX})$

C. Longitudinal Balance

Note:
Z_D is the desired impedance (e.g., the characteristic impedance of the line).

$$R_L = -20 \log (2 V_M / V_S)$$
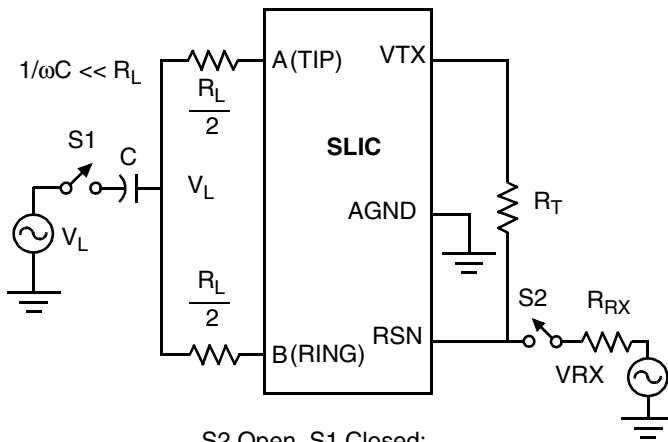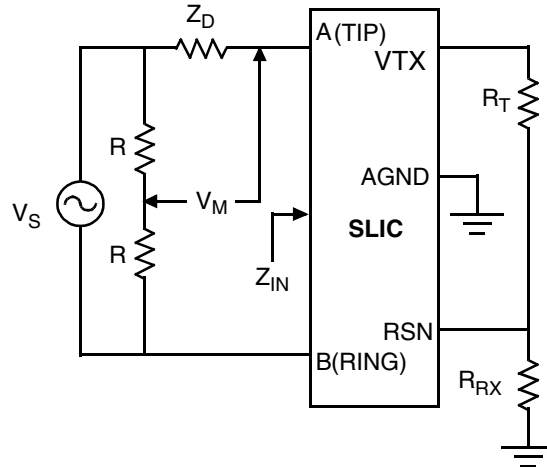
D. Two-Wire Return Loss Test Circuit

TEST CIRCUITS (continued)
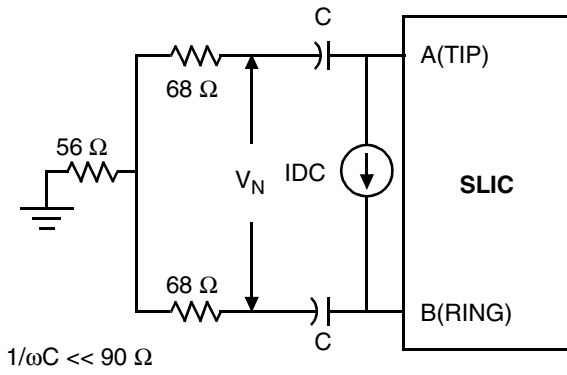
E. Single-Frequency Noise
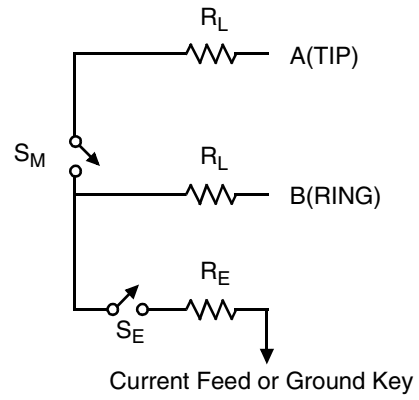
F. Ground-Key Detection Center Point Test
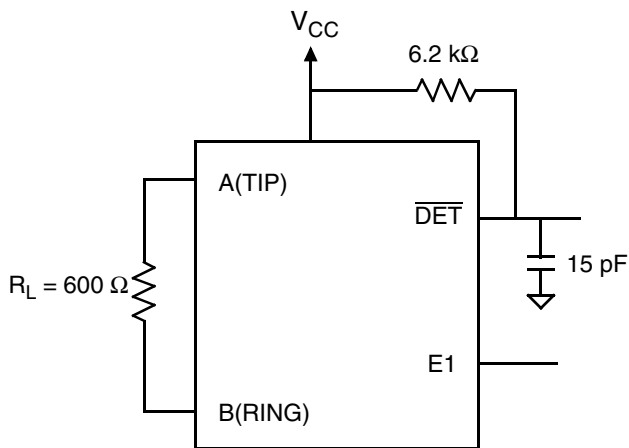
G. Loop-Detector Switching
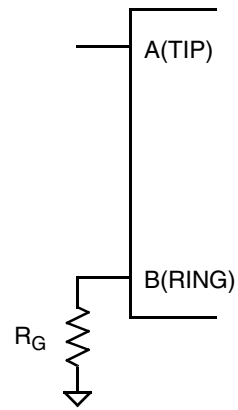
R_G: 2 kΩ at V_{BAT} = −48 V
1 kΩ at V_{BAT} = −24 V

H. Ground-Key Switching

PHYSICAL DIMENSIONS

PL032

TOP VIEW

SIDE VIEW
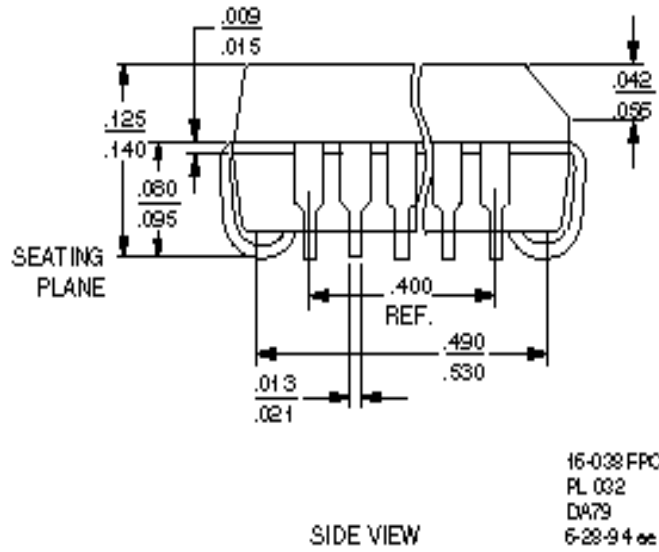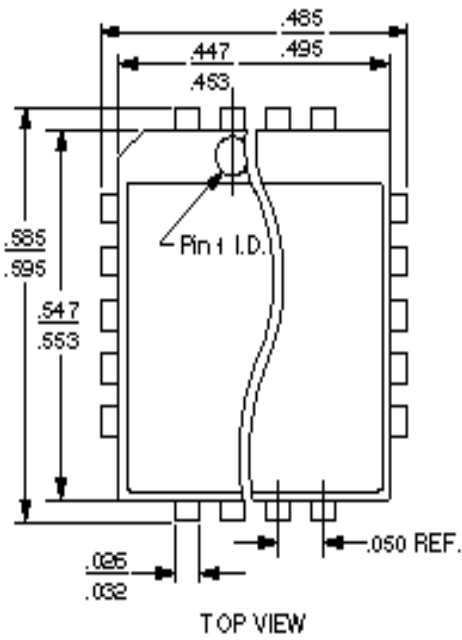
16-038 FPO-5
PL 032
DA79
6-28-94 ac

REVISION SUMMARY

Revision C to Revision D

- Minor changes were made to the data sheet style and format to conform to Legerity standards.

- Table 1—Some information in the table was revised, including the addition of the Reserved status.

Revision D to Revision E

- Minor changes were made to the data sheet style and format to conform to Legerity standards.

- In the Pin Description table, the TP pin description was inserted/changed to: "Thermal pin. Connection for heat dissipation. Internally connected to substrate (QBAT). Leave as open circuit or connected to QBAT. In both cases, the TP pins can connect to an area of copper on the board to enhance heat dissipation."

Revision E to Revision F

- The physical dimension (PL032) was added to the Physical Dimensions section.

- Deleted the Ceramic DIP and Plastic DIP packages and references to them.

- Updated the Pin Description table to correct inconsistencies.

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