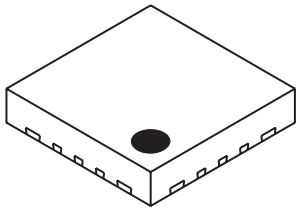
SONY

CXG1171UR

High Power SP4T Switch with Logic Control

20 pin UQFN (Plastic)



Description

This IC can be used in wireless communication systems, for example, W-CDMA handsets.

The IC has on-chip logic for operation with 5 CMOS control inputs.

The Sony JPHEMT process is used for low insertion loss and on-chip logic circuit.

Features

- Low insertion loss
- 5 CMOS compatible control line
- Small package size: 20-pin UQFN

Applications

Antenna switch for cellular handsets
W-CDMA

Structure

GaAs JPHEMT MMIC

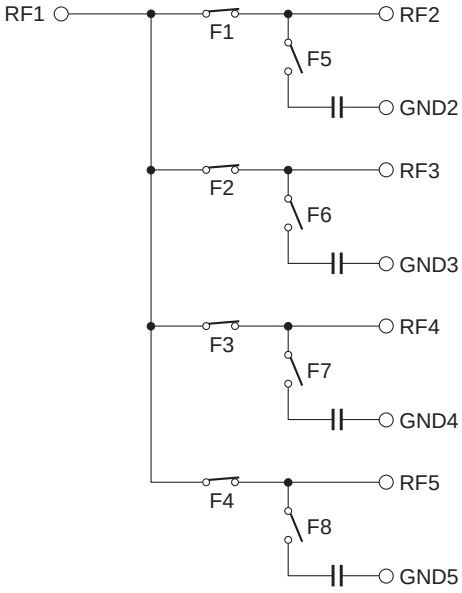
Absolute Maximum Ratings (Ta = 25°C)

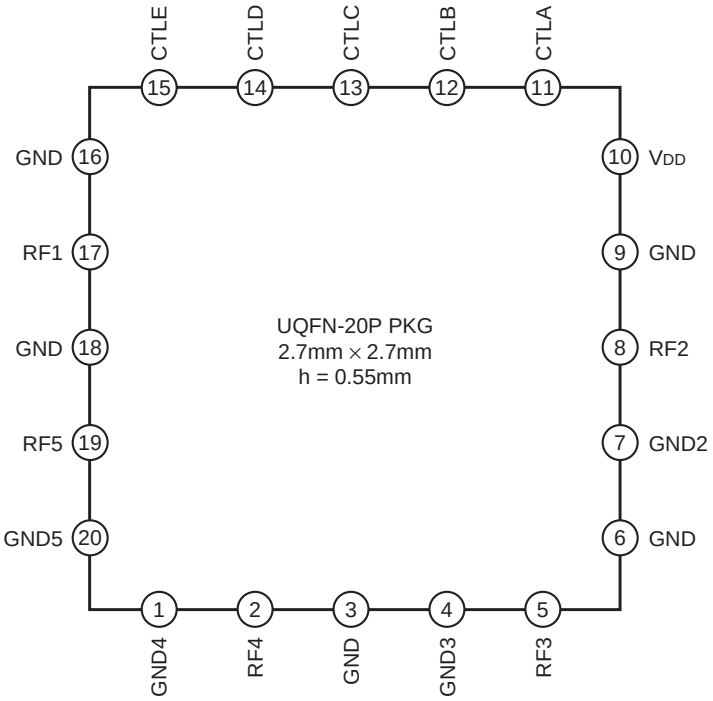
• Bias voltage	V_{DD}	7	V
• Control voltage	Vctl	5	V
• Operation temperature	Topr	–35 to +85	°C
• Storage temperature	Tstg	–65 to +150	°C

GaAs MMIC's are ESD sensitive devices. Special handling precautions are required.

E03Y13-PS

Block Diagram and Recommended Circuit





Truth Table

State	ON Pass	CTLA	CTLB	CTLC	CTLD	CTLE	F1	F2	F3	F4	F5	F6	F7	F8
1	RF1 – RF2	H H H	H/L H L	H H L	L L H	L H L	ON	OFF	OFF	OFF	OFF	ON	ON	ON
2	RF1 – RF3	H H	H L	L L	H/L H/L	H/L H	OFF	ON	OFF	OFF	ON	OFF	ON	ON
3	RF1 – RF4	H H H	H/L L L	H H L	H L L	H/L H L	OFF	OFF	ON	OFF	ON	ON	OFF	ON
4	RF1 – RF5	L	H/L	H/L	H/L	H/L	OFF	OFF	OFF	ON	ON	ON	ON	OFF

DC Bias Condition (Ta = 25°C)

Item	Min.	Typ.	Max.	Unit
Vctl (H)	2.0	2.85	3.6	V
Vctl (L)	0	—	0.4	V
V_{DD}	2.5	2.85	3.6	V

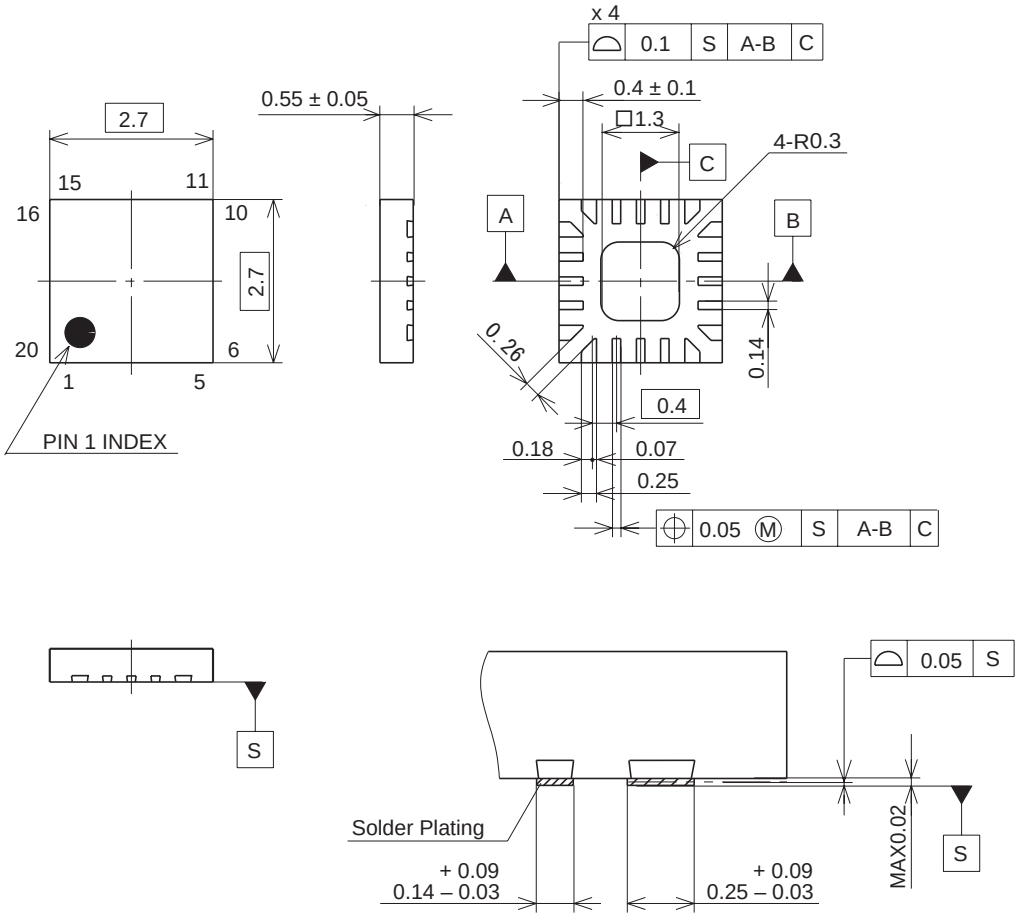
Electrical Characteristics (Ta = 25°C)

Item	Symbol	State	Condition	Min.	Typ.	Max.	Unit
Insertion loss	IL	1	RF1 – RF2, 1920 to 1980MHz		0.35	0.60	dB
			2110 to 2170MHz		0.40	0.65	dB
		2	RF1 – RF3, 1920 to 1980MHz		0.35	0.60	dB
			2110 to 2170MHz		0.40	0.65	dB
		3	RF1 – RF4, 1920 to 1980MHz		0.35	0.60	dB
			2110 to 2170MHz		0.40	0.65	dB
		4	RF1 – RF5, 1920 to 1980MHz		0.80	1.10	dB
			2110 to 2170MHz		0.85	1.15	dB
Isolation	ISO.	2, 3	RF1 – RF2, 1920 to 2170MHz	30	35		dB
		1, 3	RF1 – RF3, 1920 to 2170MHz	30	35		dB
		1, 2	RF1 – RF4, 1920 to 2170MHz	30	35		dB
		1, 2, 3	RF1 – RF5, 1920 to 2170MHz	20	25		dB
		4	RF1 – RF2, 3, 4, 1920 to 2170MHz	25	30		dB
VSWR	VSWR		50Ω		1.2		—
Switching speed	TSW				4	10	µs
ACLR	ACLR1		±5MHz, 3.84MHz BW, *1		–60	–50	dBc
	ACLR2		±10MHz, 3.84MHz BW, *1		–62	–55	dBc
Harmonics	2fo		*1		–75	–60	dBc
	3fo		*1		–75	–60	dBc
Bias current	I_{DD}		V_{DD} = 2.85V		0.20	0.35	mA
Control current	Ictl		Vctl (H) = 2.85V		15	25	µA

*1 Pin = 25dBm, 0/2.85V control, V_{DD} = 2.85V, 1920 to 1980MHz

Package Outline Unit: mm

20PIN UQFN（PLASTIC）



TERMINAL SECTION

Note:Cutting burr of lead are 0.05mm MAX.

SONY CODE	UQFN-20P-01
EIAJ CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.02g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18µm