

64 K × 1 High Speed CMOS SRAM

Introduction

The HM 65787 is a high speed CMOS static RAM organized as 65536 × 1 bit. It is manufactured using MHS's high performance CMOS technology.

Access times as fast as 15 ns are available with maximum power consumption of only 495 mW.

The HM 65787 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 60 % when the circuit is deselected.

Easy memory expansion is provided by an active low chip select (CS) and three state drivers.

All inputs and outputs of the HM 65787 are TTL compatible and operate from single 5V supply thus simplifying system design.

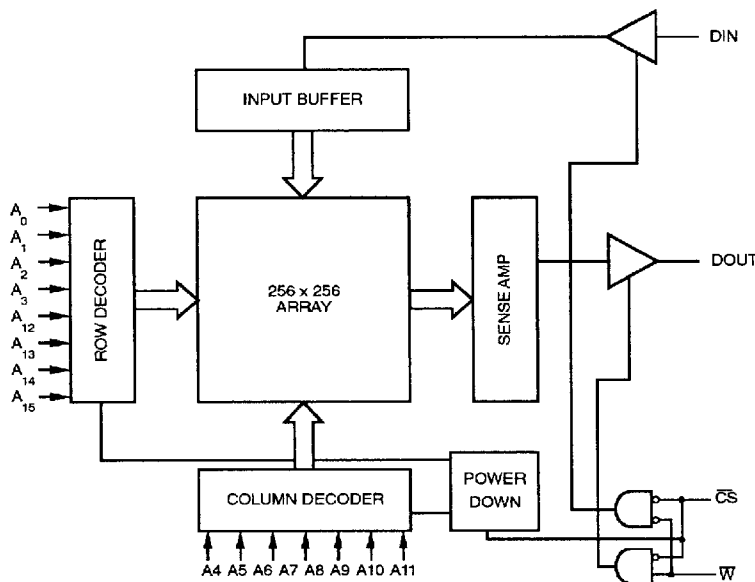
The HM 65787 is processed following the test methods of MIL STD 883.

Features

- Fast access time
Commercial : 15/20/25/35/45 ns
Industrial military : 20/25/35/45/55 ns
- Low power consumption
Active : 320 mW (typ)
Standby : 75 mW (typ)
- Wide temperature range :
-55°C to + 125°C
- 300 mils width package
- TTL compatible inputs and outputs
- Asynchronous
- Capable of withstanding greater than 2000 V electrostatic discharge
- Single 5 volt supply

Interface

Block Diagram

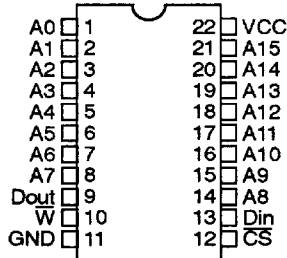


HM 65787

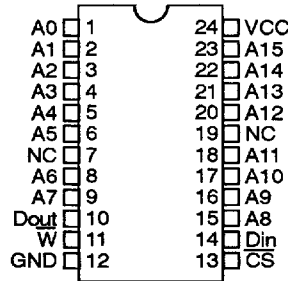
Pin Configuration

Plastic 300 mils, 22 pins, DIL
Ceramic 300 mils, 22 pins, DIL

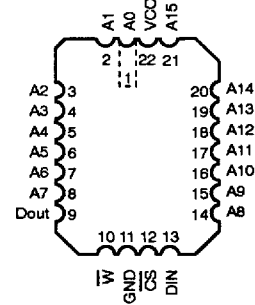
SOIC & SOJ 300 mils, 24 pins



Pinout DIL 22 pins (top view)

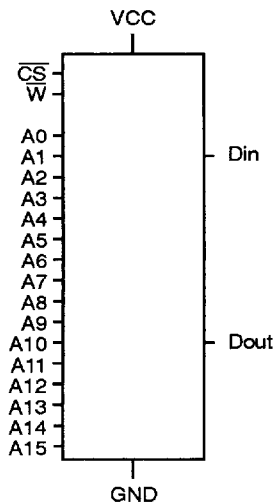


Pinout SOIC/SOJ 24 pins



Pinout LCC 22 pins (top view)

Logic Symbol



Pin Names

| | |
|--|-------------------------------|
| A ₀ -A ₁₅ : Address inputs | \overline{W} : Write enable |
| Din : Input | Vcc : Power |
| Dout : Output | GND : Ground |
| \overline{CS} : Chip Select | |

Truth Table

| \overline{CS} | \overline{W} | DATA-IN | DATA-OUT | MODE |
|-----------------|----------------|---------|----------|----------|
| H | X | Z | Z | Deselect |
| L | H | Z | Valid | Read |
| L | L | Valid | Z | Write |

L = Low - H = High, X = H or L, Z = High impedance.

Electrical Characteristics

Absolute Maximum Ratings

| | | | |
|---|------------------|---|--|
| Supply voltage to GND potential : | -0.5 V to +7.0 V | Storage temperature : | -65°C to +150°C |
| DC input voltage : | -3.0 V to +7.0 V | Output current into outputs (low) : | 20 mA |
| DC output voltage in high Z state : | -0.5 V to +7.0 V | Electro Static Discharge Voltage | > 2000 V (MIL STD 883C METHOD 3015-2) |

Operating Range

| | | OPERATING VOLTAGE | OPERATING TEMPERATURE |
|------------|-------|-------------------|-----------------------|
| Military | (- 2) | 5 V ± 10 % | - 55°C to + 125°C |
| Industrial | (- 9) | 5 V ± 10 % | - 40°C to + 85°C |
| Commercial | (- 5) | 5 V ± 10 % | 0°C to + 70°C |

Recommended DC Operating Conditions

| PARAMETER | DESCRIPTION | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|-----------|--------------------|---------|---------|---------|------|
| Vcc | Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| Gnd | Ground | 0.0 | 0.0 | 0.0 | V |
| VIL | Input low voltage | - 3.0 | 0.0 | 0.8 | V |
| VIH | Input high voltage | 2.2 | - | 5.5 | V |

Capacitance

| PARAMETER | DESCRIPTION | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|-----------|--------------------|---------|---------|---------|------|
| Cin (1) | Input capacitance | - | - | 5 | pF |
| Cout (1) | Output capacitance | - | - | 7 | pF |

Note : 1. TA = 25°C, f = 1 MHz, Vcc = 5.0 V. These parameters are not 100 % tested.

DC Parameters

| PARAMETER | DESCRIPTION | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|-----------|------------------------------|---------|---------|---------|------|
| IIX (2) | Input leakage current | - 10.0 | - | 10.0 | µA |
| IOZ (3) | Output leakage current | - 10.0 | - | 10.0 | µA |
| IOS (3) | Output short circuit current | - | - | - 350.0 | mA |
| VOL (4) | Output low voltage | - | - | 0.4 | V |
| VOH (5) | Output high voltage | 2.4 | - | - | V |

- Note :
2. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.
 3. Vcc = max, Vout = Gnd, duration of the short circuit should not exceed 30 seconds.
 4. Vcc min, IOL = 12.0 mA (commercial) 8.0 mA (military).
 5. Vcc min, IOH = -4.0 mA.

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Consumption for Commercial (-5) Specification

| SYMBOL | PARAMETER | 65787 E-5 | 65787 F-5 | 65787 H-5 | 65787 K-5 | 65787 M-5 | UNIT | VALUE |
|------------|---------------------------|--------------|--------------|--------------|--------------|--------------|------|-------|
| ICCSB (6) | Standby supply current | 40 | 40 | 30 | 30 | 30 | mA | max |
| ICCSB1 (7) | Standby supply current | 20 | 20 | 20 | 20 | 20 | mA | max |
| ICCOP (8) | Dynamic operating current | 90 | 80 | 80 | 80 | 80 | mA | max |

Consumption for Industrial (-9) and Military (-2) Specification

| SYMBOL | PARAMETER | 65787 F-9/-2 | 65787 H-9/-2 | 65787 K-9/-2 | 65787 M-9/2 | 65787 N-9/-2 | UNIT | VALUE |
|------------|---------------------------|-----------------|-----------------|-----------------|----------------|-----------------|------|-------|
| ICCSB (6) | Standby supply current | 40 | 40 | 30 | 30 | 30 | mA | max |
| ICCSB1 (7) | Standby supply current | 20 | 20 | 20 | 20 | 20 | mA | max |
| ICCOP (8) | Dynamic operating current | 90 | 80 | 80 | 80 | 80 | mA | max |

- Note :
- $\overline{CS} \geq V_{IH}$ min duty cycle = 100 %, a pull-up resistor to Vcc on the CS input is required to keep the device deselected during Vcc power-up otherwise ICCSB will exceed values given above.
 - $\overline{CS} = V_{cc} - 0.3$ V Iout = 0 mA.
 - Vcc max, Output current = 0 mA, f = max, Vin = Vcc or Gnd.

AC Parameters

AC Conditions

Input pulse levels : Gnd to 3.0 V Input timing reference levels : 1.5 V
 Input rise : 5 ns Output loading IOL/IOH (see figure 1a) : +30 pF

AC Test Loads and Waveforms

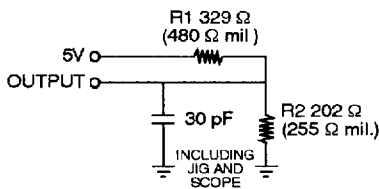


Figure 1
a

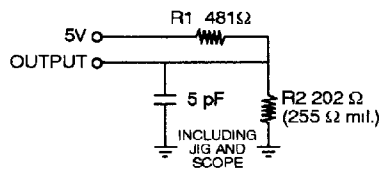


Figure 1 b

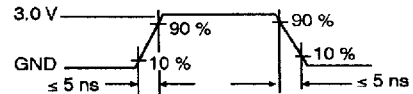
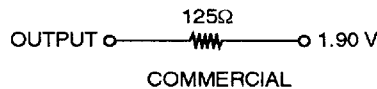
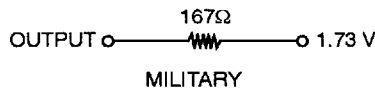


Figure 2

Equivalent to : THEVENIN EQUIVALENT



Write Cycle : Commercial (-5) Specification

| SYMBOL | PARAMETER | 65787 E-5 | 65787 F-5 | 65787 H-5 | 65787 K-5 | 65787 M-5 | UNIT | VALUE |
|-----------|----------------------------------|--------------|--------------|--------------|--------------|--------------|------|-------|
| TAVAV | Write cycle time | 15 | 20 | 20 | 25 | 40 | ns | min |
| TAVWL | Address set-up time | 0 | 0 | 0 | 0 | 0 | ns | min |
| TAVWH | Address valid to end of write | 12 | 15 | 20 | 25 | 30 | ns | min |
| TDVWH | Data set-up time | 10 | 10 | 10 | 15 | 15 | ns | min |
| TELWH | \overline{CS} low to write end | 12 | 15 | 20 | 25 | 30 | ns | min |
| TWLQZ(8) | Write low to high Z | 7 | 7 | 7 | 10 | 15 | ns | max |
| TWLWH | Write pulse width | 12 | 15 | 15 | 20 | 20 | ns | min |
| TWHAX | Address hold from end of write | 0 | 0 | 0 | 0 | 0 | ns | min |
| TWHDX | Data hold time | 0 | 0 | 0 | 0 | 0 | ns | min |
| TWHQX (8) | Write high to low Z | 5 | 5 | 5 | 5 | 5 | ns | min |

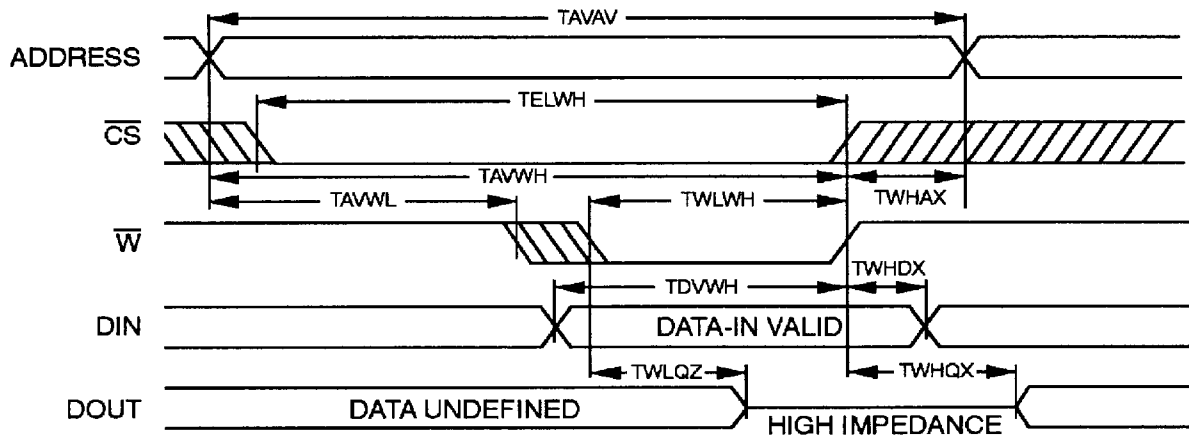
Write Cycle : Industrial (-9) and Military (-2) Specification

| SYMBOL | PARAMETER | 65787 F-9/-2 | 65787 H-9/-2 | 65787 K-9/-2 | 65787 M-9/-2 | 65787 N-9/-2 | UNIT | VALUE |
|-----------|----------------------------------|-----------------|-----------------|-----------------|-----------------|-----------------|------|-------|
| TAVAV | Write cycle time | 20 | 20 | 25 | 40 | 50 | ns | min |
| TAVWL | Address set-up time | 0 | 0 | 0 | 0 | 0 | ns | min |
| TAVWH | Address valid to end of write | 15 | 20 | 25 | 30 | 40 | ns | min |
| TDVWH | Data set-up time | 10 | 10 | 15 | 15 | 20 | ns | min |
| TELWH | \overline{CS} low to write end | 15 | 20 | 25 | 30 | 40 | ns | min |
| TWLQZ(8) | Write low to high Z | 7 | 7 | 10 | 15 | 15 | ns | max |
| TWLWH | Write pulse width | 15 | 15 | 20 | 20 | 25 | ns | min |
| TWHAX | Address hold from end of write | 0 | 0 | 0 | 0 | 0 | ns | min |
| TWHDX | Data hold time | 0 | 0 | 0 | 0 | 0 | ns | min |
| TWHQX (8) | Write high to low Z | 5 | 5 | 5 | 5 | 5 | ns | min |

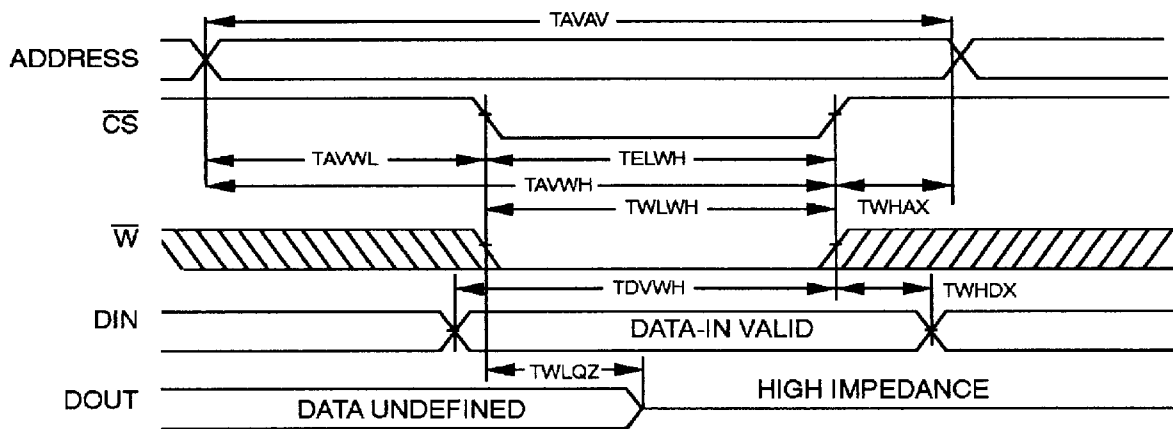
Note : 8. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

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Write Cycle 1 (\overline{W} Controlled)



Write Cycle 2 (\overline{CS} controlled)



Read Cycle : Commercial (-5) Specification

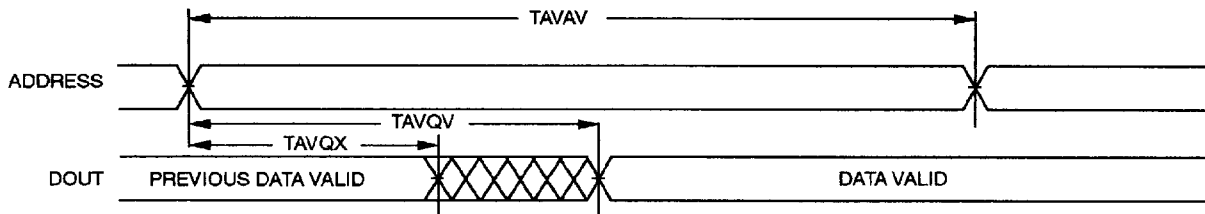
| SYMBOL | PARAMETER | 65787 E-5 | 65787 F-5 | 65787 H-5 | 65787 K-5 | 65787 M-5 | UNIT | VALUE |
|--------|------------------------------------|--------------|--------------|--------------|--------------|--------------|------|-------|
| TAVAV | Read cycle time | 15 | 20 | 25 | 35 | 45 | ns | min |
| TAVQV | Address access time | 15 | 20 | 25 | 35 | 45 | ns | max |
| TAVQX | Address valid to low Z | 3 | 3 | 3 | 3 | 3 | ns | min |
| TELQV | Chip-select access time | 15 | 20 | 25 | 35 | 45 | ns | max |
| TELQX | \overline{CS} low to low Z | 5 | 5 | 5 | 5 | 5 | ns | min |
| TEHQZ | \overline{CS} high to high Z | 8 | 8 | 10 | 15 | 15 | ns | max |
| TELIC | \overline{CS} low to power up | 0 | 0 | 0 | 0 | 0 | ns | min |
| TEHICL | \overline{CS} high to power down | 15 | 20 | 20 | 20 | 25 | ns | max |

Read Cycle : Industrial (-9) and Military (-2) Specification

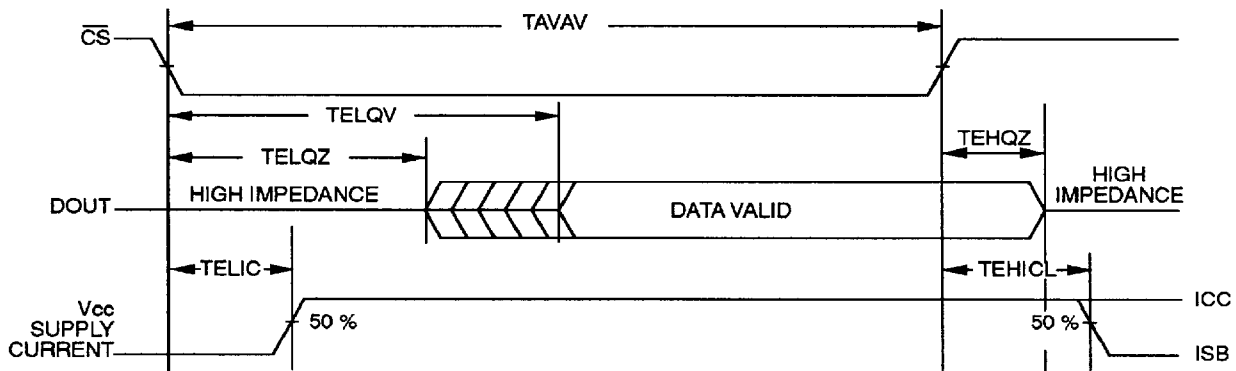
| SYMBOL | PARAMETER | 65787 F-9/-2 | 65787 H-9/-2 | 65787 K-9/-2 | 65787 M-9/-2 | 65787 N-9/-2 | UNIT | VALUE |
|--------|------------------------------------|-----------------|-----------------|-----------------|-----------------|-----------------|------|-------|
| TAVAV | Read cycle time | 20 | 25 | 35 | 45 | 55 | ns | min |
| TAVQV | Address access time | 20 | 25 | 35 | 45 | 55 | ns | min |
| TAVQX | Address valid to low Z | 3 | 3 | 3 | 3 | 3 | ns | min |
| TELQV | Chip-select access time | 20 | 25 | 35 | 45 | 55 | ns | min |
| TELQX | \overline{CS} low to low Z | 5 | 5 | 5 | 5 | 5 | ns | min |
| TEHQZ | \overline{CS} high to high Z | 8 | 10 | 15 | 15 | 20 | ns | min |
| TELIC | \overline{CS} low to power up | 0 | 0 | 0 | 0 | 0 | ns | min |
| TEHICL | \overline{CS} high to power down | 20 | 20 | 20 | 25 | 30 | ns | min |

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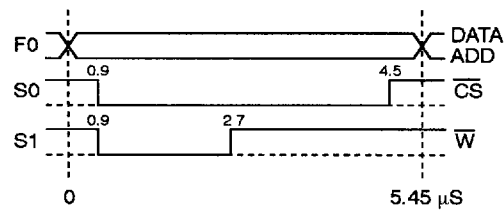
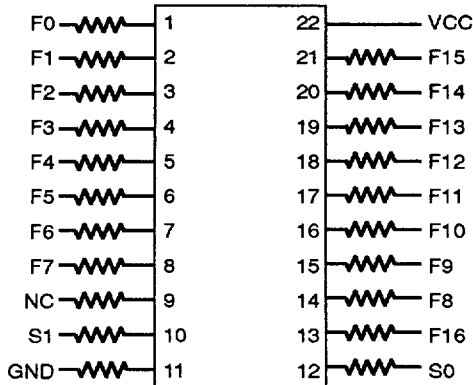
Read Cycle nb 1



Read Cycle nb 2



Burn-In Schematics



VCC = 5 V (- 0, + 0.5)

R = 1 kΩ per pin

FO = 91.6 KHz ± 20 %

F_n = 1/2 F_{n-1}

S0 & S2 : programmable signals for write/read cycles

NC = Non connected.

Ordering Information

| PACKAGE | | DEVICE | GRADE | LEVEL |
|------------------------------|----------|--------------------------------|-----------|----------------------------------|
| HM | 3 | 65787 | F | -5 : R |
| | | 64 k × 1 high speed static RAM | | |
| 0 - Chip form | | | E = 15 ns | -2 : Military |
| 1 - Ceramic 22 pins 300 mils | | | F = 20 ns | -5 : Commercial |
| 3 - Plastic 22 pins 300 mils | | | H = 25 ns | -6 : 100% 25°C Probe |
| 4 - LCC 22 pins rectangular | | | K = 35 ns | -9 : Industrial |
| T-SOIC 24 pins 300 mils | | | M = 45 ns | /883 : MIL STD 883 Class B or S |
| U - SOJ 24 pins 300 mils | | | N = 55 ns | DB : Dice Military program |
| | | | | R : Tape & Reel option |
| | | | | RD : Tape & Reel/Dry pack option |
| | | | | D : Dry pack option |

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