INNOVATIVE SILICON TECHNOLOGY™

HCMOS CONTINUOUS ARRAYS™

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SGS-THOMSON MICROELECTRONICS

GENERAL DESCRIPTION

The ISB18000 CONTINUOUS ARRAY series uses a high performance, double level metal HCMOS process to achieve sub-nanosecond internal speeds, while, at the same time offering high current, up to 24 mA, off chip drive capability. The total gate count ranges from 2,500 to 21,000 wireable 2-input NAND gates. The high current I/O cell counts range from 68 to 196 full function cells. The output buffers have a drive strength which is capable of sinking up to 24 mA. In addition, each high drive I/O cell macro has a slew rate control pin that can be used as a logical connection so as to provide a means of programmability. Most of the internal macros are designed with double drive output devices to reduce the delay times of critical paths.

A wide range of CAD tools are combined into the design system which allow designs to be developed on multiple workstations. The high density internal core, continuous array architecture, using transistor isolation, is the identical approach used with the previous ISB12000 series. An extensive package offering makes this series well suited for a broad range of high performance bus buffering applications. The product technology may be used in commercial, industrial and military environments.

FEATURES

- Output buffers capable of driving ISA, EISA, MCA, and SCSI interface levels.
- 2 - input NAND delay of 0.4 ns (typ) with fanout = 2
- 0.8 micron HCMOS process, with a polysilicide gate, and double level metal with a titanium barrier.
- CONTINUOUS ARRAY architecture utilizing transistor gate isolation.
- Broad range of Macrocell elements that are compatible with the ISB9000/12000.
- Usable gate counts ranging from 2,500 to 21,000.
- Full function TTL and compatible high drive I/O cells capable of sinking up to 24 mA of DC current.
- Slew rate control programmability.
- Independent power supply distribution to the high power output drive transistors.
- CONCERT design system with interfaces from multiple workstations.
- Latchup trigger current > +/- 500 mA. ESD protection > +/- 2000 volts.

PRODUCT RANGE

Device Name	Internal Cells	Total (1) Gates	Estimated (2) Useable Gates	Total (3) Device Pads	Power Pads	Maximum (4) I/O
ISB18006	16,200	6,480	2,592	80	12	68
ISB18010	24,200	9,680	3,872	96	12	84
ISB18013	33,800	13,500	5,400	112	12	100
ISB18018	45,000	18,000	7,200	128	12	116
ISB18026	64,800	25,920	10,368	152	16	136
ISB18032	80,000	32,000	12,800	168	16	152
ISB18042	105,800	42,320	16,928	192	20	172
ISB18054	135,200	54,080	21,632	216	20	196

Notes:
1. A factor of 2.5 is used to derive gate complexity from internal cells.
2. A conservative routing efficiency of 40% is estimated. This number will vary depending on the design.
3. Eight corner pads are dedicated V_{DDEXT}/V_{SSEXT} pads. I/O pads may be reconfigured for additional V_{DD}/V_{SS} pads.
4. Maximum I/O = Total device pads less Power pads

The ISB18000 high current I/O buffers are located on the periphery of the array. Figure 3 is a plot of a high drive I/O buffer. The I/O cell consists of a bond pad with input protection and transmission line diode clamps, large n-channel transistors that can sink up to 24 mA of current, and a receiver/pre-driver/slew rate control section. Every high drive I/O cell may be configured as input, output, or bidirectional circuit.

ARCHITECTURE

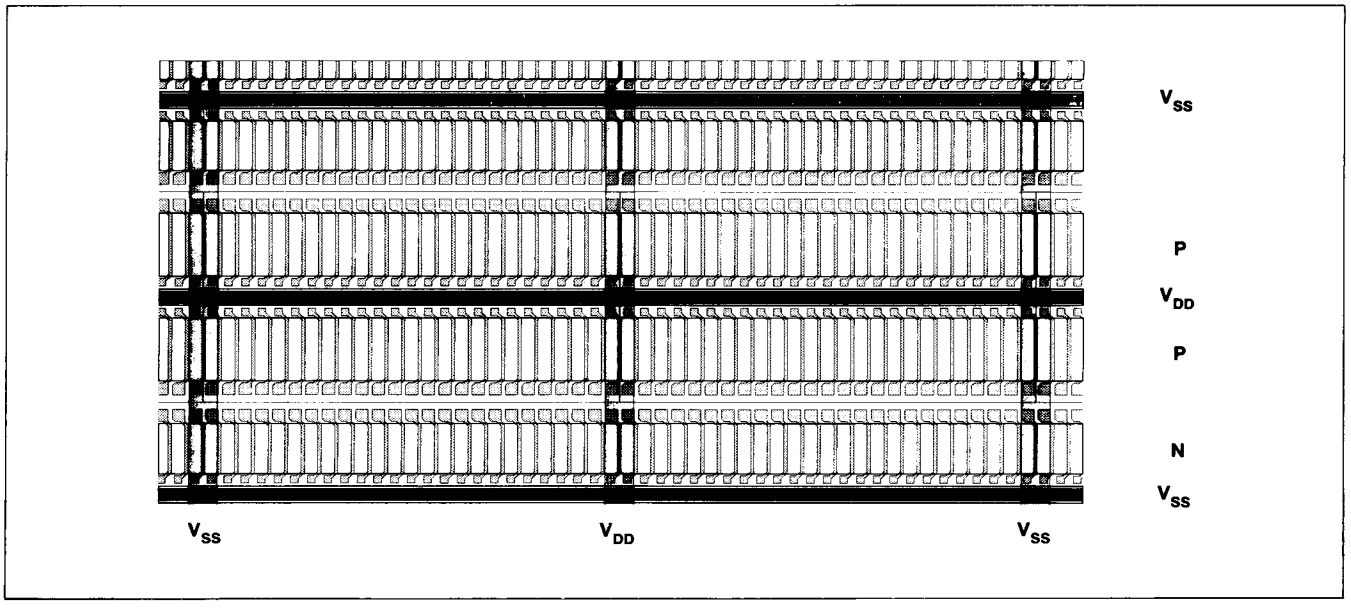
The CONTINUOUS ARRAY™ architecture, as previously used with the ISB12000 technology, provides the ISB18000 with a core that is completely filled with potentially active transistors. Surrounding the core are the configurable I/O cells, V_{DD} and V_{SS} pads occupying pre-established locations. The ISB18000 allows the signal routing over unused transistors as needed rather than routing pre-established transistor free channels as in conventional arrays. The basic cell is a pair of N and P transistors that are vertically arranged. The width of the P transistor is larger than the N transistor thereby providing improved symmetry between the rise and fall times of the macrocells. The basic cells are placed adjacent to each other without field isolation to form a multiple column row. Adjacent basic cells may be uniquely wired together to form a variety of macrocells. Isolation between macrocells is accomplished by placing the endmost basic cell in the cutoff state, thus providing flexibility and space efficiency. Each basic cell has 12 horizontal wiring channels on first metal and 1 vertical wiring channel on second metal. All wiring internal to the macrocell is done on first metal. Careful attention has been given in each macrocell layout to provide multiple target locations to avoid interference with second metal power busses and for ease of global routing.

As can be seen from Figure 1, the first metal V_{DD} and V_{SS} power lines run horizontally on the top and bottom of each row. Every other row is flipped relative to the previous row thereby allowing the sharing of supply lines between adjacent rows. Additionally, a 2 column wide vertical power screen is provided every 25 columns on second metal. Finally, a third augmented power grid is provided for the larger arrays. This wide grid is designed to maintain signal integrity, noise margin and improve delay equation tolerance in extreme conditions.

MACROCELLS AND MACROFUNCTIONS

The ISB18000 series has internal macrocells that are robust in variety and performance. Specialized cells for scan techniques and a mix of complex logic functions round off the SSI offering. High drive, double output power versions, which may be used to speed up critical paths, are available for most internal macrocells.

Figure 1. Internal Matrix



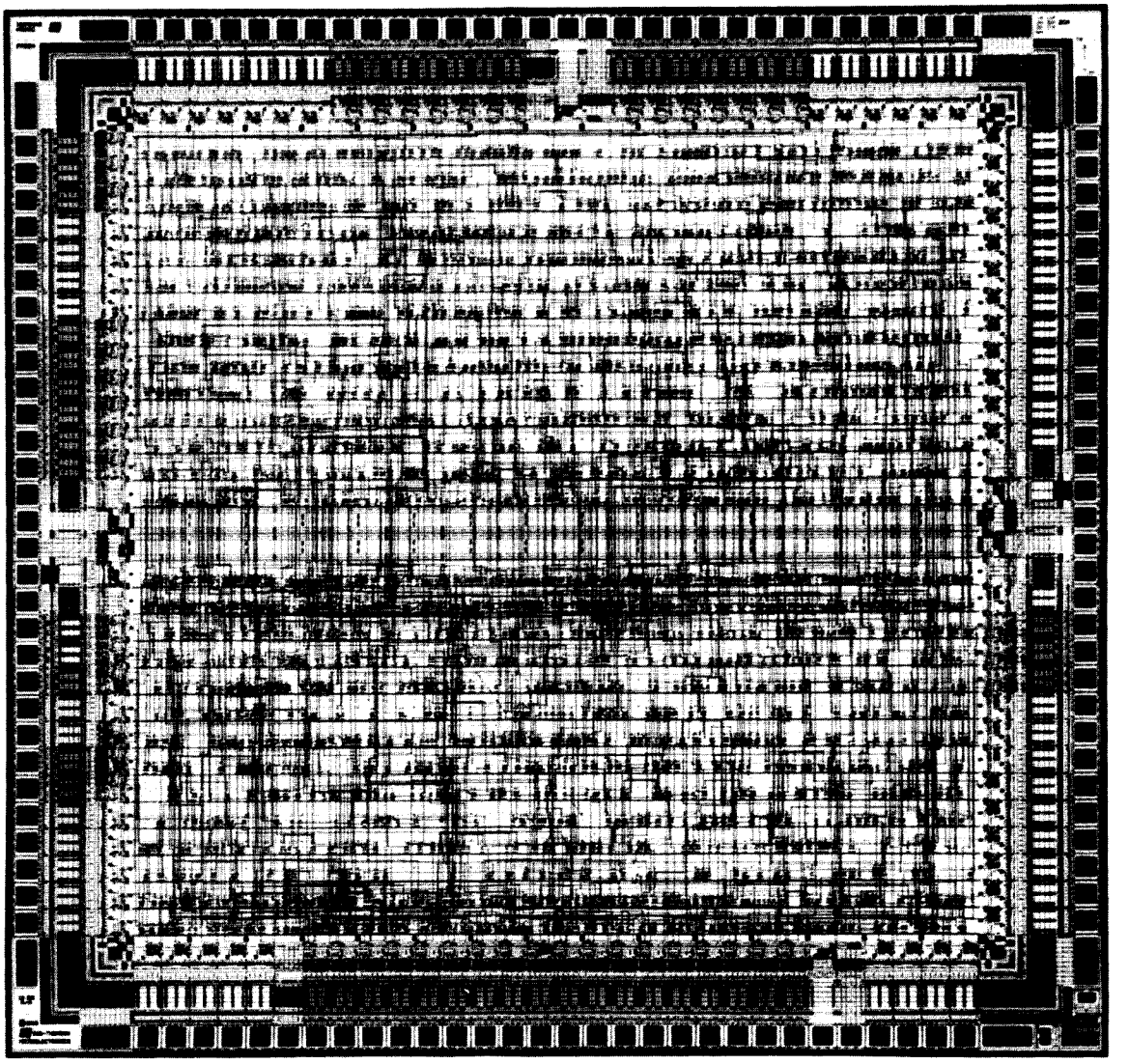
EVALUATION DEVICE

An evaluation device using the ISB18018 base array is available to demonstrate the performance of the ISB18000 series as well as verify the effectiveness of the design system. The device has path delays, latches and a host of macrocells which were used to verify the simulated characteristics that are supplied in the data book.

Characterization of the path delays including interconnect shows typical delays of 400 ps for a 2 input NAND with receivers/drivers operating at frequencies in excess of 100 MHz.

The evaluation device is available in a 120 pin plastic quad flat pack.
An application note that describes how to use it as an evaluation device is also available.

Figure 2. ISB18000 Evaluation Device



PROPAGATION DELAY

The propagation delays shown in the ISB18000 data book and the AC Characteristics section of this data sheet are given for nominal processing, 5 V operation, and 25°C temperature conditions. However there are additional factors that affect the delay characteristics of the macrocells. These include loading due to fanout and interconnect routing, voltage supply, junction temperature of the device, processing tolerance and input signal transition time. Prior to physical layout, the design system can estimate the delays associated with any critical path. The impact of the placement and routing can be back annotated from the layout for final simulations of critical timing.The effects of junction temperature, (K_T) and voltage supply, (K_V) on the delay numbers are summarized in Table 1. A third factor, is associated with process variation. This multiplier has a minimum of 0.6 and a maximum of 1.5.

Table 1. Temperature and Voltage Multipliers

Temperature (°C)	K_T
–55	0.68
–40	0.74
0	0.90
25	1.00
70	1.17
85	1.23
125	1.39

V_{DD} (V)	K_V
4.50	1.12
4.75	1.05
5.00	1.00
5.25	0.95
5.50	0.90

I/O BUFFERS

The I/O buffers are located on the periphery of the array. Figure 3 is a plot of an I/O buffer. The basic cell consists of a bond pad with an input protection, an output driver section, and a receiver/pre-driver section. Every I/O may be configured as either input, output, bidirectional, tri-state output, tri-state bidirectional, or additional V_{DD} or V_{SS}. High impedance pull-up or pull-down resistors are also available in the I/O cell resistors. Input and output macrocells do not invert logic signals. The output transistors are provided with an independent power distribution metalization thereby minimizing switching transients in the periphery from affecting either the on chip receivers and the internal matrix.

Several important features are incorporated in the output drivers. These include slew rate control, and current spike suppression. Slew rate is controlled by turning on individual sections of the large output transistor in a controlled manner. During normal switching a large surge of current occurs when a conventional CMOS buffer has both P and N channel transistors in conduction. This situation is avoided by placing the buffer in tri-state for approximately 200 ps during the time the buffer changes state. Each output buffer may be configured for up to 24 mA current drive capability.

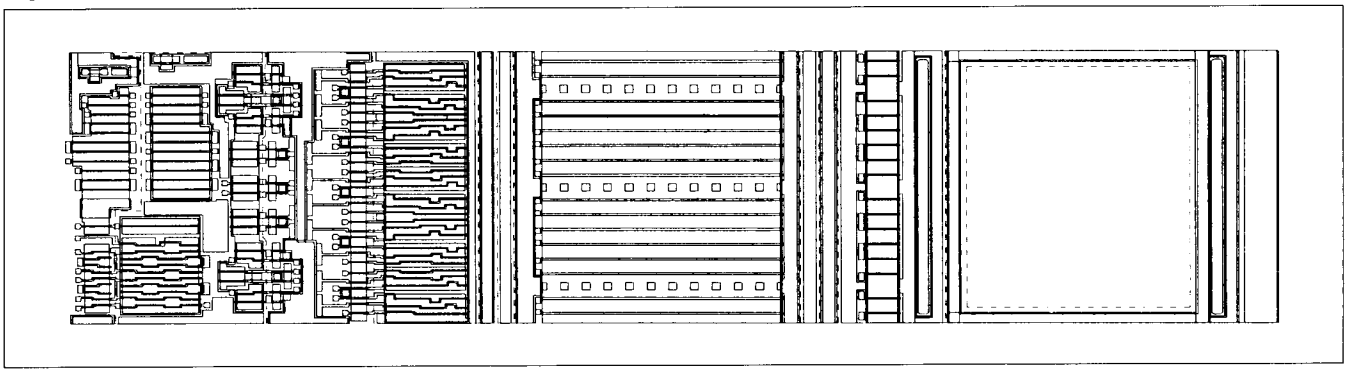
Table 2. I/O Drive capability for slew rate control buffers

Current Drive (mA)	Standard Unit	Maximum Capacitance (pF)
4.0	0.33	100
8.0	0.67	200
12.0	1.00	300
16.0	1.33	500
24.0	2.00	750

Table 3. I/O Drive capability for non-slew rate control buffers

Current Drive (mA)	Standard Unit	Maximum Capacitance (pF)
4.0	1.0	100
8.0	2.0	200
16.0	3.0	500
24.0	4.0	750

Figure 3. Full Function I/O Cell



Selection of the correct output buffer is very important to achieve the desired performance. Two parameters are used to select the appropriate buffer: maximum drive current and load capacitance. See Tables 2 and 3. Exceeding the maximum load capacitance will also result in slower switching performance. Exceeding the maximum current may result in degraded levels and reliability. Standard CMOS and TTL levels are specified for all external buffers. Schmitt Trigger input receivers are available. All buffers are designed for commercial, industrial and military operation.

Table 4. Minimum Power Supply Requirements

Device Name	V_{DDEXT}/ V_{SSEXT}	V_{DDINT}/ V_{SSINT}	Total
ISB18006	1/1	1/1	4
ISB18010	2/2	2/2	8
ISB18013	2/2	4/4	12
ISB18018	2/2	4/4	12
ISB18026	2/2	4/4	12
ISB18032	2/2	4/4	12
ISB18042	2/2	6/6	16
ISB18054	2/2	6/6	16

POWER PAD REQUIREMENTS

Slew rate control and current spike suppression are designed into the individual output buffers and control the di/dt. Simultaneous switching of multiple outputs will result in large amounts of instantaneous current being demanded from the power busses that service the output driver transistors. To minimize this impact on the core matrix and the input receivers, each array in the ISB18000 series has four pairs of V_{DD} and V_{SS} power pads (V_{DDEXT} and V_{SSEXT}) that service the output driver transistors independently of the power distribution to the internal matrix, pre-driver, and receiver circuitry which is supplied through other power pads (V_{DDINT} and V_{SSINT}). For the ISB18006 through the ISB18054, depending on their application, all four pairs of V_{DDEXT}/V_{SSEXT} may not be required. The minimum number of power supply pads bonded per generic array is defined in Table 4.

Depending on the current drive capability of the output buffers selected, it may be necessary to establish additional V_{DDEXT} and V_{SSEXT} power pads. This may be accomplished by configuring a pair of I/O pads as power pads for each additional V_{DDEXT} and V_{SSEXT} pair. The maximum available I/O will decrease by the corresponding amount.

Two rules must be adhered to:

1. A pair of V_{DDEXT} and V_{SSEXT} is required for every 20 Standard Units.

2. No more than 20 Standard Units may be physically positioned between any V_{DDEXT} and V_{SSEXT}.

A Standard Unit of current drive is defined in Tables 2 and 3.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage, V_{DD}	–0.50 V to + 7.00 V
Input or Output Voltage	–0.50 V to (V_{DD} + 0.50) V
DC Forward Bias Current, Input Or Output	± 24 mA
Storage Temperature (Ceramic)	–65 to 150°C
Storage Temperature (Plastic)	–40 to 125°C

Note 1: Referenced to V_{SS}. Stresses above those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the device reliability.

RECOMMENDED DC OPERATING CONDITIONS

Operating Supply Voltage V_{DD}	
Commercial	4.50 V to 5.50 V
Industrial	4.50 V to 5.50 V
Military	4.75 V to 5.25 V
Operating Ambient Temperature	
Commercial	0 to + 70°C
Industrial	–40 to + 85°C
Military	–50 to + 125°C

DC ELECTRICAL CHARACTERISTICS
Across Temperature Range (Note 1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Notes
TTL INTERFACE							
V_{IL}	Low Level Input Voltage				0.8	V	2,3
V_{IH}	High Level Input Voltage		2.0			V	2,3
V_{OL}	Low Level Output Voltage	I_{OL} = Rated buffer current			0.4	V	2,3,4
V_{OH}	High Level Output Voltage	I_{OH} = Rated buffer current	2.4			V	2,3,4
V_{T+}	Schmitt Trig. +ve Threshold			2.0	2.4	V	
V_{T-}	Schmitt Trig. –ve. Threshold		0.6	0.8		V	
CMOS INTERFACE							
V_{IL}	Low Level Input Voltage				1.5	V	3
V_{IH}	High Level Input Voltage		3.5			V	3
V_{OL}	Low Level Output Voltage				0.4	V	3,5,6
V_{OH}	High Level Output Voltage	$I_o \geqslant = 1\mu A$	4.5			V	3,5,7
V_{T+}	Schmitt Trig. +ve Threshold			3.0	4.0	V	
V_{T-}	Schmitt Trig. –ve Threshold		1.0	1.5		V	
GENERAL							
I_{IL}	Low Level Input Current	$V_I = V_{SS}$			± 1	µA	
I_{IH}	High Level Input Current	$V_I = V_{DD}$			± 1	µA	
I_{OZ}	Tri-state Output Leakage	V_O = 0 V or V_{DD}			± 10	µA	
C_{IN}	Input Capacitance	Freq = 1 MHz @ 0 V		2	4	pF	8
C_O	Output Capacitance	Freq = 1 MHz @ 0 V		4	8	pF	8
$C_{I/O}$	Bidi. I/O Capacitance	Freq = 1 MHz @ 0 V		4	8	pF	8
I_{KLU}	I/O Latch-up Current	$V < V_{SS}$, $V > V_{DD}$	500			mA	
V_{ESD}	Electrostatic Protection	C= 100 pF, R = 1.5 KOHM	2000			V	
PD_G	Power Dissipation per gate			6		µ W/Gate/MHz	9
PD_O	Power Dissipation per Output	C = 50 pF		3.0		mW/Output/MHz	9

Notes 1.Commercial 0 to 70°C, V_{DD} = 5 V ± 5%.
Industrial –40 to 85°C, V_{DD} = 5 V ± 5%.
Military –55 to 125 °C, V_{DD} = 5 V ± 10%.
2.Adherence to rules in Power Requirements section required.
3.Refer to the Design Manual for AC Testing Levels and Conditions
4.Buffers offered in 4, 8, 12, 16, 24, 48 mA TTL options. The 48mA buffer is rated for sink current only.
5.Buffers are available in 4mA CMOS options.
6.If all outputs are CMOS then VOL (Max) = 0.05V
7.If all outputs are CMOS then VOH (Min) = VDD-0.05V
8.Excluding Package.
9.Refer to section on Power Requirements.

AC ELECTRICAL CHARACTERISTICS
V_{DD} = 5 V, T_A = 25°C (Note)

Internal Macrocells					Propagation Delays (ns) Standard Loads (1)		
Cell Name	Symbol	Cell Usage			2	4	16
2-input Exclusive OR, double drive	EOP	10	A to Z	t_{PHL}	0.9	1.0	1.2
				t_{PLH}	0.7	0.9	1.5
2-input NAND, double drive	ND2P	5	A to Z	t_{PHL}	0.3	0.4	0.9
				t_{PLH}	0.3	0.4	0.8
3-input NAND, double drive	ND3P	7	A to Z	t_{PHL}	0.4	0.5	1.0
				t_{PLH}	0.4	0.4	0.8
4-input NAND double drive	ND4P	10	A to Z	t_{PHL}	0.6	0.7	1.3
				t_{PLH}	0.4	0.5	0.8
6-input NAND double drive	ND6P	12	A to Z	t_{PHL}	1.1	1.1	1.4
				t_{PLH}	0.8	0.8	1.2
8-input NAND, double drive	ND8P	14	A to Z	t_{PHL}	1.2	1.2	1.5
				t_{PLH}	0.8	0.8	1.2
2-input NOR, double drive	NR2P	5	A to Z	t_{PHL}	0.3	0.3	0.6
				t_{PLH}	0.5	0.6	1.3
3-input NOR, double drive	NR3P	7	A to Z	t_{PHL}	0.2	0.3	0.6
				t_{PLH}	0.6	0.7	1.7
4-input NOR, double drive	NR4P	9	A to Z	t_{PHL}	0.3	0.3	0.6
				t_{PLH}	0.7	0.9	2.1
6-input NOR, double drive	NR6P	10	A to Z	t_{PHL}	0.7	0.7	0.9
				t_{PLH}	1.2	1.3	1.6
8-input NOR, double drive	NR8P	12	A to Z	t_{PHL}	0.7	0.7	0.9
				t_{PLH}	1.3	1.4	1.7
D Flip-Flop, double buffered outputs	FD1P	16	CP to Q	t_{PHL}	0.8	0.8	1.1
				t_{PLH}	1.0	1.0	1.4
			CP to QN	t_{PHL}	1.2	1.2	1.5
				t_{PLH}	1.0	1.1	1.4
			D	t_S	0.75		
				t_H	0.44		
			CP	t_{PWL}	0.85		
				t_{PWH}	1.03		

AC ELECTRICAL CHARACTERISTICS
V_{DD} = 5 V, T_A = 25°C (Note)

External Macrocells Input Interface				Propagation Delays (ns) Standard Loads (1)		
Cell Name	**Symbol**			**2**	**4**	**16**
TTL Input Buffer	TLCHT	A to Z	t_{PHL}	1.1	1.1	1.3
			t_{PLH}	0.5	0.5	0.6
TTL Schmitt Trigger Input Buffer	SCHMITT	A to Z	t_{PHL}	1.3	1.3	1.6
			t_{PLH}	0.8	0.8	1.0
CMOS Input Buffer	IBUF	A to Z	t_{PHL}	0.7	0.7	0.9
			t_{PLH}	0.8	0.8	0.9
CMOS Schmitt Trigger Input Buffer	SCHMITC	A to Z	t_{PHL}	1.1	1.2	1.4
			t_{PLH}	2.4	2.4	2.6
Outputs				**Output Load Capacitance**		
Cell Name	**Symbol**			**25pF**	**50pF**	**100pF**
Tristate Output Buffer (4 mA, Non Slew Rate)	BT4	A to Z	t_{PHL}	2.4	3.5	5.5
			t_{PLH}	1.8	2.1	2.9
				50pF	**100pF**	**200pF**
Tristate Output Buffer (8 mA, Non Slew Rate)	BT8	A to Z	t_{PHL}	2.8	4.2	6.9
			t_{PLH}	2.2	3.0	4.5
				100pF	**200pF**	**500pF**
Tristate Output Buffer (16 mA, Full Slew Rate)	BT16R	A to Z	t_{PHL}	4.9	6.6	11.7
			t_{PLH}	4.2	5.1	7.9
				100pF	**200pF**	**240pF (2)**
Tristate Output Buffer (24 mA, Non Slew Rate)	BT24VN	A to Z	t_{PHL}	2.8	3.9	4.3
			t_{PLH}	2.9	3.6	3.9

Note: 1. Please refer to the ISB18000 Design Manual for standard load equivalents for estimated wirelengths.
2. The EISA bus specification requires that the characterization of the 24mA Output Buffer is at 240 pF maximum.

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