Microchip®

PIC1670

8 Bit Microcontroller

FEATURES

- 1024 x 13-bit Program ROM
- 64 x 8-bit RAM (16 special purpose registers)
- Arithmetic Logic Unit
- Sophisticated interrupt structure
- 6 level pushdown stack
- Versatile self contained oscillator
- 2.0μs instruction execution time
- Wide power supply operating range (4.5-5.5 volts)
- 4 sets of 8 user defined TTL compatible I/O lines
- Available in two temperature ranges: 0°C to 70°C and -40°C to 85°C

PIN CONFIGURATION
40 Lead Dual In Line

Top View

→	OSC1	1	40	V_{DD}	←
←	OSC2	2	39	$\overline{MCLR}$	←
↔	RA0	3	38	RT	←
↔	RA1	4	37	RD7	→
↔	RA2	5	36	RD6	↔
↔	RA3	6	35	RD5	↔
←	CLKOUT	7	34	RD4	↔
↔	RA4	8	33	RD3	↔
↔	RA5	9	32	RD2	↔
↔	RA6	10	31	RD1	↔
↔	RA7	11	30	RD0	↔
↔	RB0	12	29	RC7	↔
↔	RB1	13	28	RC6	↔
↔	RB2	14	27	RC5	↔
↔	RB3	15	26	RC4	↔
↔	RB4	16	25	RC3	↔
↔	RB5	17	24	RC2	↔
↔	RB6	18	23	RC1	↔
↔	RB7	19	22	RC0	↔
→	V_{SS}	20	21	TEST	←

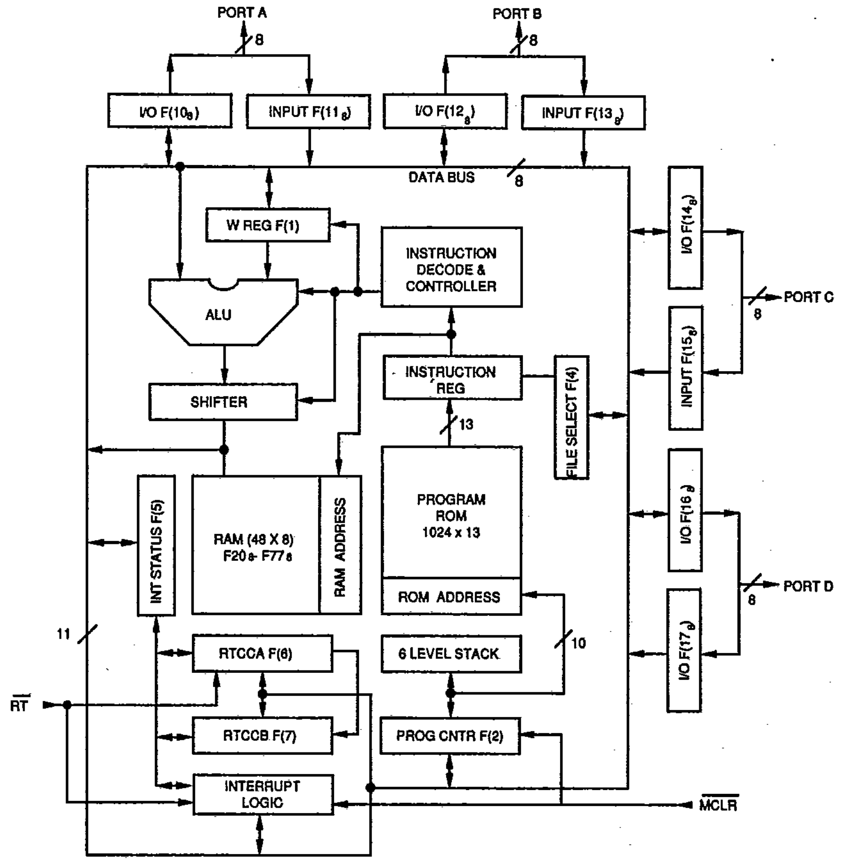
DESCRIPTION

The PIC1670 microcontroller is an MOS/LSI device containing RAM, I/O, and a central processing unit as well as customer-defined ROM on a single chip. This combination produces a low cost solution for applications which require sensing individual inputs and controlling individual outputs. Keyboard scanning, display driving, and system control functions can be done at the same time due to the power of the 8-bit CPU.

The internal ROM contains a customer-defined program using the PIC's powerful instruction set to specify the overall functional characteristics of the device. The 8-bit input/output registers provide latched lines for interfacing to a limitless variety of applications. The PIC can be used to scan keyboards, drive displays, control electronic games and provide enhanced capabilities to vending machines, traffic lights, radios, television, consumer appliances, industrial timing and control applications. The 13-bit instruction word format provides a powerful yet easy to use instruction repertoire emphasizing single bit manipulation as well as logical and arithmetic operations using bytes.

The PIC1670 is fabricated with N-Channel Silicon Gate technology resulting in a high performance product. Only a single wide range power supply is required for operation. An on-chip oscillator provides the operating clock with an external crystal or ceramic resonator to establish the frequency. Inputs and outputs are TTL-compatible, with open-drain option available.

Extensive hardware and software support is available to aid the user in developing an application program and to verify performance before committing to mask tooling. Programs can be assembled into machine language using PICALC, eliminating the burden of coding with ones and zeros. Once the application program is developed, several options are available to insure proper performance. The PIC's operation can be verified in any hardware application by using the PIC1665. The PIC1665 is a ROM-less PIC1670 microcontroller with additional pins to connect external EPROM or RAM and to accept HALT commands. The PFD 1020 Field Demo System is available containing a PIC1665 with sockets for erasable PROMS. Finally, the PICES II (PIC In-Circuit Emulation System) provides the user with emulation and debugging capability in either a stand-alone mode or operation as a peripheral to a larger computer system. Easy program debugging and changing is facilitated because the user's program is stored in RAM. With these development tools, the user can quickly and confidently order the masking of the PIC's ROM and bring his application into the market.



ARCHITECTURAL DESCRIPTION

The firmware architecture of the PIC1670 microcontroller is based on a register file concept with simple yet powerful instruction commands designed to optimize the code for bit, byte, and register transfer operations. The instruction set also supports computing functions as well as these control and interface functions.

Internally, the functional blocks of the PIC1670 are connected by an 8-bit bidirectional bus: the 64 8-bit registers of which the first 16 are special purpose, an Arithmetic Logic Unit, and a user defined program ROM composed of 1024 x 13 words. The register file is divided into two functional groups: operational registers and general purpose registers. The first sixteen are the operational registers and they include the Real Time Clock Counter A and B, four I/O registers, two Status registers, a Program Counter and a File Select Register. The general purpose registers are used for data and control information under command of the instructions.

The Arithmetic Logic Unit contains one temporary working register (W Register), an adder, and hardware for decimal adjust. Manipulation between data in the working register and any other register can be performed.

The Program ROM contains the user defined application program and is supported by an instruction decoder and instruction register. Sequencing of microinstructions is controlled via the Program Counter (PC) which automatically increments to execute in-line programs. The Program Counter is modified by bit test, jump, call or branch instructions and the lower 8-bits can be modified for computed addresses by file register instructions. In addition, an on-chip six level stack is employed to push and pull the contents of the program counter. This provides easy to use subroutine nesting. Activating the $\overline{MCLR}$ input on power-up initializes the ROM program to address 1777_8.

T-49-19-08

REGISTERS

REGISTER FILE ARRANGEMENT

File	Function
F0₈	Not a physical register. F0 calls for contents of the FSR (F4) to be used to select a file register. F4 is used as an indirect address pointer.
F1₈	W Register: The working register.
F2₈	Program Counter: Points to the next program ROM address to be executed (8 lower bits only).
F3₈	Arithmetic Status Register
F4₈	File Select Register: The FSR is used in generating effective file register addresses under program control.
F5₈	Interrupt Status Register: Used to control interrupts and registers F6 and F7. (See "Interrupt System")
F6₈, F7₈	RTCCA and RTCCB: Real Time Clock Counters A & B respectively can be configured as a single 16 bit counter, an 8 bit counter and an 8 bit general purpose register or two general purpose registers when no external counting is required. The RTCC registers can be loaded and read by the program, as well as count negative transitions on the $\overline{RT}$ pin or count at 1/8 the frequency of the oscillator. If data are being stored into RTCCA simultaneous with a negative transition on the $\overline{RT}$ pin (and CNTE = 1 and CNTS = 1), RTCCA will contain the new stored value and the external transition will be ignored by the microcomputer. (See "Real Time Clock Interrupt" for further details about the RTCC).
F10₈, 11₈	I/O Port A
F12₈, 13₈	I/O Port B
F14₈, 15₈	I/O Port C
F16₈, 17₈	I/O Port D
F20₈, 77₈	General Purpose Registers: Used for temporary and general purpose storage during program execution time.

Note: F10₈, 12₈, 14₈ & 16₈ are the I/O registers and F11₈, 13₈, 15₈ & 17₈ are used for reading the actual pin levels.

ARITHMETIC STATUS REGISTER F3

7	6	5	4	3	2	1	0
1	1	A9	A8	OV	Z	DC	C

Bit	Name	Function
0	C	Bit 0 is the carry flag and is usually the carry from the A.L.U., also used as a borrow subtract instructions.
1	DC	Bit 1 is the half carry (decimal carry) and is used to indicate a carry from bit 3 in the A.L.U. as the result of an addition (byte). This bit is used in the decimal adjust instruction to allow B.C.D. decimal addition.
2	Z	Bit 2 is the zero flag and is set to a one if the results of the previous operation was identically zero.
3	OV	Bit 3 is the overflow flag and is set to a one by operations which cause a signed two's complement arithmetic overflow. The bit is set when the carry from the MSB in the A.L.U. is opposite to the carry from the MSB-1 bit.
4	A8	Bit 4 is the 9th bit of the program counter. This bit is a read only bit.
5	A9	Bit 5 is the 10th bit of the program counter. This bit is a read only bit.

INTERRUPT STATUS REGISTER F5

7	6	5	4	3	2	1	0
0	CNTE	AIE	CNTS	FTCIR	XIR	FTCIE	XIE

4

BASIC INSTRUCTION SET AND PIN FUNCTIONS

Each PIC instruction is a 13-bit word divided into an OP code which specifies the instruction type and one or more operands which further specify the operation of the instruction. The following PIC instruction summary lists byte-oriented, bit-oriented, and literal and control operations.

For byte-oriented instructions, "f" represents a file register designator and "d" represents a destination designator. The file register designator specifies which one of the PIC file registers is to be utilized by the instruction. The destination designator specifies where the result of the operation performed by the instruction is to be placed if "d" is zero. The result is placed in the W register if "d" is one. The result is returned to the file register specified in the instruction.

For bit-oriented instructions, "b" represents a bit field designator which selects the number of the bit affected by the operation while "f" represents the number of the file in which the bit is located.

For literal and control operations, "k" represents an eight or nine bit constant or literal value.

For an oscillator frequency of 4 MHz the instruction execution time is 2.0µsec unless a conditional test is true or the program counter is changed as a result of an instruction. In these two cases, the instruction execution time is 4.0µsec.

BYTE ORIENTED FILE REGISTER OPERATIONS

(12 - 7)	(6)	(5 - 0)
OPCODE	d	f(FILE #)

Instruction-Binary					(Octal)	Name	Mnemonic, Operands		Operation	Status Affected
0	000	000	000	100	(00004)	Decimal adjust W	DAW	-	(Note 1)	C
0	000	001	fff	fff	(00100)	Move W to file	MOVWF	f	W→f	-
0	000	1d	fff	fff	(00200)	Subtract W from file w/borrow	SUBBWF	f,d	f + $\overline{W}$ + c→ d	OV,C,DC,Z
0	000	10d	fff	fff	(00400)	Subtract W from file	SUBWF	f,d	f + $\overline{W}$ + 1→ d	OV,C,DC,Z
0	000	11d	fff	fff	(00600)	Decrement file	DECF	f,d	f - 1→ d	OV,C,DC,Z
0	001	00d	fff	fff	(01000)	Inclusive or W with file	IORWF	f,d	WVf → d	Z
0	001	01d	fff	fff	(01200)	And W with file	ANDWF	f,d	W • 1→ d	Z
0	001	10d	fff	fff	(01400)	Exclusive OR W with file	XORWF	f,d	W ⊕ f → d	Z
0	001	11d	fff	fff	(01500)	Add W with file	ADDWF	f,d	W + f → d	OV,C,DC,Z
0	010	00d	fff	fff	(02000)	Add W to file with carry	ADCWF	f,d	W + f + c → d	OV,C,DC,Z
0	010	01d	fff	fff	(02200)	Complement file	COMPF	f,d	$\overline{f}$ → d	Z
0	010	10d	fff	fff	(02400)	Increment file	INCF	f,d	f + 1 → d	OV,C,DC,Z
0	010	11d	fff	fff	(02600)	Decrement file, skip if zero	DECFSZ	f,d	f • 1 → d, skip if zero	-
0	011	00d	fff	fff	(03000)	Rotate file right through carry	RRCF	f,d	f(n)→d(n - 1), c→d(7), f(0)→c	C
0	011	01d	fff	fff	(03200)	Rotate file left through carry	RLCF	f,d	f(n)→d(n + 1), c→d(0), f(7)→c	C
0	011	01d	fff	fff	(03400)	Swap upper and lower nibble of file	SWAPF	f,d	f(0-3) ↔ (4-7)→d	-
0	011	11d	fff	fff	(03600)	Increment file, skip if zero	INCFSZ	f,d	f + 1 → d, skip if zero	-
1	000	000	fff	fff	(0004)	Move file to W	MOVFW	f	f → W	Z
1	000	001	fff	fff	(00100)	Clear file	CLRF	f	0 → f	Z
1	000	010	fff	fff	(00200)	Rotate file right/no carry	RRNCF	f	f(n) → d(n-1), f(0) → f(7)	-
1	000	011	fff	fff	(00300)	Rotate file left/nocarry	RLNCF	f	f(n)→d(n + 1), f(7)→f(0)	-
1	000	100	fff	fff	(00400)	Compare file to W, skip if F < W	CPFSLT	f	f - W, skip if C = 0	-
1	000	101	fff	fff	(00500)	Compare file to W skip if F = W	CPFSEO	f	f - W, skip if Z = 1	-
1	000	110	fff	fff	(00800)	Compare file to W, skip if F> W	CPFSGT	f	f - W, skip if Z • C = 1	-
1	000	111	fff	fff	(01000)	Move file to itself	TESTF	f	f - 1	Z

Note 1: The DAW instruction adjusts the eight bit number in the W register to form two valid BCD (binary coded decimal) digits, one in the lower and in the upper nibble. (The results will only be meaningful if the number in W to be adjusted is the result of adding together two valid two digit BCD numbers). The adjustment obeys the following two step algorithm.
1. If the lower nibble is greater than 9 or the digit carry flag (DC) is set, 06 is added to the W register.
2. Then, if the upper nibble is greater than 9 or the carry from the original or step 1 addition is set, 60 is added to the W register. The carry bit is set if there is a carry from the original step 1 or step 2 addition.

BIT ORIENTED FILE REGISTER OPERATIONS

(12 - 9)	(8 - 6)	(5 - 0)
OPCODE	b(BIT #)	f(FILE #)

Instruction-Binary	(Octal)	Name	Mnemonic, Operands		Operation	Status Affected
0 100 bbb fff fff	(04000)	Bit clear file	BCF	f,b	0 → f(b)	-
0 101 bbb fff fff	(05000)	Bit set file	BSF	f,b	1 → f(b)	-
0 110 bbb fff fff	(06000)	Bit test, skip if clear	BTFSC	f,b	Bit Test f(b),skip if clear	-
0 111 bbb fff fff	(07000)	Bit test,skip if set	BTFSS	f,b	Bit Test f(b), skip if set	-

LITERAL AND CONTROL OPERATIONS

(12 -8)	(7 - 0)
OPCODE	k (LITERAL)

Instruction-Binary	(Octal)	Name	Mnemonic, Operands		Operation	Status Affected
0 000 000 000 000	(00000)	No Operation	NOP	-	-	-
0 000 000 000 010	(00002)	Return from interrupt	RETFI	-	Stack → PC	-
0 000 000 000 011	(00003)	Return from Subroutine	RETFS	-	Stack → PC	-
1 001 0kk kkk kkk	(11000)	Move Literal tro W	MOVLW	k	k → W	-
1 001 1kk kkk kkk	(11400)	Add Literal to W	ADDLW	k	k + W → W	OV,C,DC,Z
1 010 0kk kkk kkk	(12000)	Inclusive OR Literal to W	IORLW	k	kVW →- W	Z -
1 010 1kk kkk kkk	(02400)	And Literal and W	ANDLW	k	k • W → W	Z
1 011 0kk kkk kkk	(13000)	Exclusive OR Literal to W	XCRLW	k	k W → W	Z
1 011 1kk kkk kkk	(13400)	Return and load literal in W	RETLW	k	k ⊕ W, Stack - PC	-
1 10k kkk kkk kkk	(14000)	Go to address	GOTO	k	k → PC	-
1 11k kkk kkk kkk	(16000)	Call Subroutine	CALL	k	PC + 1 → Stack, k → PC	-

PIN FUNCTIONS

Signal Name	Signal Type	Function
OSC1, OSC2	Input Output	Oscillator pins. The on-board oscillator can be driven by an external crystal ceramic resonator or an external clock via these pins.
$\overline{RT}$	Input	Real Time Input. Negative transitions on this pin increment the RTCC (F6) register. This pin can also be used for an interrupt input. This pin uses a Schmitt trigger input. There is no internal active pull-up device.
RA0-7, RB-7, RC0-7, RD0-7	Input Output	User programmable input/output lines. These lines can be used as inputs and/ or outputs and are under direct control of the program.
$\overline{MCLR}$	Input	Master Clear: Used to initialize the internal ROM program to address 1777_8 latch all I/O registers high, and disables the interrupts. This pin uses a Schmitt trigger input. There is no internal active pull-up device.
TEST	Input	Test pin. This pin is used for testing purposes only. It must be grounded for normal operation.
V_{DD}	-	Power supply pin.
V_{SS}	-	Ground pin.
CLKOUT	Output	Clock Output: A signal derived from the internal oscillator. May be used by external circuitry to synchronize with PIC1670 timing.

T-49-19-08

INTERRUPT SYSTEM

The interrupt system of the PIC1670 is comprised of an external interrupt and a real-time clock counter interrupt. These have different interrupt vectors, enable bits and status bits. Both interrupts are controlled by the status register (F5) shown below.

7	6	5	4	3	2	1	0
0	CNTE	A/B	CNTS	RTCIR	XIR	RTCIE	XIE

Notes: 1. Bit 7 is unused and is read as zero.
2. The Status Register F5 will power up to all zeroes.

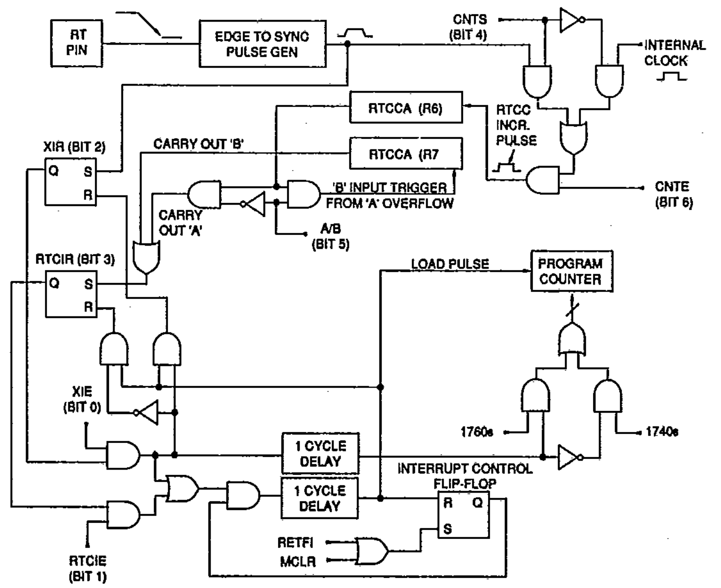
External Interrupt

On any high to low transition of the $\overline{RT}$ pin the external interrupt request (XIR) bit will be set. This request will be serviced if the external interrupt enable (XIE) bit is set or if it is set at a later point in the program. The latter allows the processor to store a request (without interrupting) while a critical timing routine is being executed. Once external interrupt service is initiated, the processor willclear the XIR bit, delay one cycle (to execute the current instruction), then push the current program counter onto the stack and execute the instruction at location 1760_8. It takes three to four instruction cycles from the transition on the $\overline{RT}$ pin until the instruction at 1760_8 is executed. No new interrupts can be serviced until a return from interrupt (RETFI) instruction has been executed.

Real-Time Clock Interrupt

The real-time clock counter (RTCCA & RTCCB, file registers F6 and F7) have a similar mechanism of interrupt service. The RTCCA register will increment if the count enable (CNTE) bit is set: If this bit is not set the RTCCA & RTCCB will maintain their present contents and can therefore be used as general purpose RAM registers. The count source (CNTS) bit selects the clocking source for RTCCA. If CNTS is cleared to a '0', then RTCCA will use the internal instruction clock and increment at 1/8 the frequency present on the OSC pins. If CNTS is set to a '1', then RTCCA will increment on each high to low transition of the RT pin. RTCCB can only be incremented when RTCCA makes a transition from 377_8 to 0 and the A/B status bit is set. This condition links the two eight bit registers together to form one sixteen bit counter. An interrupt request under these conditions will occur when the combined registers make a transition from 177777_8 to 0. If, however, the A/B bit is not set, then RTCCA will be the only incrementing register and an interrupt request will occur when RTCCA makes a transition from 377_8 to 0. (In this setup the RTCCB register will not increment and can be used as a general purpose RAM register). Once a request has come from the real-time clock counter, the real-time clock interrupt request (RTCIR) bit will be set. At this point, the request can either be serviced immediately if the real-time clock interrupt enable (RTCIE) bit is set or be stored if RTCIE is not set. The latter allows the

INTERRUPT SYSTEM BLOCK DIAGRAM



Interrupt System (Cont.)

processor to store a real-time clock interrupt while a critical timing routine is being executed. Once interrupt service is initiated, the processor will clear the RTCIR bit, delay one cycle (to execute the current instruction), then push the present program counter onto the stack and execute the instruction at location 1740₈. It takes three instruction cycles from when the RTCC(A or B) overflows until the instruction 1740₈ is executed. No new interrupts can be serviced until a RETFI instruction has been executed.

The RETFI instruction (00002₈) must be used to return from any interrupt service routine if any pending interrupts are to be serviced. External interrupts have priority over RTCC driven interrupt in the event both types occur simultaneously. Interrupts cannot be nested but will be serviced sequentially. The existance of any pending interrupts can be tested via the state of the XIR (bit 2) and RTCIR (bit 1) in the status word F5.

INPUT/OUTPUT CAPABILITY

The PIC1670 provides four complete quasi-bidirectional input/output ports. A simplified schematic of an I/O pin is shown below. The ports occupy address locations in the register file space of the PIC1670. Thus, any instruction that can operate on a general purpose register can operate on an I/O port. Two locations in the register file space are allocated for each I/O port. Port RA0-7 is addressable as either F10₈ or F11₈. Port RB0-7 is addressable as either F12₈ or F13₈. Port RC0-7 is addressable as either F14₈ or F15₈. An I/O port READ on its odd-numbered location will interrogate the chip pins while an I/O port READ on its even-numbered location will interrogate the internal latch in that I/O port. This simplifies programming in cases where a portion of a single port is used for inputting only while the remainder is used for outputting as illustrated in the following example.

Here, the low 3 bits of port RA are used as output-only, while the high 5 bits are used as input-only. During power on reset (MCLR low), the latches in the I/O ports will be set high, turning off all pull down transistors as represented by Q 2 in the figure below. During program execution if we wish to interrogate an input pin, then, for example,

BTFSS 11,6

will test pin RA6 and skip the next instruction if that pin is set. If we wish to modify a single output, then, for example,

BCF 10, 2

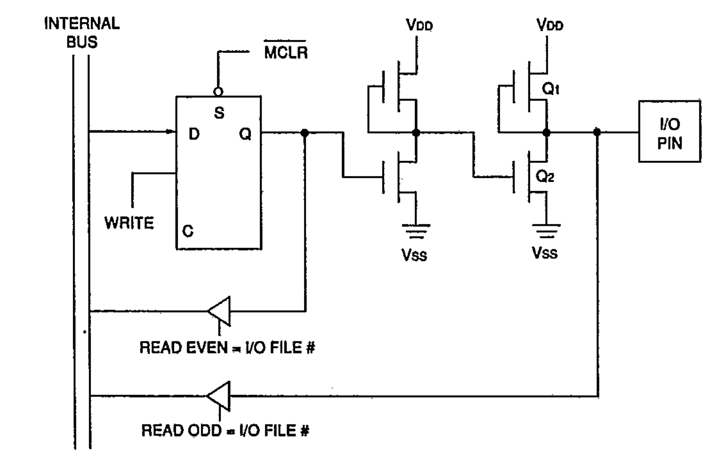
will force RA2 to zero because its internal latch will be cleared to zero. This will turn on Q2 and pull the pin to zero.

The way this instruction operates internally is the CPU reads file 10 into the A.L.U., modifies the bit and re-outputs the data to file 10. If the pins were read instead, any input which was grounded externally would cause a zero to be read on that bit. When the CPU re-outputted the data to the file, that bit would be cleared to zero, no longer useful as an input until set high again.

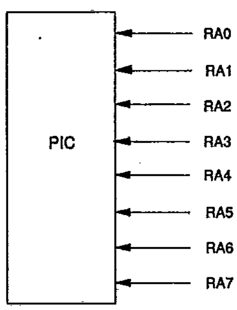
During program execution, the latches in bits 3-7 should remain in the high state. This will keep Q2 off, allowing external circuitry full control of pins RA3-RA7, which are being used here as input.

4

BIDIRECTIONAL INPUT-OUTPUT PORT



I/O PORT



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Temperature Under Bias .... 125°C
Storage Temperature .... - 55°C to +150°C
Voltage on any pin with
respect to Vss .... -0.3V to +10.0V
Power Dissipation 1000mW

* Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied. Operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

DC CHARACTERISTICS

Operating temperature:
- Commercial: $T_A = 0\ ^\circ C$ to $+ 70\ ^\circ C$
- Industrial: $T_A = -40\ ^\circ C$ to $+ 85\ ^\circ C$

Characteristic	Sym	Min	Typ*	Max	Units	Conditions
Power Supply Voltage	V_{DD}	4.5	-	5.5	V	
Primary Supply Current	I_{DD}	-	-	100	mA	All I/O pins high
Input Low Voltage (except $\overline{MCLR}$ & $\overline{RT}$)	V_{IL}	Vss	-	0.8	V	
Input High Voltage (except $\overline{MCLR}$, $\overline{RT}$, OSC1)	V_{IH1}	2.4	-	VDD	V	
Input High Voltage ($\overline{MCLR}$, $\overline{RT}$, OSC1)	V_{IH2}	VDD-1	-	VDD	V	
Output High Voltage	V_{OH}	2.4	-	VDD	V	I_{OH} - 100 µA provided by internal pullups (Note 2)
Output Low Voltage (I/O and CLK OUT)	V_{OL}	-	-	0.45	V	I_{OL} = 1.6mA
Input Leakage Current ($\overline{MCLR}$, $\overline{RT}$, OSC1)	I_{LC}	-5	-	+5	µA	$V_{SS} = V_{IN} - V_{DD}$
Input Low Current (All I/O ports)	I_{IL}	-0.2	-0.6	-2.0	mA	V_{IL} = 0.4V internal pullup
Input High Current (All I/O ports)	I_{IH}	-0.1	-0.4	-	mA	V_{IH} = 2.4V

* Typical data is at T_A = 25°C, V_{DD} = 0V.

Notes: 1. Total power dissipation for the package is calculated as follows:
$P_O = (V_{DD})(I_{DD}) + \Sigma\{(V_{DD} - V_{IL})\cdot|V_{IL}|\} + \Sigma\{(V_{DD} - V_{OH})\cdot|I_{OH}|\} + \Sigma\{(V_{OL})\cdot I_{OL}\}$.
2 Positive current indicates current into pin. Negative current indicates current out of pin.
3. Total I_{OL} for all output pin (I/O ports plus CLK OUT) must not exceed 175mA.

T-49-19-08

AC CHARACTERISTICS

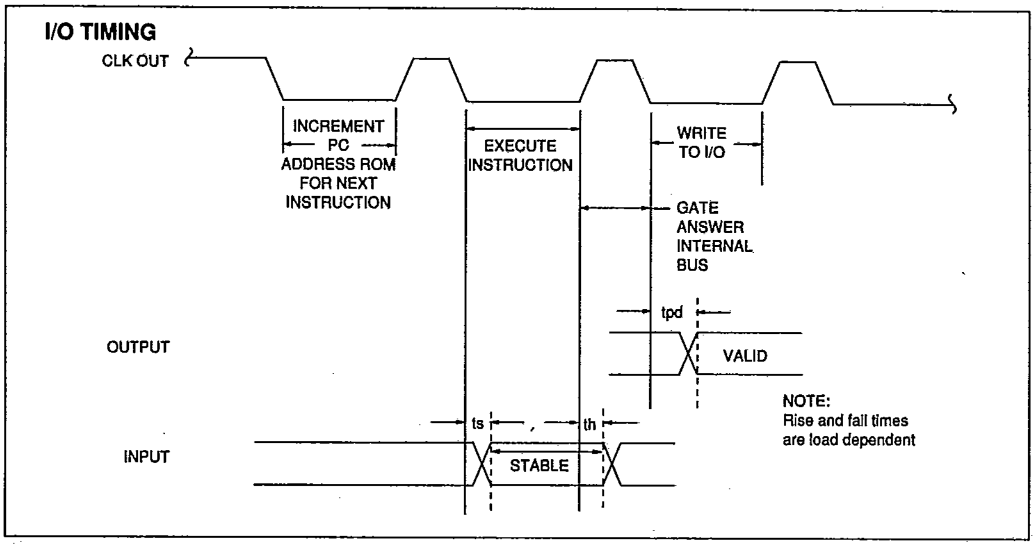
Operating temperature:
- Commercial: $T_A = 0\ ^\circ C$ to $+70\ ^\circ C$
- Industrial: $T_A = -40\ ^\circ C$ to $+85\ ^\circ C$

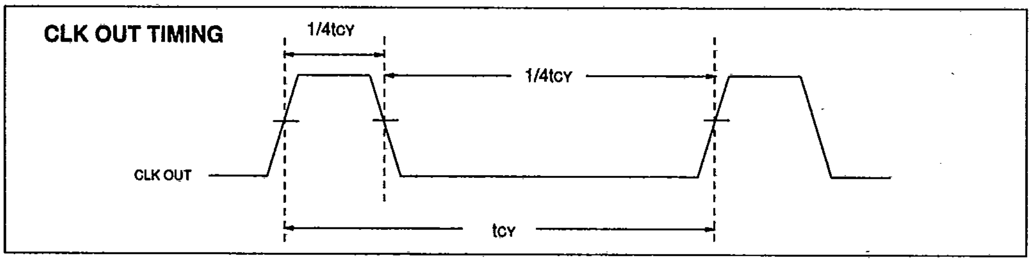
Characteristic	Sym	Min	Typ	Max	Units	Conditions
Instruction Cycle Time	t_{CY}	2.0	-	8	µs	4 MHz external time base (Notes 1, 2, 4))
$\overline{RT}$ Input						(Note 3)
Period - Commercial	t_{RT}	t_{CY}+175ns	-	-	-	Commercial: $T_A = 70^\circ C$
Period -Industrial	t_{RT}	t_{CY}+200ns	-	-	-	Industrial: $T_A = 85^\circ C$
High Pulse Width	t_{RTH}	1/2t_{RT}	-	-	-	Commercial: $T_A = 70^\circ C$
Low Pulse Width	t_{RTL}	1/2t_{RT}	-	-	-	Commercial: $T_A = 70^\circ C$
I/O Ports						
Data Input Setup Time	t_R	-	-	1/4t_{CY} - 125	ns	
Data Input Hold Time	t_H	0	-	-	ns	
Data Output Propagation Delay	t_{RT}	-	500	800	ns	Capacitance load = 50pF

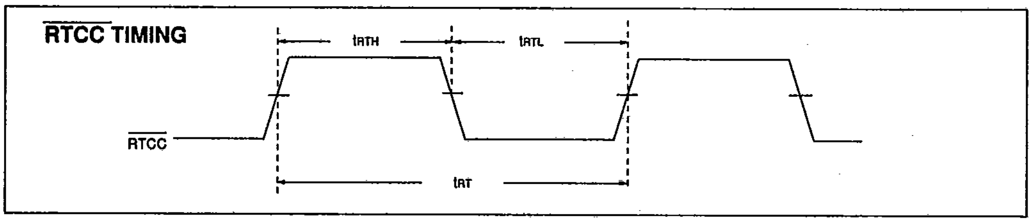
Notes:
1. Instruction cycle period (t_{CY}) equals eight times the oscillator time base period.
2. The oscillator frequency may deviate to 4.08 MHz to allow for tolerance of the time base element (LC, crystal, or ceramic resonator).
3. Due to the synchronous timing nature between CLK OUT and the sampling circuit used on the $\overline{RT}$ input, CLK OUT may be directly tied to the $\overline{RT}$ input. The minimum times specified represent theoretical limits.
4. The maximum frequency which may be input to the $\overline{RT}$ pin is calculated as follows: $f_{max} = \frac{1}{t_{RTmin}} = \frac{1}{t_{CYmin}+\delta}$
   where: ∂=175 ns for Commercial
   ∂=200 ns for Industrial
   Examples: Commercial: if t_{CY} = 2µs, f(max) = 1/2.175 µs = 460 KHz
   Industrial: if t_{CY} = 2µs, f(max) = 1/2.2µs = 455 KHz.

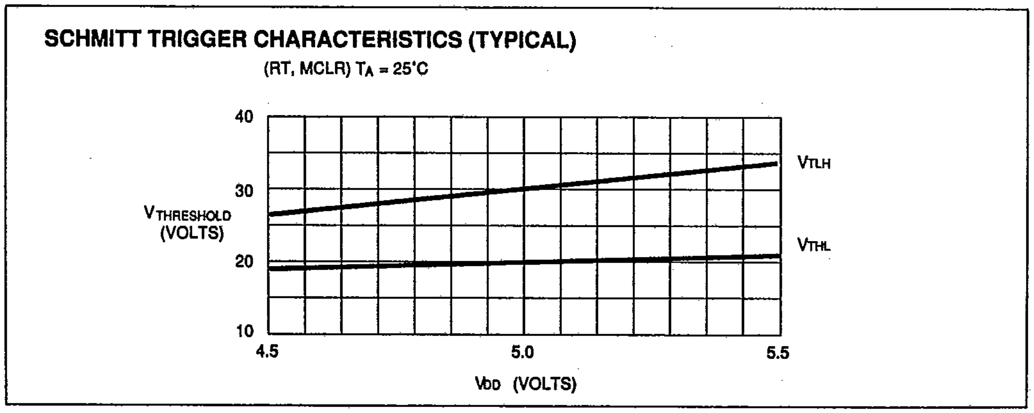
4

T-49-19-08


I/O TIMING
CLK OUT
INCREMENT PC
ADDRESS ROM FOR NEXT INSTRUCTION
EXECUTE INSTRUCTION
WRITE TO I/O
GATE ANSWER INTERNAL BUS
tpd
OUTPUT
VALID
NOTE: Rise and fall times are load dependent
ts
th
INPUT
STABLE

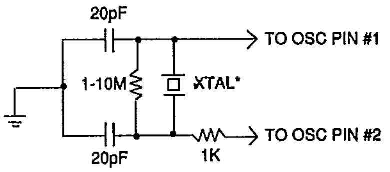

CLK OUT TIMING
1/4tCY
1/4tCY
CLK OUT
tCY


RTCC TIMING
tRTH
tRTL
RTCC
tRT


SCHMITT TRIGGER CHARACTERISTICS (TYPICAL)
(RT, MCLR) TA = 25°C
40
30
20
10
VTHRESHOLD (VOLTS)
VTLH
VTHL
4.5
5.0
5.5
VDD (VOLTS)

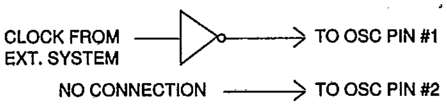
TYPICAL OSCILLATOR CIRCUITS

CRYSTAL INPUT OPERATION

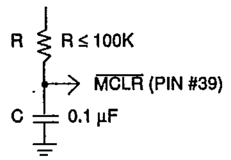


* OR CERAMIC RESONATOR, PARALLEL RESONANT (1.0 - 4.0 MHz)

EXT. INPUT OPERATION

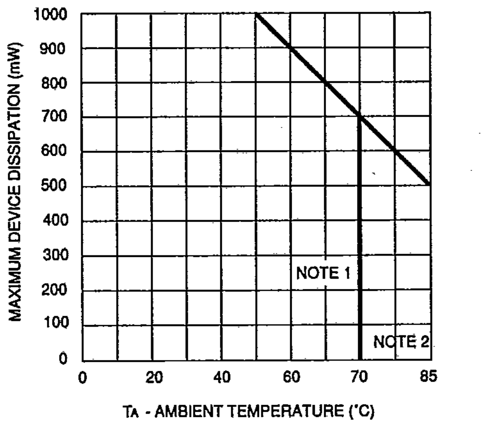


MASTER CIRCUIT (TYPICAL)



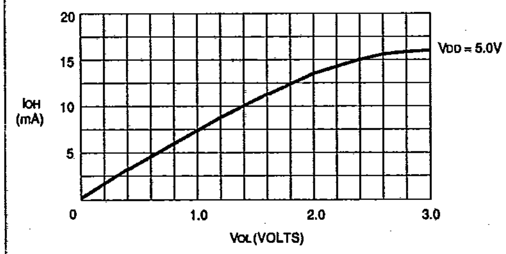
Note: The $\overline{MCLR}$ pin must be pulsed low for a minimum of one complete instruction cycle (tCY) for the master clear function to be guaranteed, assuming that power is applied and the oscillator is running. For inititial power application, a delay is required for the external oscillator time base element to start up before $\overline{MCLR}$ is brought high. To achieve this, an external RC configuration as shown can be used. This provides approximately a 10 ms delay (assuming VDD is applied as a step function), which may be insufficient for some time base elements. Consult the manufacturer of the time base element for specific start-up times.

POWER DISSIPATION DERATING GRAPH

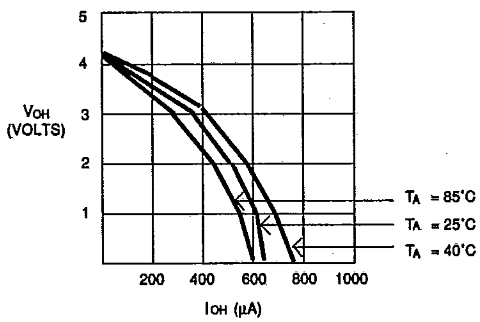


Notes:
1. 70°C is the maximum operating temperature for standard parts.
2. 85°C is the maximum operating temperature for "I" suffix parts.

OUTPUT SINK CURRENT GRAPH



VOH VS IOH (I/O PORTS) (TYPICAL)



T-49-19-08

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

PIC1670 - H /P XXX

Pattern:		3-Digit Pattern Code
Package:	P	Plastic DIP
Temperature Range:	-	0°C to +70°C
	I	-40°C to +85°C
	H	-40°C to +110°C
Device:		PIC1670

LIFE SUPPORT SYSTEM - Microchip's products are not authorized for use as critical components in life support devices or systems without the express written approval of Microchip Technology, Inc.