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32K x 32 EEPROM Module

PUMA67E1001/A-90/12

Issue 4.0 : February 1996

Description

The PUMA 67E1001/A is a 1Mbit CMOS EEPROM module in a JEDEC 68 pin J leaded Ceramic Surface Mount Substrate. Access times of 90 and 120 ns are available. The output width is user configurable as 8, 16, or 32 bits wide using $\overline{CS1\text{-}4}$ and is available in two pinout options, single $\overline{WE}$ or $\overline{WE1\text{-}4}$ (version /A). Page write (64 bytes) is performed in 10 ms (typical). The device also features both hardware and software data protection with $\overline{DATA}$ polling and Toggle bit indication of end of write. Write cycle endurance is 10,000 Erase/Write cycles with a data retention time of 10 years.
The device may be screened in accordance with MIL-STD-883 or with BS9400 requirements.

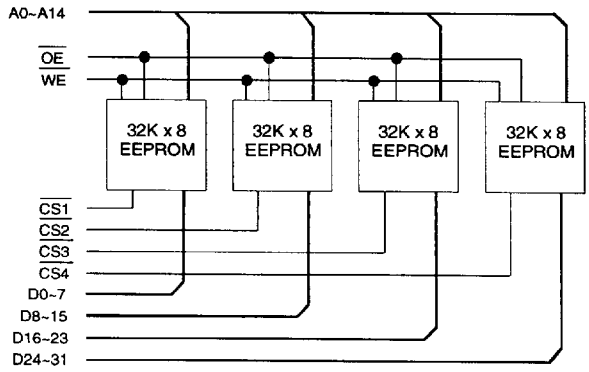
1,048,576 bit CMOS EEPROM Module

Features

- Access Times of 90/120 ns.
- User Configurable as 8 / 16 / 32 bit wide output.
- Operating Power 490 / 915 / 1760 mW (max).
- JEDEC 68 'J' Ceramic Surface Mount Substrate, available in two pinouts : Single $\overline{WE}$, $\overline{WE1\sim4}$ is version A.
- Byte and Page Write (64 Bytes) in 5ms typical with $\overline{DATA}$ Polling and Toggle bit indication of end of Write.
- Hardware and Software Data Protection.
- Endurance of 10^4 Erase/Write Cycles and Data Retention Time of 10 years.
- Can be processed in accordance with MIL-STD-883.

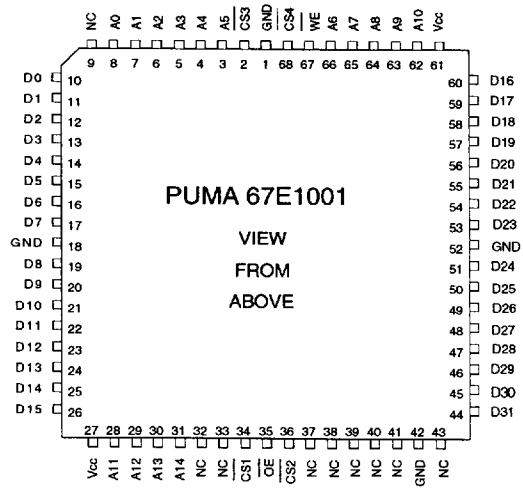
Block Diagram

(see page 12 for Block Diagram of option /A)



Pin Definition

(see page 12 for Pin Definition of option /A)



Pin Functions

A0~14	Address Inputs	**D0~31**	Data Inputs/Outputs
$\overline{CS1\sim4}$	Chip Select	**$\overline{OE}$**	Output Enable
$\overline{WE}$	Write Enable (**$\overline{WE1\sim4}$** on version A)	**NC**	No Connect
V_{cc}	Power (+5V)	**GND**	Ground

DC OPERATING CONDITIONS

Absolute Maximum Ratings (1)

Operating Temperature	T_{OPR}	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C
Input voltages (including N.C. pins) with Respect to GND	V_{IN}	-0.6 to +6.25	V
Output voltages with respect to GND	V_{OUT}	-0.6 to V_{CC}**+0.6**	V

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

		min	*typ*	*max*	
DC Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-0.6	-	0.8	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.75	V
Operating Temp Range	T_A	0	-	70	°C
	T_{AI}	-40	-	85	°C (**I** Suffix)
	T_{AM}	-55	-	125	°C (**M**, **MB** Suffix)

DC Electrical Characteristics (T_A=-55°C to +125°C, V_{CC}=5V ± 10%)

Parameter		*Symbol*	*Test Condition*	*min*	*max*	*Unit*
Input Leakage Current	A0-A14, $\overline{OE}$	I_{LI1}	V_{IN} = GND to V_{CC}+0.75	-	40	µA
	$\overline{CS1\sim4}$, $\overline{WE}$(2)	I_{LI2}	V_{IN} = GND to V_{CC}+0.75	-	10	µA
Output Leakage Current		I_{LO}	$V_{I/O}$ = GND to V_{CC}, $\overline{CS}$(1)=V_{IH}	-	40	µA
Operating Supply Current	32 bit	I_{CC32}	$\overline{CS}$(1)=$\overline{OE}$=V_{IL}, $\overline{WE}$(2)=V_{IH}, I_{OUT}=0mA, f=5MHz	-	320	mA
	16 bit	I_{CC16}	As above	-	166	mA
	8 bit	I_{CC8}	As above	-	89	mA
Standby Supply Current	TTL levels	I_{SB1}	$\overline{CS}$(1)= 2.0V to V_{CC}+0.75V	-	12	mA
	CMOS levels	I_{SB2}	$\overline{CS}$(1)= -0.3V to V_{CC}+0.75V	-	1.2	mA
Output Low Voltage		V_{OL}	I_{OL}=6.0mA.	-	0.45	V
Output High Voltage		V_{OH}	I_{OH}=-4.0mA.	2.4	-	V

Notes (1) $\overline{CS}$ above are accessed through $\overline{CS1\text{-}4}$. These inputs must be operated simultaneously for 32 bit operation, in pairs in 16 bit mode and singly for 8 bit mode.

(2) $\overline{WE}$ above refers to $\overline{WE1\sim4}$ on the PUMA 67E1001A version. Additionally, $\overline{WE1\sim4}$ are accessed as in note (1) above.

Capacitance (T_A=25°C, f=1MHz) Note: These parameters are calculated, not measured.

Parameter		*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance	$\overline{CS1\sim4}$, $\overline{WE1\sim4}$(1)	C_{IN1}	V_{IN}=0V	-	16	pF
	Address, $\overline{OE}$, $\overline{WE}$	C_{IN2}	V_{IN}=0V	-	34	pF
Output Capacitance	32 Bit mode	C_{OUT}	V_{OUT}=0V	-	22	pF

AC READ CHARACTERISTICS

Read Cycle

Parameter	Symbol	90 min	90 max	12 min	12 max	Unit
Read Cycle Time	t_{RC}	-	90	-	120	ns
Address to Output Delay	t_{ACC}	-	90	-	120	ns
$\overline{CS}$ to Output Delay(1)	t_{CS}	-	90	-	120	ns
$\overline{OE}$ to Output Delay(2)	t_{OE}	0	45	0	50	ns
$\overline{CS}$ or $\overline{OE}$ to Output Float(3,4)	t_{DF}	0	45	0	50	ns
Output Hold from $\overline{OE}$, $\overline{CS}$ or Address, (whichever occured first)	t_{OH}	0	-	0	-	ns

Notes: (1) $\overline{CS}$ may be delayed up to $t_{ACC} - t_{CS}$ after the address transition without impact on t_{ACC}.
(2) $\overline{OE}$ may be delayed up to $t_{CS} - t_{OE}$ after the falling edge of $\overline{CS}$ without impact on t_{CS} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
(3) t_{DF} is specified from $\overline{OE}$ or $\overline{CS}$ whichever occurs first.
(4) This parameter is only sampled and is not 100% tested.

Write Cycle

Parameter	Symbol	min	typ	max	Unit
Address, $\overline{OE}$ Set-up Time	t_{AS}, t_{OES}	0	-	-	ns
Address Hold Time	t_{AH}	50	-	-	ns
Chip Select Set-up Time	t_{CS}	0	-	-	ns
Chip Select Hold Time	t_{CH}	0	-	-	ns
Write Pulse Width ($\overline{WE}$ or $\overline{CS}$)	t_{WP}	100	-	-	ns
Data Set-up Time	t_{DS}	50	-	-	ns
Data, $\overline{OE}$ Hold Time	t_{DH}, t_{OEH}	0	-	-	ns
Time to Data Valid	t_{DV}	NR(1)	-	-	ns

Note: (1) NR = No Restriction

Page Mode Write Cycle

Parameter	Symbol	min	typ	max	Unit
Write Cycle Time	t_{WC}	-	5	10	ms
Address Set-up Time	t_{AS}	0	-	-	ns
Address Hold Time	t_{AH}	50	-	-	ns
Data Set-up Time	t_{DS}	50	-	-	ns
Data Hold Time	t_{DH}	0	-	-	ns
Write Pulse Width	t_{WP}	100	-	-	ns
Byte Load Cycle Time	t_{BLC}	-	-	150	µs
Write Pulse High Width	t_{WPH}	50	-	-	ns

DATA Polling Characteristics(1)

Parameter	Symbol	min	typ	max	Unit
Data Hold Time	t_{DH}	0	-	-	ns
$\overline{OE}$ Hold Time	t_{OEH}	0	-	-	ns
$\overline{OE}$ to Output Delay	t_{OE}	-	-	70	ns
Write Recovery Time	t_{WR}	0	-	-	ns

Note : (1) These parameters are sampled and not 100% tested.

Toggle Bit Characteristics[1,2,3,4]

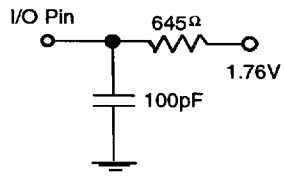
Parameter	*Symbol*	*min*	*typ*	*max*	*Unit*
Data Hold Time	t_{DH}	10	-	-	ns
$\overline{OE}$ Hold Time	t_{OEH}	10	-	-	ns
$\overline{OE}$ to Output Delay	t_{OE}	-	-	70	ns
$\overline{OE}$ High Pulse	t_{OEH}	150	-	-	ns
Write Recovery Time	t_{WR}	0	-	-	ns

Note : (1) These parameters are sampled and not 100% tested.
(2) Toggling either $\overline{OE}$ or $\overline{CS}$, or both $\overline{OE}$ and $\overline{CS}$ will operate toggle bit.
(3) Beginning and ending state of I/O6 will vary.
(4) Any address location may be used but the address should not vary.

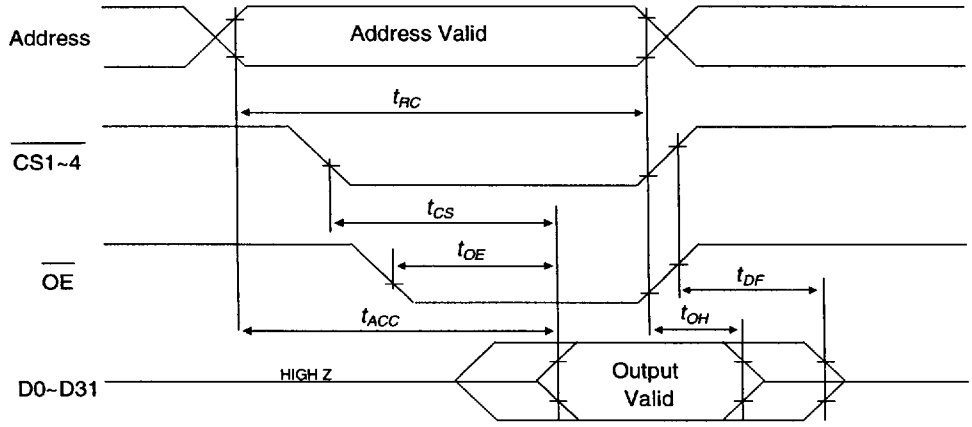
AC Test Conditions

* Input pulse levels: 0V to 3.0V
* Input rise and fall times: 5ns
* Input and Output timing reference levels: 1.5V
* Output load: 1 TTL gate + 100pF
* V_{CC}=5V±10%

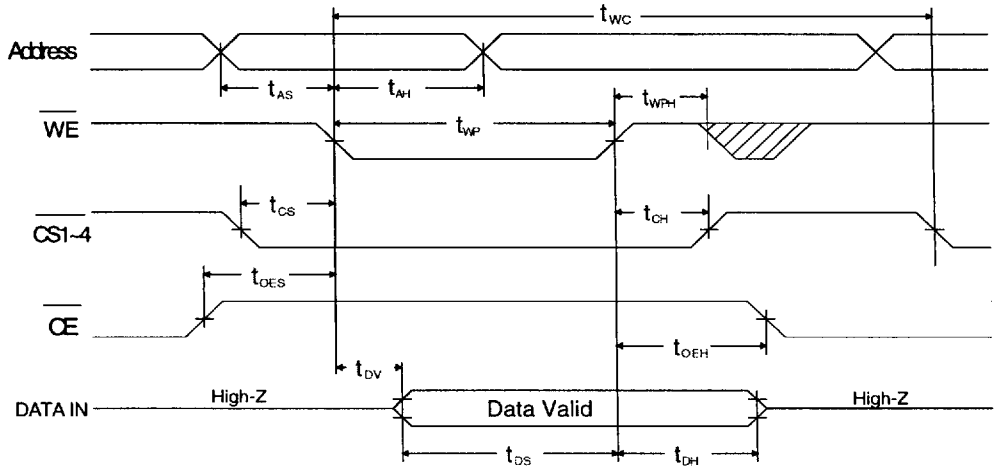
Output Test Load



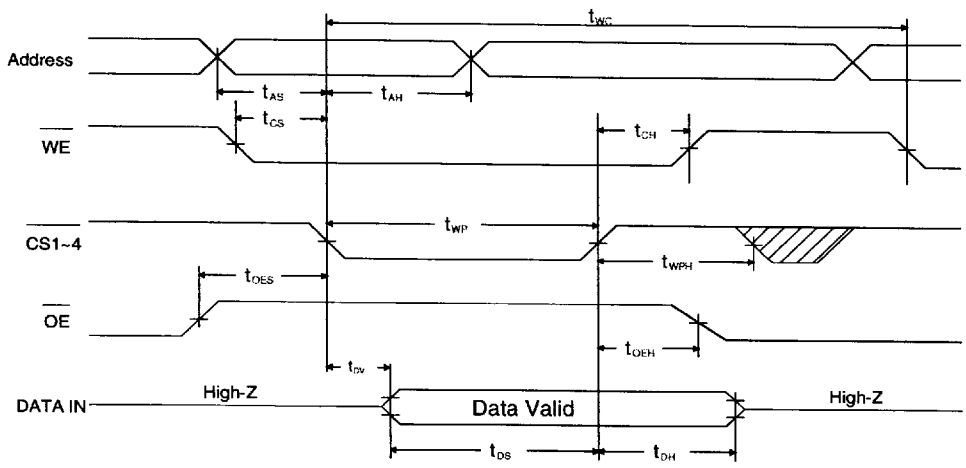
Read Cycle Timing Waveform



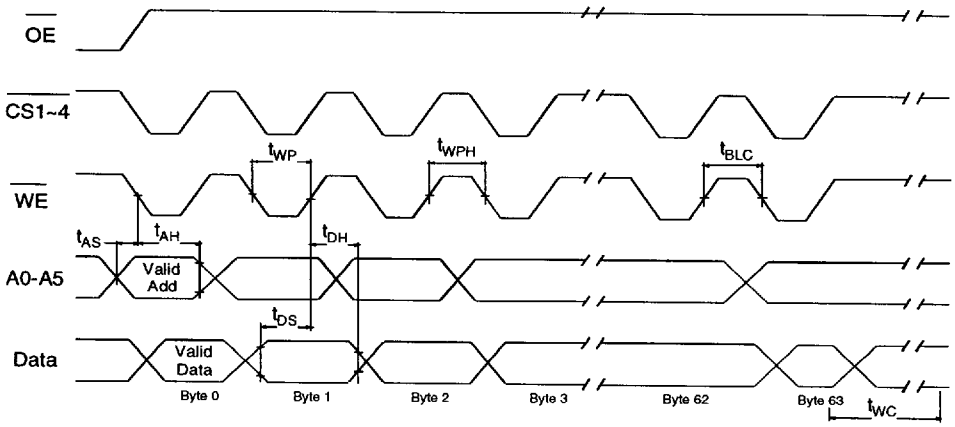
AC Write Waveform - $\overline{WE}$ Controlled (3)



AC Write Waveform - $\overline{CS}$ Controlled (3)

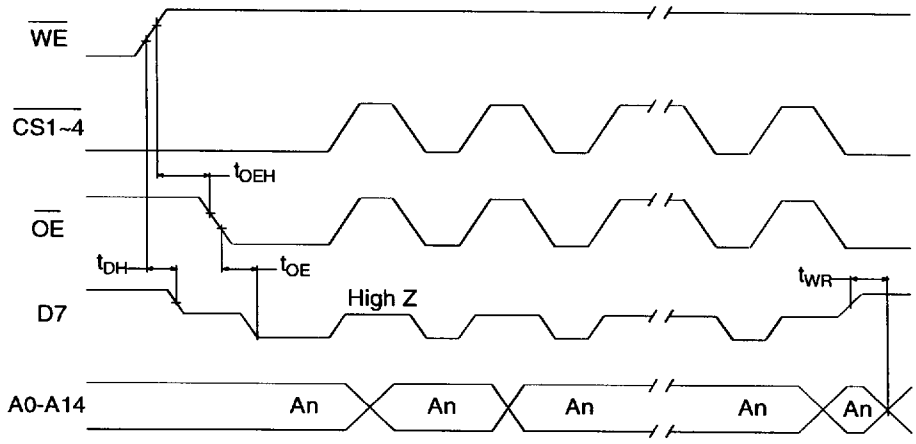


Page Mode Write Waveform (1,2,3)

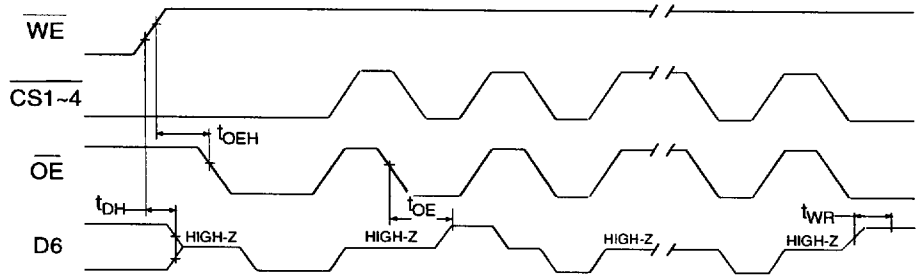


Note: (1) A6 through A14 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CS1~4}$).
(2) $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CS1~4}$ are both low.
(3) $\overline{WE}$ above refers to $\overline{WE1~4}$ on the Puma67E1001A

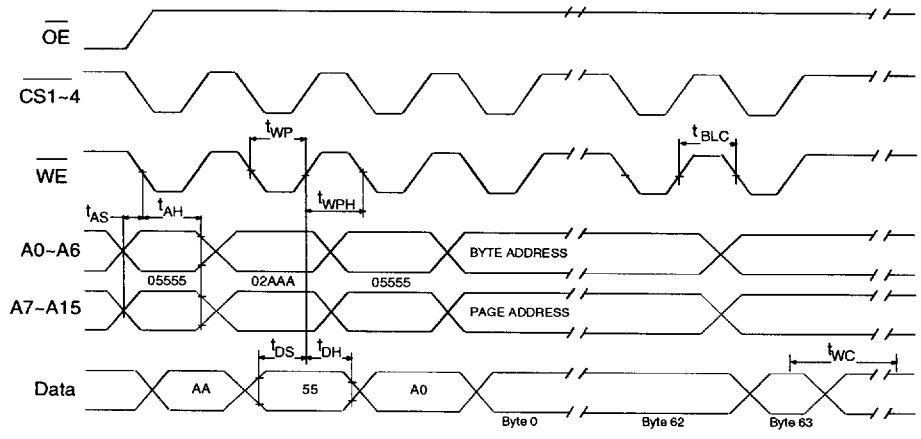
DATA Polling Waveform



Toggle Bit Waveform

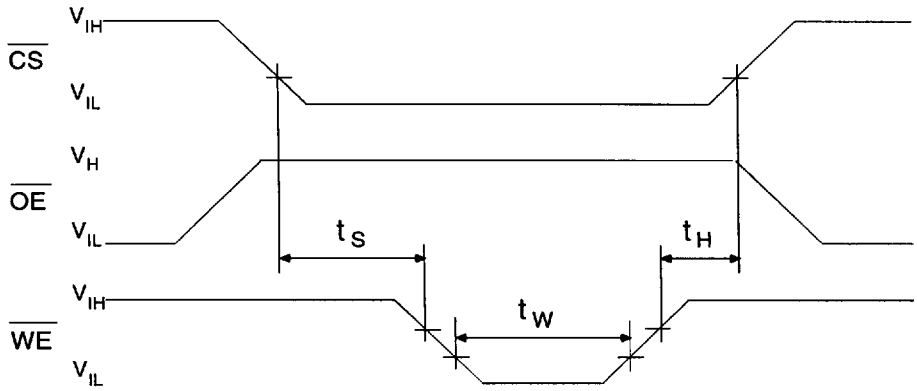


Software Protected Write Waveform(1,2)



Notes: (1) A6 through A14 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CS1\sim4}$).
(2) $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CS1\sim4}$ are both low.

Chip Erase Waveform



$t_S = t_H = 5\mu s$ (min) $t_W = 10$ ms (min) $V_H = 12V \pm 0.5V$

Device Operation

The following description deals with the PUMA 67E1001 device, with the references to $\overline{WE}$ meaning $\overline{WE1\sim4}$ on the PUMA 67E1001A part.

Read

The PUMA 67E1001 read operations are initiated by both Output Enable and Chip Select LOW. The read operation is terminated by either Chip Select or Output Enable returning HIGH. This 2-line control architecture elimanates bus contention in a system environment. The data bus will be in a high impendence state when either Output Enable or Chip Select is HIGH.

Write

Write operations are initated when both Chip Select and Write Enable are LOW and Output Enable is HIGH. The PUMA 67E1001 supports both a Chip Select and Write Enable controlled write cycle. That is, the address is latched by the falling edge of either Chip Select or Write Enable, whichever occurs last. Similarly, the data is latched internally by the rising edge of either Chip Select or Write Enable, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms.

Page Mode Write

The page write feature of the PUMA 67E1001 allows the entire memory to be written in 2.5 seconds. Page Write allows 64 bytes of data to be written prior to the internal programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address (A6 through A14) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write up to 64 bytes in the same manner as the first byte written. Each successive byte load cycle, started by the Write Enable HIGH to LOW transition, must begin within 150 µs of the falling edge of the preceding Write Enable. If a subsequent Write Enable HIGH to LOW transition is not detected within 150 µs, the internal automatic programming cycle will commence.

DATA Polling

The PUMA 67E1001 features DATA Polling to indicate if the write cycle is completed. During the internal programming cycle, any attempt to read the last byte written will produce the compliment of that data on D7. Once the programming is complete, D7 will refect the true data. Note: If the the PUMA 67E1001 is in a protected state and an illegal write operation is attempted DATA Polling will not operate.

TOGGLE bit

In addition to DATA polling, another method is provided to determine the end of a Write Cycle. During a write operation successive attempts to read data will result in D6 toggling between 1 and 0. Once a write is complete, this toggling will stop and valid data will be read.

Hardware Data Protection

The PUMA 67E1001 provides harware features to protect nonvololitile data from inadvertent writes.

- Noise Protection - A Write Enable pulse less than 15 ns will not inditiate a write cycle.
- Default V_{CC} Sense - All functions are inhabited when $V_{CC} < 3.8$ V.
- Write Inhibit - Holding either Output Enable LOW, Write Enable HIGH or Chip Select HIGH will prevent an inadvertent write cycle during power on or power off, maintaining data integrity.
- At power on, the device times out 5ms before allowing a Write.

Software Data Protection

The PUMA 67E1001 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protect feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the PUMA 67E1001 is also protected against inadvertent and accidental writes in that, the software algorithm must be issued prior to writing additional data to the device.

Operating Modes

The table below shows the logic inputs required to control the operation of the PUMA 67E1001.

MODE	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	OUTPUTS
Read	0	0	1	Data Out
Write	0	I	0	Data in
Standby/Write inhibit	1	X	X	High-Z
Write Inhibit	X	X	1	
	X	0	X	
Output Disable	X	1	X	High-Z
Chip Erase (1)	0	1	0	High-Z

$0 = V_{IL}$: $1 = V_{IH}$: $X = V_{IH}$ or V_{IL}

Notes : (1) $\overline{OE}$ must be 12.0V ± 0.5V

Device Indentification

An extra 64 bytes of EEPROM memory are avaliable to the user for device identification, accessed by placing 12V±0.5V on A9 and using locations $7FC0_H$ to $7FFF_H$. These locations can be used during the initial programming of each EEPROM to record data such as issue number and release date, and subsequent reprogramming can change these locations to record the alterations performed.

Chip Erase

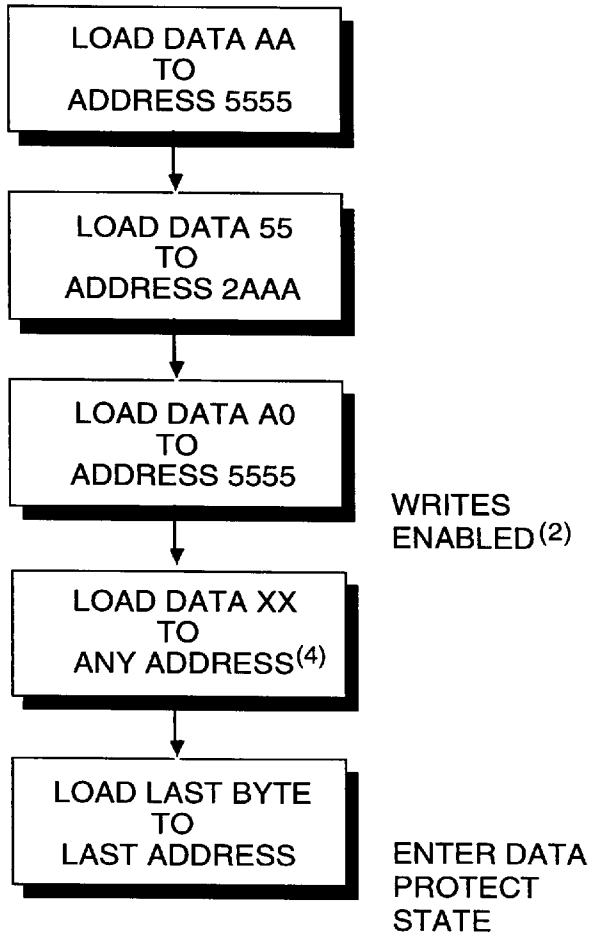
All of the memory locations on the PUMA67E1001 can be erased in 10 ms by placing 12.0V±0.5V onto $\overline{OE}$ and controlling $\overline{WE}$ and $\overline{CS}$ to follow the Chip Erase timing characteristics. This function will operate even if the module is in Software Data Protection Mode as explained later.

Software Algorithms (1)

Selecting the software data protection mode requires the host system to precede datawrite operations by a series of three write operations to three specfic addresses. The three byte sequence opens the page write window enabling the host to write from from 1 to 64 bytes of data. Once the page load cycle has been completed, the device will automatically be returned to the data protected state

Software Data Protection Algorithm

Regardless of wheather the device has been protected or not, once the software data protected aglorithm is used and the data is written, the PUMA 67E1001 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the PUMA 67E1001 will be write protected during power-down and any subsequent power-up.



Notes:

(1) Data Format I/O0 - I/O7 (Hex);
Address format A0 - A14 (Hex)
Once initiated, this sequence of write operations should not be interrupted.

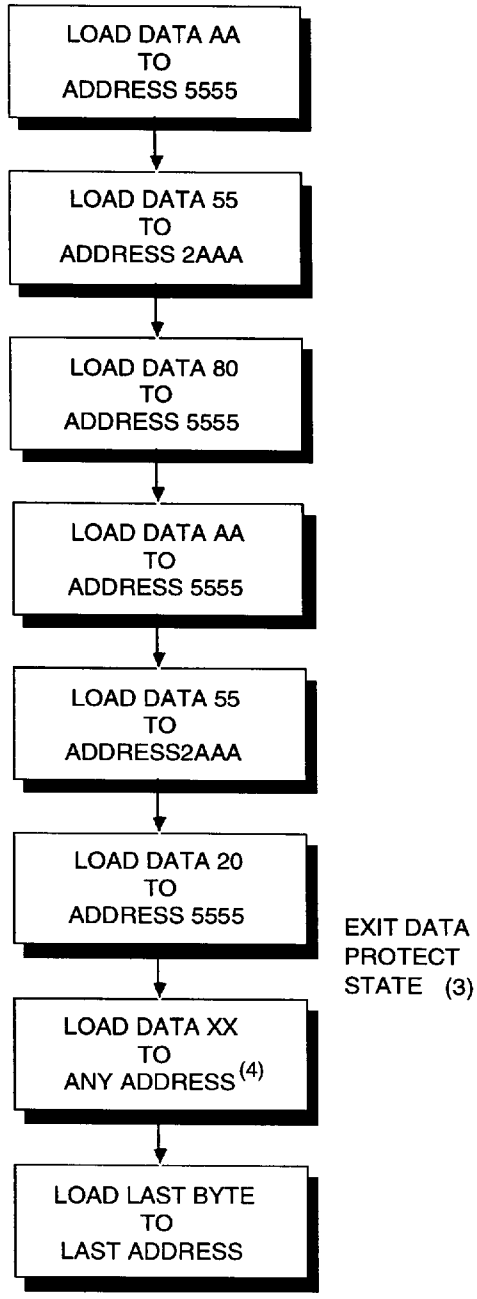
(2) Write Protect state will be activated at end of write even if no other data is loaded.

(3) Write Protect state will be disabled at end of write period even if no other data is loaded.

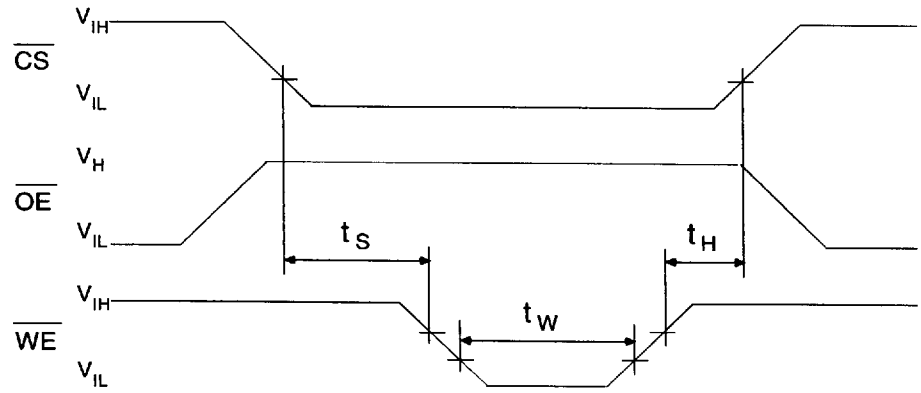
(4) 1 to 64 bytes of data are loaded.

Software Data Protect Disable

In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E²PROM programmer. The following six step algorithm will reset the internal protection circuit. After t_{WC}, the PUMA 67E1001 will be in standard operating mode.

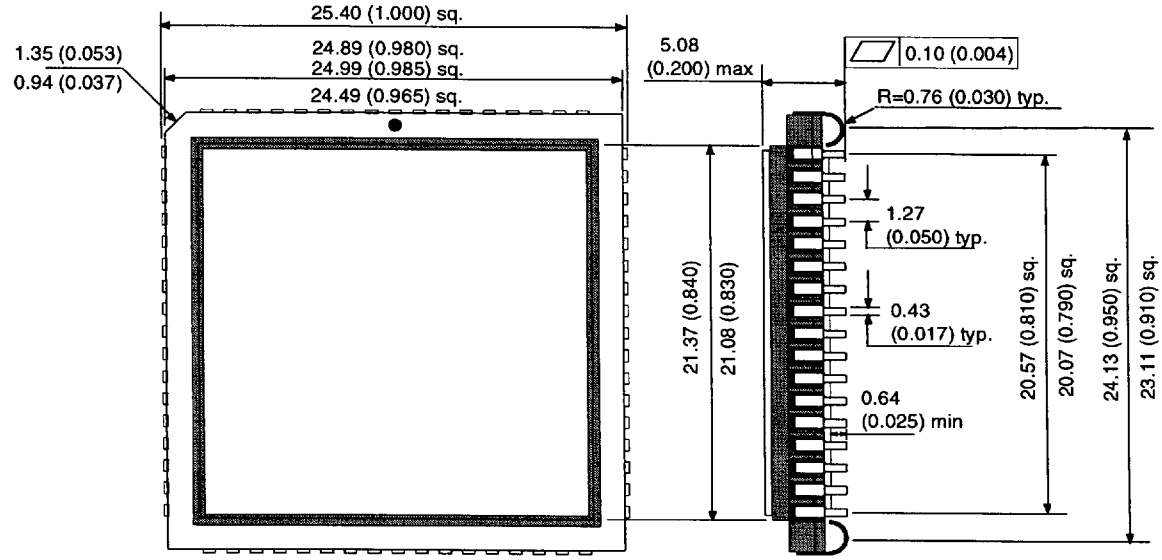


Chip Erase Waveform

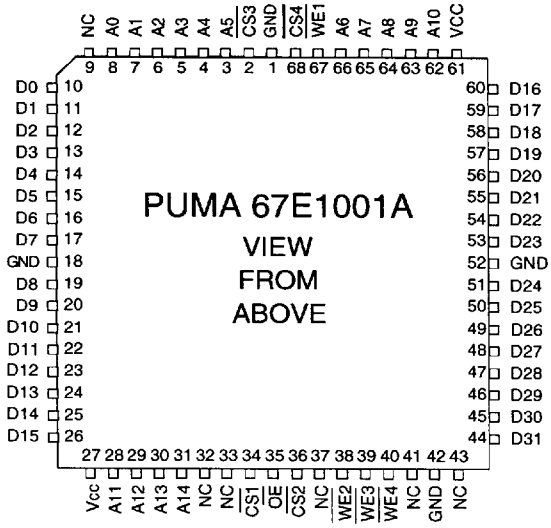


$t_S = t_H = 5\mu s$ (min) $t_W = 10$ ms (min) $V_H = 12V \pm 0.5V$

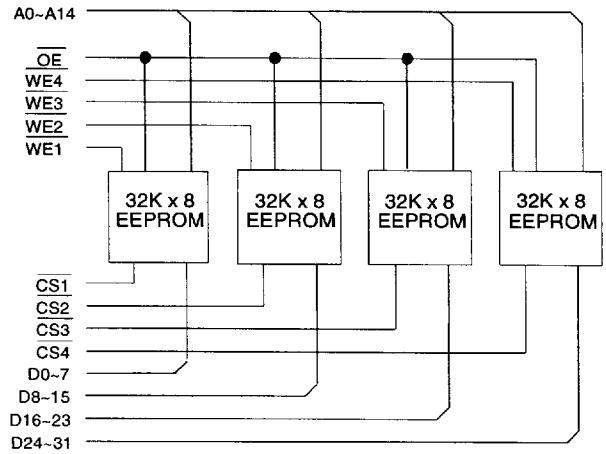
Package Details **Dimensions in inches. Lead finish gold.**



Pin Definifion version A'



Block Diagram version A



Military Screening Procedure

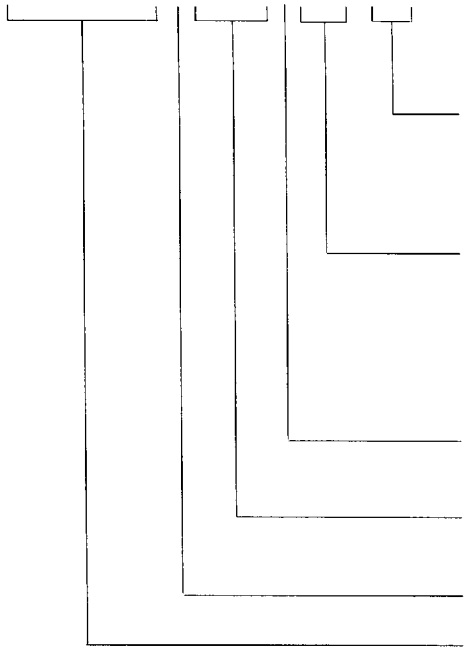
MultiChip Screening Flow for high reliability product is in accordance with Mil-883 method 5004 .

MB MULTICHIP MODULE SCREENING FLOW

SCREEN	*TEST METHOD*	*LEVEL*
Visual and Mechanical		
Internal visual	2010 Condition B or manufacturers equivalent	100%
Temperature cycle	1010 Condition C (10 Cycles, -65°C to +150°C)	100%
Constant acceleration	2001 Condition B (Y1 & Y2) (10,000g)	100%
Endurance		
Write Cycle endurance and Data Retention performance	10000 cycles as per MIL-STD 883 Method 1033 at ambient temperature followed by 72 hours minimum data retention bake at 150C minimum	
Burn-In		
Pre-Burn-in electrical	Per applicable device specifications at T_A=+25°C	100%
Burn-in	T_A=+125°C, 160hrs min	100%
Final Electrical Tests	Per applicable Device Specification	
Static (DC)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Functional	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Switching (AC)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Percent Defective allowable (PDA)	Calculated at post-burn-in at T_A=+25°C	10%
Hermeticity	1014	
Fine	Condition A	100%
Gross	Condition C	100%
Quality Conformance	Group A, B, C, D according to MIL-STD 883 method 5005	Sample
External Visual	2009 Per vendor or customer specification	100%

Ordering Information

PUMA67E1001AMB-90



Speed	90	= 90 ns
	12	= 120ns
Temp. range/screening	Blank	= Commercial Temperature
	I	= Industrial Temperature
	M	= Military Temperature
	MB	= Screened in accordance with MIL-STD-883
Special Features	Blank	= $\overline{WE}$
	A	= $\overline{WE1 \sim 4}$.
Organisation	1001	= 32K x 32, user configurable as 64K x 16 and 128K x 8
Memory Type	E	= EEPROM
Package	PUMA67	= 68 pin "J" Leaded Ceramic Surface Mount Module.