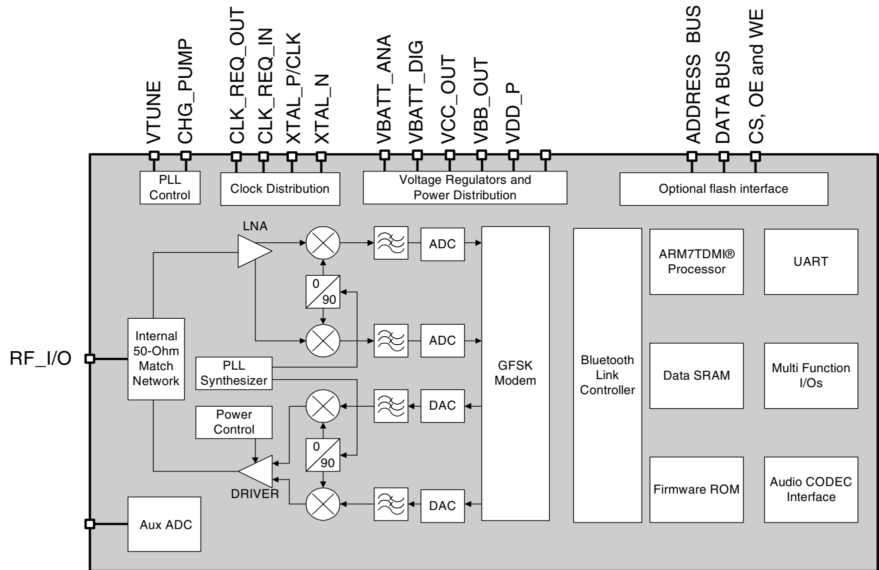
Features

- RF System on Chip (SoC) for Bluetooth wireless technology combining a 2.4 GHz transceiver, baseband processor, and protocol stack ROM.
- Bluetooth specification V1.2 qualified including mandatory and optional functions such as AFH and eSCO.
- Manufactured using standard 0.18-micron CMOS process technology.
- UART based Host Control Interface (HCI) transport layer supports standard and 3-wire modes.
- Direct conversion RF architecture improves receiver-blocking performance.
- I/O voltage supply can range from 1.62 V to 3.63 V.
- -85 dBm receiver sensitivity and +2 dBm transmitter power typical performance specifications.
- Integrated analog and digital voltage regulators simplify system design.
- 50 Ω RF I/O does not need any additional external impedance matching components.
- Flexible reference clock source options including crystal or direct input from the host platform.
- Internal temperature compensated transmitter and receiver circuits deliver consistent performance from -40° to +85°C.
- On-chip ROM software storage with patch capability.

Applications

- Mobile phones and smart phones.
- Bluetooth audio headset.
- Bluetooth hands-free kit.



Block Diagram

Product Description

The UltimateBlue SiW3500™ is a RF System On Chip (SoC) that combines a 2.4 GHz transceiver, baseband processor, and protocol stack software for Bluetooth® wireless technology. Due to its low power CMOS process, the SiW3500 is ideally suited for applications such as mobile phones, audio headsets, and other embedded products.

The SiW3500 integrates an ARM7TDMI processor for software execution from either internal ROM or external FLASH memory. The standard SiW3500 ROM contains the Bluetooth lower layer stack software including the HCI transport driver.

The SiW3500 is packaged in a 6 x 6 Pb-Free 96-VFBGA that meets RoHS (Green) requirements. Known Good Die (KGD) is available for special applications.

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ Si Bi-CMOS
- ☐ GaInP/HBT
- ☐ GaAs HBT
- ☐ SiGe HBT
- ☐ GaN HEMT
- ☐ GaAs MESFET
- ☑ Si CMOS
- ☐ SiGe Bi-CMOS

Ordering Information

SiW3500 UltimateBlue™

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Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

Radio Features

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- On-chip ROM software storage with patch capability.

Baseband Features

- Hardware based GFSK MODEM and packet processing contributes to lower system current consumption with minimal software overhead.
- ARM7TDMI processor efficiently executes all protocol stack and application software.
- Software execution from either internal ROM or external FLASH memory. The SiW3500 features a ROM patch mechanism that allows substituting small portions of ROM code with code either downloaded from the host or stored in external EEPROM.
- Extensive multi function I/Os allow flexible product configurations.
- Auxiliary analog-to-digital converter (ADC) is available for applications such as battery level detection.

Standard Protocol Stack Features

- Full-featured lower layer Bluetooth protocol stack software up to the host interface (HCI).
- Bluetooth 1.2 qualified including mandatory and optional features such as AFH, extended SCO, faster connections, and LMP improvements.
- Full Bluetooth connection capabilities with support for piconet and scatternet modes and device scanning during SCO connection.
- Able to establish up to 3 SCO connections simultaneously.
- Supports low power connection states such as hold, sniff, and park modes with selectable sniff intervals.
- Full support of Bluetooth test modes for use during production.
- Verified HCI command level compatibility with multiple upper layer stack software.

Additional Protocol Stack Features

- Proprietary channel assessment algorithm provides fast and accurate determination of occupied channel for use in AFH mode.
- In addition to AFH, UltimateBlue Coexistence Technology is part of the baseline protocol stack. UltimateBlue coexistence minimizes interference to 802.11b/g products.
- The Channel Quality Driven Data Rate (CQDDR) feature optimizes data transfer in noisy or weak signal environments.
- Full selection of upper layer protocol stack software and profiles available for license and customization.

ROM Features	SiW3500 HCI	SiW3500 Headset
Protocol Stack		
Lower stack up to HCI	✓	✓
UltimateBlue Coexistence	✓	✓
Upper Stack (L2CAP, SDP, RFCOMM)	–	✓
Programming Interface (API)	–	✓
Profiles		
Headset Profile (HSP)	–	✓
Hands Free Profile (HFP)	–	✓

✓= Included in SiW3500 ROM

External System Interfaces

Host HCI Transport (UART)

The high speed UART interface provides the physical transport between the SiW3500 and the application host for the transfer of Bluetooth data compliant with the Bluetooth specification. The table below shows the supported configurations. The default baud rate is 115,200 bps and can be set depending on the product.

SiW3500 Radio Processor HCI UART Parameters	Required Host Setting
Number of data bits	8
Parity bit	No parity
Stop bit	1 stop bit
Flow control	RTS/CTS
Host flow-off response requirement from the SiW3500	8 bytes
SiW3500 IC flow-off response requirement from host	2 bytes
Supported baud rates (bps)	9.6k, 19.2k, 38.4k, 57.6k, 115.2k, 230.4k, 460.8k, 500k, 921.6k, 1M, 1.5M, 2M

Host HCI Transport (3-Wire UART)

To reduce the number of signals and to increase the reliability of the HCI UART interface, a 3-wire UART protocol is available in the SiW3500. The protocol is compliant with the Bluetooth specification H:5 transport and backwards compatible with the BCSP 3-wire UART protocol. Selection between H:4 UART, H:5 UART, and BCSP UART is done automatically by the SiW3500.

SiW3500 Radio Processor HCI 3-Wire UART Parameters	Required Host Setting
Number of data bits	8
Parity bit	Even
Stop bit	1 stop bit
Error detection	SLIP and checksum
Sleep modes	Shallow and deep

Audio Codec Interface

The SiW3500 supports direct interface to an external audio CODEC or PCM host device. The interface provides the following configurations:

- Standard PCM clock rates from 64 kHz to 2.048 MHz with multi-slot handshakes and synchronization.
- Supports either master or slave mode.
- Supports any PCM data size up to 16 bits.
- Compatible with Motorola SSI mode.
- Configuration of the CODEC interface is done by the firmware during boot-up using non-volatile memory (NVM) parameters.

Multi-function I/Os (MFPs)

Up to 8 (eight) multi-function I/O ports are available in the SiW3500. The table below identifies the I/Os and their usage.

Multi Function I/O Number	Possible Usage Configuration
MFP[0]	General purpose.
MFP[1]	CLOCK_REQ_IN, HOST_WAKEUP, General purpose.
MFP[2]	Address A[18], SYNC_CLOCK, AUX_RTS, General purpose.
MFP[3]	FREQ_SEL[3], SYNC_DATA, General purpose.
MFP[4]	FREQ_SEL[1], General purpose.
MFP[5]	FREQ_SEL[2], General purpose.
MFP[6]	AUX_RXD, General purpose.
MFP[7]	AUX_CTS, TX_RX_SWITCH, General purpose.

External Memory Interface

The SiW3500 does not require additional memory for standard below HCI protocol functions. An external memory interface is available for execution of protocol stack software from FLASH memory if desired. If external FLASH memory will be used, the read access time of the device must be 100 ns or less.

Auxiliary UART

The SiW3500 can be configured and enabled with an auxiliary UART port. This UART port can be used for debug depending on the application software.

Signal	Description
AUX_TXD	TX Data
AUX_RXD	RX Data
AUX_CTS	Clear To Send
AUX_RTS	Request To Send

External Power Amplifier Interface

The SiW3500 supports the use of an external power amplifier for +20 dBm designs. When enabled, these signals provide an integrated interface for the control of an external PA.

Signal	Description
IDAC	Power control to external PA. This output provides a variable current source that can be used to control the external PA. Leave unconnected if not used
TX_RX_SWITCH	Output signal used to indicate the state of the radio. This could be used as a direction control for the PA. The polarity is programmable with the default set as: Low = Transmit; High = Receive.

Power Management

The HOST_WAKEUP and EXT_WAKE signals are used for power management control of the SiW3500. HOST_WAKEUP is an output signal used to indicate Bluetooth activity to the host. EXT_WAKE is an input signal used by the host to wake up the SiW3500 from sleep mode.

For control of the reference clock source, CLOCK_REQ_IN and CLOCK_REQ_OUT can be made available to turn on/off an external reference clock source.

General-Purpose Analog to Digital Converter (ADC)

The SiW3500 incorporates a general-purpose ADC that can be enabled to sample external analog voltage. The ADC has an 8-bit resolution.

External EEPROM Controller and Interface

This interface is intended for communication to an optional EEPROM when using the SiW3500 in ROM mode. The EEPROM is not required for configurations with external flash. The EEPROM is the non-volatile memory (NVM) in the system and contains the system configuration parameters such as the Bluetooth device address, the CODEC type, as

well as other parameters. These default parameters are set at the factory, and some parameters will change depending on the system configuration. Optionally, the memory parameters can be downloaded from the host processor at boot up eliminating the need for EEPROM. Please consult the Application Support team for details. The EEPROMs should have a serial I^2C interface with a minimum size of 2 Kbits and 16-byte page write buffer capabilities.

General System Requirements

System Reference Clock

The SiW3500 chip can use either an external crystal or a reference clock as the system clock input. A partial list of supported frequencies (in MHz) includes: 9.6, 12, 12.8, 13, 14.4, 15.36, 16, 16.8, 19.2, 19.68, 19.8, 26, 32, 38.4, and 48. For other frequencies, please contact Applications Support. The system reference crystal/clock must have an accuracy of ±20 PPM or better to meet the Bluetooth specification.

Low Power Clock

For the Bluetooth low power clock, a 32.768 kHz crystal can be used to drive the SiW3500 oscillator circuit, or alternatively, a 32.768 kHz reference clock signal can be used instead of a crystal. If the lowest power consumption is not required during low-power modes such as sniff, hold, park, and idle modes, the 32.768 kHz crystal may be omitted in the design.

If the 32.768 kHz clock source is used, the clock source should be connected to the CLK32_IN pin and must meet the following requirements:

- For AC-coupled via 100 pF or greater (peak-to-peak voltage):
  400 mV_{P-P} < CLK32_IN < V_{DD_C}
- For DC-coupled:
  CLK32_IN minimum peak voltage < V_{IL}
  CLK32_IN maximum peak voltage > V_{IH}
  Where $V_{IL} = 0.3 * V_{DD_C}$
  Where $V_{IH} = 0.7 * V_{DD_C}$
- For both cases, the signal is not to exceed:
  -0.3 V < CLK32_IN < V_{DD_C} + 0.3 V

Power Supply Description

The SiW3500 operates at 1.8 V core voltage for internal analog and digital circuits. The chip has internal analog and digital voltage regulators simplifying power supply requirements to the chip. The internal voltage regulators can be supplied directly from a battery or from other system voltage sources. Optionally, the internal regulators can be bypassed if a 1.8 V regulated source is available on the system.

Function	Internal Analog Regulator	Internal Digital Regulator
Regulator input pin	V_{BATT_ANA} = 2.3 to 3.63 V	V_{BATT_DIG} = 2.3 to 3.63 V
Regulator output pin	V_{CC_OUT} = 1.8 V	V_{DD_C} = 1.8 V

Internal Regulator Used

Function	Analog Core Circuits	Digital Core Circuits
Circuit voltage supply pin	V_{CC} = 1.8 V	V_{DD_C} = 1.8 V

Internal Regulator Bypassed

Note: Both regulators can be bypassed if external regulation is desired. When bypassing the analog regulator, the VBATT_ANA and VCC_OUT pins must be tied together and the external analog voltage (1.8 V) should be applied to the VBATT_ANA pin. When bypassing the digital regulator, the VBATT_DIG pin should be left unconnected and the external digital voltage (1.8 V) should be applied to VBB_OUT pin.

The power for the I/Os is taken from two separate sources (V_{DD_P} and $V_{DD_P_ALT}$). They can range from 1.62 to 3.63 Volts to maintain compatibility with a wide range of peripheral devices. Please check the pin list for the exact pins that are powered from the V_{DD_P} and $V_{DD_P_ALT}$ sources.

RF I/O Description

The SiW3500 employs single-ended RF input and output pins for reduced external components. In typical Class 2 (0 dBm nominal) applications, no external matching components are necessary.

On-Chip Memory

The SiW3500 Radio Processor integrates both SRAM and ROM. The ROM is pre-programmed with Bluetooth protocol stack software (HCI software) and boot code that executes automatically upon reset. The boot code serves to control the boot sequence as well as to direct the execution to the appropriate memory for continued operation.

Configuration Selection

Reference Frequency Selection

The SiW3500 is designed to operate with multiple reference frequencies. During boot, specific frequency select I/O pins are sampled to determine the default reference frequency. The reference frequency setting will be set according to the following table:

FREQ_SEL3 (MFP[3])	FREQ_SEL2 (MFP[5])	FREQ_SEL1 (MFP[4])	FREQ_SEL0 (ADC_IN)	Frequency
0	0	0	0	15.36 MHz
0	0	0	1	19.2 MHz
0	0	1	0	19.44 MHz
0	0	1	1	19.68 MHz
0	1	0	0	19.8 MHz
0	1	0	1	26 MHz
0	1	1	0	38.4 MHz
0	1	1	1	Do not program frequency (leave as ref/2 and set according to system parameters).
1	0	X	X	32 MHz
1	1	0	0	32 MHz
1	1	0	1	12 MHz
1	1	1	0	13 MHz
1	1	1	1	14.4 MHz

Application Software Memory Selection

The SiW3500 can support application (protocol stack) software execution from internal ROM or external FLASH memory. To run from internal ROM, pins D[9] and D[10] must be connected together as shown in the application circuit section of this document (Application Circuit). To run from external flash memory, the flash must be connected as shown in the application circuit diagram and contain valid application code. If the external memory does not have valid program data, the device enters a download mode in which a valid program may be loaded into the external memory through a sequence of commands over the HCI transport layer.

Pin Description

The following table provides detailed listings of pin descriptions arranged by functional groupings.

Name	Pad Type	Ball	Bump See Note 1	Description
Radio (Power from VCC)				
RF_IO	Analog	A2	92	RF signal. Input and output.
TX_BIAS	Analog	A4	89	Internal transmitter driver bias.
VTUNE	Analog	A6	85	Pin for reference PLL loop filter, only used if reference frequency is not integer multiples of 4 MHz.
CHG_PUMP	Analog	F1	10	Pin for RF loop filter.
XTAL_N	Analog	B7	82	System clock crystal negative input. If a reference clock is used, this pin should be left unconnected.
XTAL_P/CLK	Analog	A7	83	System clock crystal positive input or reference clock input.
IDAC	Analog	B1	1	Power control to external power amplifier. This output provides a variable current source that can be used to control the external power amp. Leave unconnected if not used.
ADC_IN	Analog	J2	19	Analog to digital converter input or FREQ_SEL_(0).
VREFN_CAP	Analog	C2	3	Decoupling capacitor for internal A/D converter voltage reference.
VREFP_CAP	Analog	C1	2	Decoupling capacitor for internal A/D converter voltage reference.
Low Power Oscillator and Reset (Power from VDD_P_ALT)				
CLK32K_IN	Analog	L1	21	For crystal or external clock input (32.768 kHz).
CLK32K_OUT	Analog	K1	20	Drive for crystal.
RESET_N	CMOS input	G1	12	System level reset (active low).
Power Control Interface (Power from VDD_P)				
PWR_REG_EN	CMOS bi-directional	G2	14	CLOCK_REQ_OUT control line for external TCXO by default, or can be used as enable for an external voltage regulator. Programmable active high or active low.
AUX_TXD	CMOS bi-directional	G9	58	Auxiliary UART serial port output.
Multi-function (MFP) I/O (Power from VDD_P)				
MFP [0]	CMOS bi-directional	F3	15	Multi-function I/O port.
MFP [1]	CMOS bi-directional	J1	17	Multi-function I/O port.
MFP [2]	CMOS bi-directional	L6	35	Multi-function I/O port.
MFP [3]	CMOS bi-directional	F10	59	Multi-function I/O port.
MFP [4]	CMOS bi-directional	B9	76	Multi-function I/O port.
MFP [5]	CMOS bi-directional	C8	77	Multi-function I/O port.
MFP [6]	CMOS bi-directional	C7	80	Multi-function I/O port.
MFP [7]	CMOS bi-directional	C6	81	Multi-function I/O port.
PCM Interface (Power from VDD_P_ALT)				
PCM_IN	CMOS bi-directional	H3	28	PCM data output from SiW3500.
PCM_OUT	CMOS bi-directional	L2	23	PCM data input to SiW3500.
PCM_CLK	CMOS bi-directional	K3	25	PCM synchronous data clock to the remote device. Normally an output. Input for slave mode.
PCM_SYNC	CMOS bi-directional	K2	22	PCM synchronization data strobe to the remote device. Normally an output. Input for slave mode.

Table 1. SiW3500 Radio Processor Pin List

Name	Pad Type	Ball	Bump See Note 1	Description
UART Interface (Power from VDD_P_ALT)				
UART_RXD	CMOS input	G3	24	UART receive data.
UART_TXD	CMOS output	L4	29	UART transmit data.
UART_CTS	CMOS input	H2	18	UART flow control clear to send.
UART_RTS	CMOS output	H1	16	UART flow control ready to send.
EXT_WAKE	CMOS input	C5	13	Wake up signal from host.
External Memory Interface (power from VDD_P)				
A[17] A[16] A[15] A[14] A[13] A[12] A[11] A[10] A[9] A[8] A[7] A[6] A[5] A[4] A[3] A[2] A[1]	CMOS output	E11 J11 L5 F11 B8 K6 L7 A10 H11 A11 B11 K9 K7 C10 K10 D10 L11	62 51 32 60 78 36 38 73 54 72 71 44 39 69 46 66 47	Address lines. **Note**: A[17] and A[16] can be used to support an optional external serial EEPROM when using the internal ROM in place of the external Flash memory.
D[15] D[14] D[13] D[12] D[11] D[10] D[9] D[8] D[7] D[6] D[5] D[4] D[3] D[2] D[1] D[0]	CMOS bi-directional	A9 C9 B10 E10 K5 G11 G10 H9 K4 J9 K8 J6 J5 F9 J4 H10	75 74 70 63 33 57 56 55 30 52 43 37 34 61 31 53	Data lines. **Note**: Connect D[9] to D[10] to use internal ROM.
OE_N	CMOS output	L10	45	Output enable for external memory (active low).
WE_N/EEPROM_WP	CMOS output	A8	79	Write enable for external memory (active low).
FCS_N	CMOS output	J10	50	Chip select for external memory (active low).
Power and Ground				
VBATT_ANA	Power	D3	6	Positive supply to internal analog voltage regulator.
VBATT_DIG	Power	L9	42	Positive supply to internal digital voltage regulator.
VCC_OUT	Power	D1	5	Regulated output from internal analog voltage regulator.
VDD_P	Power	D11 K11	65 48	Positive supply for external memory interface and some digital I/Os.
VDD_C	Power	C11 L8	68 41	Positive supply for digital circuitry or output of internal digital voltage.

Table 1. SiW3500 Radio Processor Pin List (Continued)

Name	Pad Type	Ball	Bump See Note 1	Description
VCC	Power	A1 B6 C4 E1 E3	94 84 88 7 9	Positive supply for RF and analog circuitry.
VSS_P	GND	J8 E9	49 64	Ground connections for VDD_P.
VDD_P_ALT	Power	L3	26	Positive supply for UART, CODEC, and other digital I/Os.
VSS_P_ALT	Ground	J3	27	Ground connection for VDD_P_ALT.
GND	GND	A3 A5 B2 B3 B4 B5 C3 D2 E2 F2 D9 J7	91 86 93 NA 90 87 NA 4 8 11 67 40	Ground connections for RF and analog circuitry.
1. Bump number information is provided as a reference to the Known Good Die I/O configuration.				

Table 1. SiW3500 Radio Processor Pin List (Continued)

System Specifications

Absolute Maximum Ratings

Parameter	Description	Min	Max	Unit
V_{DD_C}	Digital circuit supply voltage	-0.3	3.63	V
V_{CC}	Analog circuit supply voltage	-0.3	3.63	V
V_{DD_P}, $V_{DD_P_ALT}$	I/O supply voltage	-0.3	3.63	V
V_{BATT_ANA}	Analog regulator supply voltage	-0.3	3.63	V
V_{BATT_DIG}	Digital regulator supply voltage	-0.3	3.63	V
T_{ST}	Storage temperature	-55	+125	°C
RF_{MAX}	Maximum RF input level	–	+5	dBm

Note: Absolute maximum ratings indicate limits beyond which the useful life of the device may be impaired or damage may occur.

Recommended Operating Conditions

Parameter	Description	Min	Max	Unit
T_{OP}	Operating temperature (industrial grade)	-40	+85	°C
T_{EOP}	Extended operating temperature[1]	-40	+105	°C
V_{BATT_ANA}	Unregulated supply voltage into internal analog regulator	2.3	3.63	V
V_{BATT_DIG}	Unregulated supply voltage into internal digital regulator	2.3	3.63	V
V_{CC}	Regulated supply voltage directly into analog circuits	1.71	1.89	V
V_{DD_C}	Regulated supply voltage directly into digital circuits	1.62	1.98	V
V_{DD_P} , $V_{DD_P_ALT}$	Digital interface I/O supply voltage	1.62	3.63	V

1.The extended operating temperature range applies to special order devices qualified for extended operating range. Please contact factory for details.

ESD Rating

Symbol	Description	Rating
ESD	ESD protection - all pins	2000 V

Note: This device is a high performance RF integrated circuit with an ESD rating of 2,000 volts (HBM conditions per Mil-Std-883, Method 3015). Handling and assembly of this device should only be done using appropriate ESD controlled processes.

Electrical Characteristics

DC Specification (T_{OP}=+25°C, V_{DD_P}=3.0V)

Symbol	Description	Min.	Typ	Max.	Unit
V_{IL}	Input low voltage	GND-0.1	–	$0.3 \cdot V_{DD_P}$	V
V_{IH}	Input high voltage	$0.7 \cdot V_{DD_P}$	–	V_{DD_P}	V
V_{OL}	Output low voltage	GND	–	$0.2 \cdot V_{DD_P}$	V
V_{OH}	Output high voltage	$0.8 \cdot V_{DD_P}$	–	V_{DD_P}	V
I_{OH}	Output high current	–	1	–	mA
I_{OL}	Output low current	–	1	–	mA
I_{ILI}	Input leakage current	–	1	–	µA

AC Characteristics (T_{OP}=+25°C, V_{DD_P}=3.0V, C_{LOAD}=15pF)

Symbol	Description	Typ	Max.	Unit
t_r	Rise time	5	11	ns
t_f	Fall time	5	8	ns

Current Consumption (T_{OP}=+25°C, V_{BATT}=3.0V using internal regulators)

Operating Mode	Average	Max	Unit
Standby	40	80	µA
Continuous transmit*	48	55	mA
Continuous receive*	54	60	mA
Parked slave, 1.28 sec. interval	90	–	µA
Inquiry scan, 1.28 sec interval	440	–	µA
Page scan, 1.28 sec. interval	560	–	µA
ACL connection, sniff mode, 40 ms interval	1.3	–	mA
ACL data transfer 723 kbps TX, 57 kbps RX	42	–	mA
SCO connection, HV3 packets	22	–	mA

*Note: Continuous transmit and receive currents are measured in operating modes where there is no activity in baseband digital circuits.

Digital Regulator Specification (T_{OP} = 25°C)

Parameter	Description	Min	Typ	Max	Unit
Output voltage	(I_{OUT} = 10 mA)	1.62	1.80	1.98	V
Line regulation	(I_{OUT} = 0 mA, V_{BATT_DIG} = 2.3 V to 3.63 V)	–	8.0	–	mV
Load regulation	(I_{OUT} = 3 mA to 80 mA)	–	9.0	–	mV
Dropout voltage	(I_{OUT} = 10 mA)	–	–	250	mV
Output maximum current	Maximum supplied current while maintaining regulation	–	–	80	mA
Quiescent current	Off current	–	10	–	µA
Ripple rejection	f_{RIPPLE} = 400 Hz	–	40	–	dB

Radio Specification

Parameter	Description	Min	Typ	Max	Unit
VCO Operating Range	Frequency	2402	–	2480	MHz
PLL lock time	Average tune time	–	60	100	µs

Receiver Specification[1] (V_{BATT}=3.3V, V_{CC}=internal analog regulator output, T_{OP} = 25°C)

Parameter	Description	Min	Typ	Max	Unit
Receiver sensitivity	BER < 0.1%	–	-85	-78	dBm
Maximum usable signal	BER < 0.1%	-10	0	–	dBm
C/I co-channel (0.1% BER)	Co-channel selectivity	–	+8.0	+10.0	dB
C/I 1 MHz (0.1% BER)	Adjacent channel selectivity	–	-4.0	-3.0	dB
C/I 2 MHz (0.1% BER)	2nd adjacent channel selectivity	–	-38.0	-35.0	dB
C/I ≥ 3 MHz (0.1% BER)	3rd adjacent channel selectivity	–	-43.0	-40.0	dB
Out-of-band blocking[2]	Fc/3	-23	–	–	dBm
	Fc/2	-25	–	–	dBm
	2 * Fc/3	-45	–	–	dBm
	30 MHz - 2000 MHz	-10	–	–	dBm
	2000 MHz - 2399 MHz	-27	–	–	dBm
	2498 MHz - 3000 MHz	-27	–	–	dBm
	3000 MHz - 12.75 GHz	-10	–	–	dBm
Intermodulation	Max interferer level to maintain 0.1% BER, interference signals at 3 and 6 MHz offset.	-39	-36	–	dBm
Receiver spurious emission	30 MHz to 1 GHz	–	–	-57	dBm
	1 GHz to 12.75 GHz	–	–	-47	dBm

1. Measured into the chip with 50 Ω source and no bandpass filter.
2. Out-of-band blocking guaranteed by design.

Transmitter Specification[1] (V_{BATT}=3.3V, V_{CC}=internal analog regulator output, T_{OP} = 25°C)

Parameter	Description	Min	Typ	Max	Unit
Output RF transmit power	At maximum power output level	-2	+2	+5	dBm
Modulation Characteristics[2]	$\Delta f1_{avg}$	140	155	175	kHz
	$\Delta f2_{max}$ (For at least 99.9% of all $\Delta f2_{max}$)	115	–	–	kHz
	$\Delta f1_{avg}/\Delta f2_{avg}$	0.8	–	–	kHz
Initial carrier frequency accuracy	–	-75	–	+75	kHz
Carrier frequency drift	One slot packet	-25	–	+25	kHz
	Two slot packet	-40	–	+40	kHz
	Five slot packet	-40	–	+40	kHz
	Max drift rate	–	–	20	kHz/50 µs
20 dB occupied bandwidth	Test per Bluetooth specification	–	–	1000	kHz
In-band spurious emission	2 MHz offset	–	–	-40	dBm
	>3 MHz offset	–	–	-60	dBm
Out-of-band spurious emission	30 MHz to 1 GHz, operating mode	–	–	-55	dBm
	30 MHz to 1 GHz, idle mode	–	–	-57	dBm
	1 GHz to 12.75 GHz, operating mode	–	–	-50	dBm
	1 GHz to 12.75 GHz, idle mode	–	–	-47	dBm
	1.8 GHz to 1.9 GHz	–	–	-62	dBm
	5.15 GHz to 5.3 GHz	–	–	-47	dBm

1. Measured into the chip with 50 Ω source and no bandpass filter.
2. Modulation characteristics as measured per test TRM/CA/07/C as defined in the Bluetooth test specification.

Industrial Temperature Performance[1] (V_{BATT}=2.3 – 3.63V, V_{CC}=internal analog regulator output, T_{OP} = -40 to +85°C)

Parameter	Description	Min	Typ	Max	Unit
Receiver sensitivity	BER<0.1%	–	-85	-75	dBm
Output RF transmit power	At maximum power output level	-4	+2	+6	dBm
Modulation Characteristics[2]	$\Delta f1_{avg}$	140	155	175	kHz
	$\Delta f2_{max}$ (For at least 99.9% of all $\Delta f2_{max}$)	115	–	–	kHz
	$\Delta f1_{avg}/\Delta f2_{avg}$	0.8	–	–	kHz
Initial carrier frequency accuracy	–	-75	–	+75	kHz
Carrier frequency drift	One slot packet	-25	–	+25	kHz
	Two slot packet	-40	–	+40	kHz
	Five slot packet	-40	–	+40	kHz
	Max drift rate	–	–	20	kHz/50 µs
20 dB occupied bandwidth	Bluetooth specification	–	–	1000	kHz
In-band spurious emission	2 MHz offset	–	–	-40	dBm
	>3 MHz offset	–	–	-60	dBm
Out-of-band spurious emission	30 MHz to 1GHz, operating mode	–	–	-55	dBm
	30 MHz to 1GHz, idle mode	–	–	-57	dBm
	1 GHz to 12.75 GHz, operating mode	–	-70	-50	dBm
	1 GHz to 12.75 GHz, idle mode	–	–	-47	dBm
	1.8 GHz to 1.9 GHz	–	–	-62	dBm
	5.15 GHz to 5.3 GHz	–	–	-47	dBm

1. Measured into the chip with 50 Ω impedance and no bandpass filter. Industrial temperature performance guaranteed by design.
2. The modulation characteristic is measured as per test TRM/CA/07/C defined in the Bluetooth Test Specification.

Analog Voltage Supply Requirements

The SiW3500 processor is designed for use with its own internal low noise analog voltage regulator. This configuration is recommended for all applications. When necessary, the internal analog regulator can be bypassed. In situations where bypassing the internal analog regulator is required, the supply voltage to the analog circuit must satisfy the following requirements to preserve the RF performance characteristics.

Parameter	Description	Min	Max	Unit
VCC	Analog supply voltage to all VCC input pins	1.71	1.89	V
Minimum load current	External regulator current	80	–	mA
Minimum ripple rejection	At 400Hz	40	–	dB
Output noise	Integrated 10 Hz to 80 kHz noise	–	22	mV RMS

External Reference Requirements

It is possible to provide a number of reference frequencies that are typical in most cellular phones directly into ball B7 (XTAL_P/CLK) of the device. Refer to "System Reference Clock" on page 5 for a list of supported reference frequencies.

Parameter	Description	Min	Max	Unit
Phase noise	100 Hz offset	–	-100	dBc/Hz
	1 kHz offset	–	-120	dBc/Hz
	10 kHz offset	–	-140	dBc/Hz
Drive level	AC amplitude	0.5	V_{CC}	V_{P-P}
	DC level[1]	0.3	V_{CC}	V

1.If DC-coupled, the external reference signal voltage must stay within this range at all times.

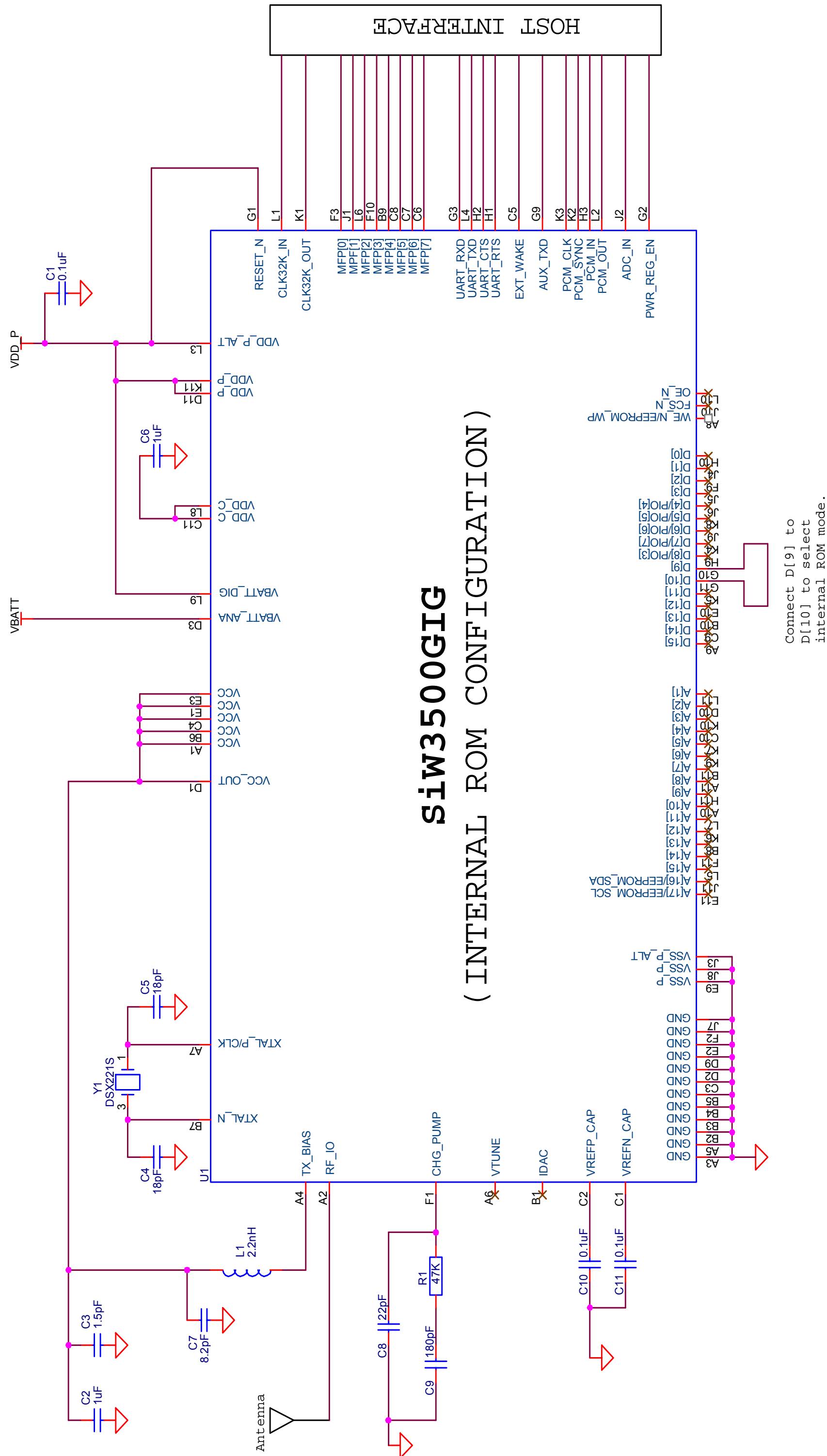
Reference Crystal Requirements

Many reference frequencies are supported by the device. If a crystal is used as the reference frequency source, the typical required parameters are listed below:

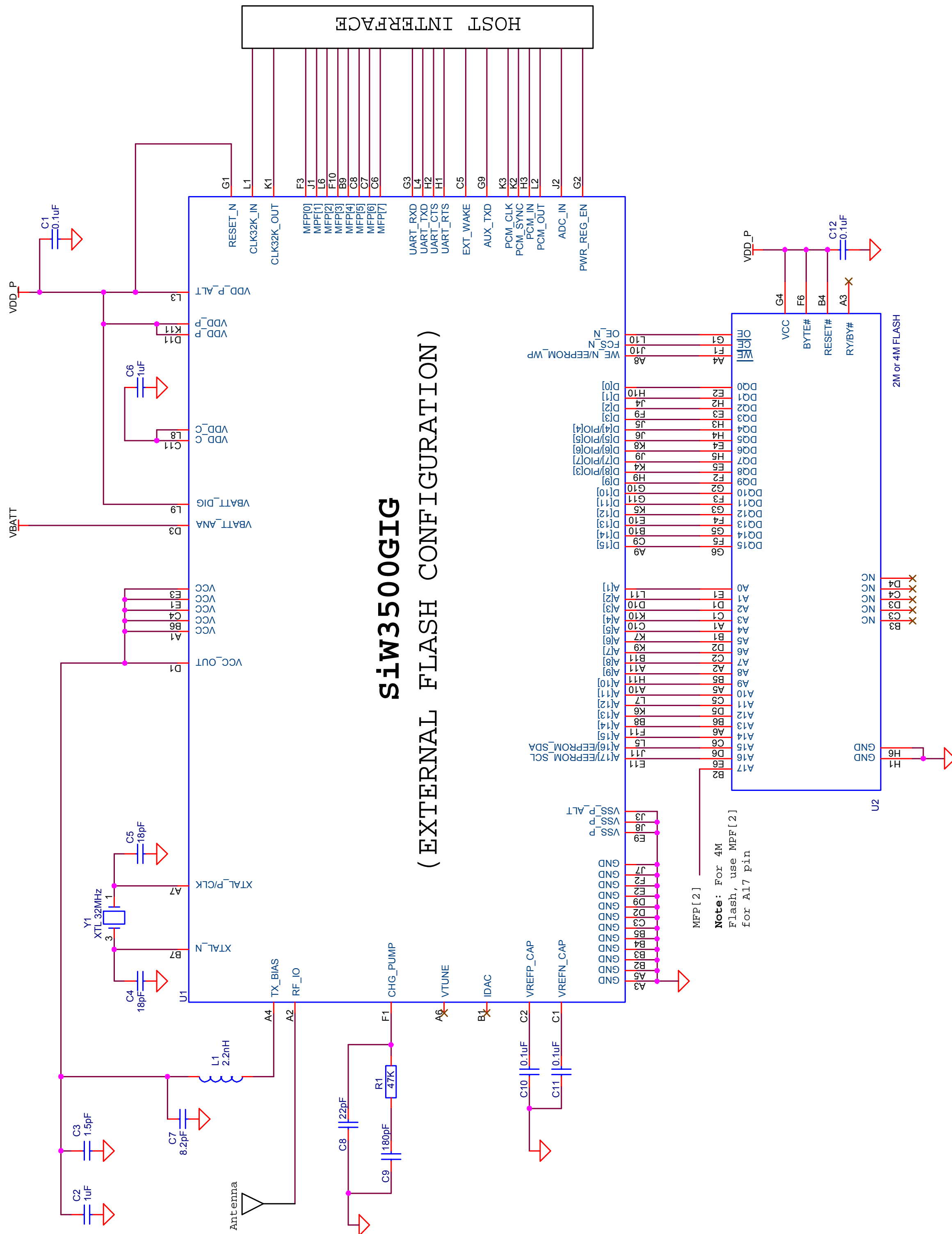
Parameter	Description	Min	Typ	Max	Unit
Drive level	–	–	–	0.3	mW
ESR	Effective serial resistance[1]	–	–	150	Ω
C_O	Holder capacitance[2]	–	3	5	pF
C_L	Load capacitance[3]	–	12	18	pF
C_M	Motional capacitance	–	6	–	fF

1. For 32 MHz crystal.
2. If DC-coupled, the external reference signal voltage must stay within this range at all times.
3. The actual values for C_O and C_L are dependent on the crystal manufacturer and can be compensated for by an internal crystal calibration capability.

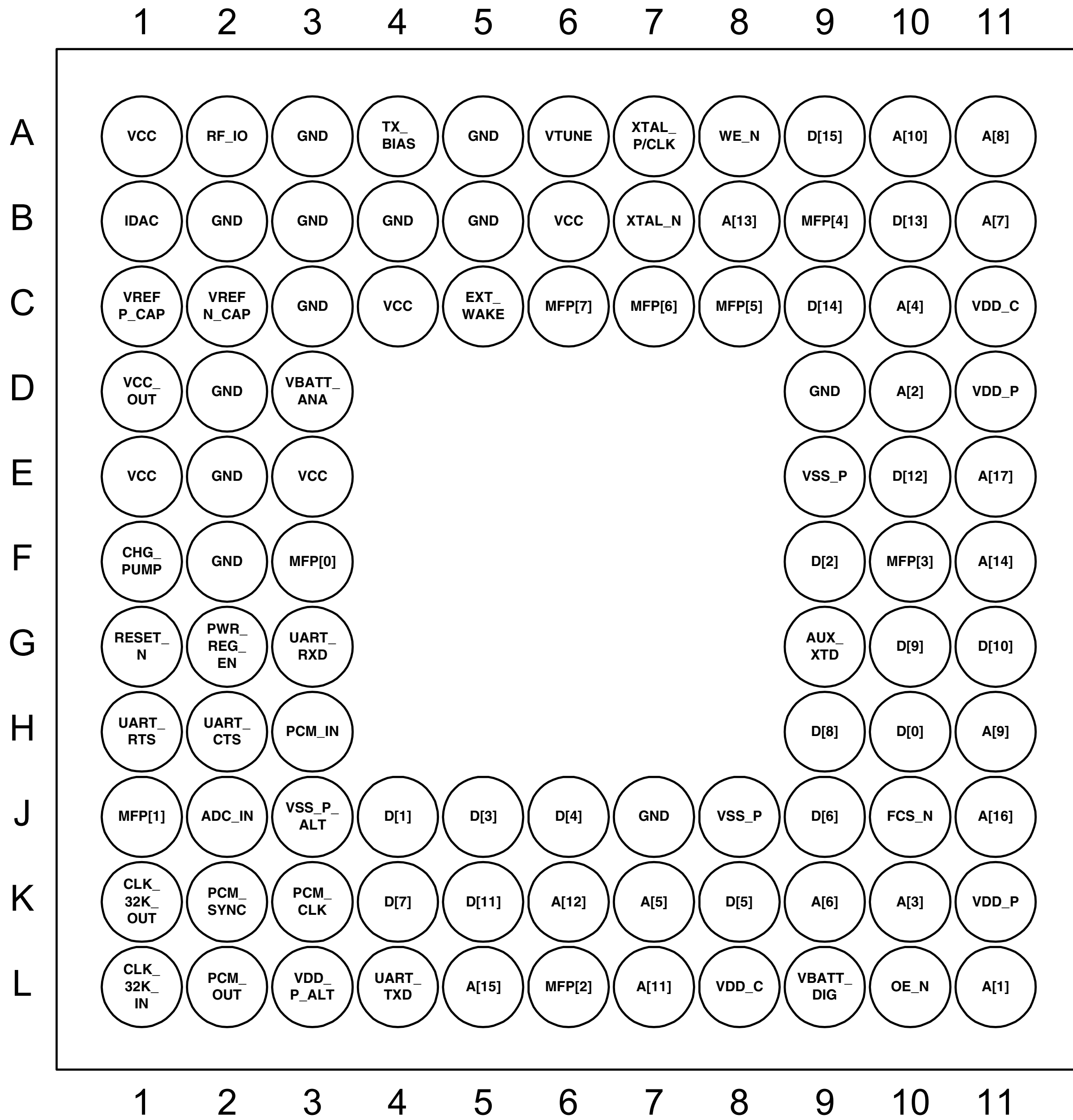
Application Circuit
Internal ROM Version
(for SiW3500GIG VFBGA Package)



Application Circuit
External FLASH Version
(for SiW3500GIG VFBGA Package)

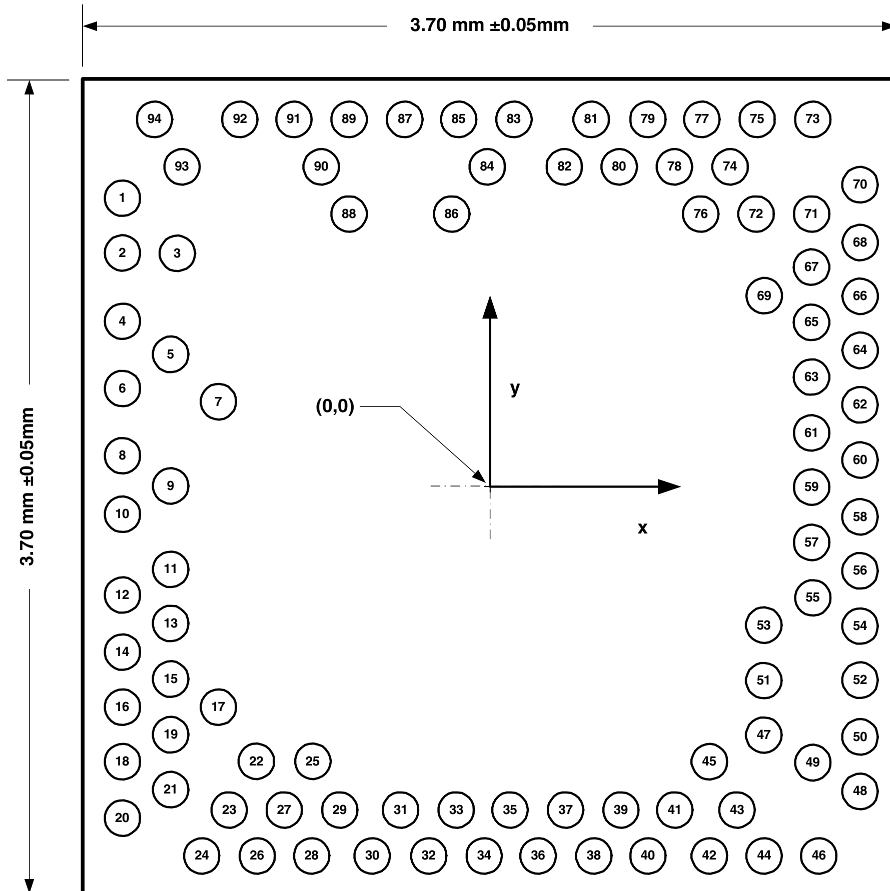


VFBGA I/O Configuration (Top View)



Known Good Die I/O Configuration (Bottom View, Bumped Side)

1. IDAC
2. VREFP_CAP
3. VREFN_CAP
4. GND
5. VCC_OUT
6. VBATT_ANA
7. VCC
8. GND
9. VCC
10. CHG_PUMP
11. GND
12. RESET_N
13. EXT_WAKE
14. PWR_REG_EN
15. MFP[0]
16. UART_RTS
17. MFP[1]
18. UART_CTS
19. ADC_IN
20. CLK32K_OUT
21. CLK32K_IN
22. PCM_SYNC
23. PCM_OUT
24. UART_RXD
25. PCM_CLK
26. VDD_P_ALT
27. VSS_P_ALT
28. PCM_IN
29. UART_TXD
30. D[7]
31. D[1]
32. A[15]
33. D[11]
34. D[3]
35. MFP[2]
36. A[12]
37. D[4]
38. A[11]
39. A[5]
40. GND
41. VDD_C
42. VBATT_DIG
43. D[5]
44. A[6]
45. OE_N
46. A[3]
47. A[1]



48. VDD_P
49. VSS_P
50. FCS_N
51. A[16]
52. D[6]
53. D[0]
54. A[9]
55. D[8]
56. D[9]
57. D[10]
58. AUX_TXD
59. MFP[3]
60. A[14]
61. D[2]
62. A[17]
63. D[12]
64. VSS_P
65. VDD_P
66. A[2]
67. GND
68. VDD_C
69. A[4]
70. D[13]
71. A[7]
72. A[8]
73. A[10]
74. D[14]
75. D[15]
76. MFP[4]
77. MFP[5]
78. A[13]
79. WE_N
80. MFP[6]
81. MFP[7]
82. XTAL_N
83. XTAL_P/CLK
84. VCC
85. VTUNE
86. GND
87. GND
88. VCC
89. TX_BIAS
90. GND
91. GND
92. RF_IO
93. GND
94. VCC

SiW3500 Radio Processor Bump Description and Location

Die Bump No.	Net Name	Ball No. See Note 1	X (µm) See Note 2	Y (µm) See Note 2
1	IDAC	B1	-1675	1316
2	VREFP_CAP	C2	-1675	1066
3	VREFN_CAP	C1	-1425	1061.5
4	GND	D2	-1675	760
5	VCC_OUT	D1	-1458.3	607
6	VBATT_ANA	D3	-1675	454
7	VCC	E1	-1241.75	392
8	GND	E2	-1675	148
9	VCC	E3	-1458.3	7.2
10	CHG_PUMP	F1	-1675	-117.5
11	GND	F2	-1458.3	-367
12	RESET_N	G1	-1675	-492
13	EXT_WAKE	C5	-1458.3	-617
14	PWR_REG_EN	G2	-1675	-742
15	MFP[0]	F3	-1458.3	-867
16	UART_RTS	H1	-1675	-992
17	MFP[1]	J1	-1241.75	-992
18	UART_CTS	H2	-1675	-1242
19	ADC_IN	J2	-1458.3	-1117
20	CLK32K_OUT	K1	-1675	-1492
21	CLK32K_IN	L1	-1458.3	-1367
22	PCM_SYNC	K2	-1064.5	-1241.9
23	PCM_OUT	L2	-1189.5	-1458.45
24	UART_RXD	G3	-1314.5	-1675
25	PCM_CLK	K3	-814.5	-1241.9
26	VDD_P_ALT	L3	-1064.5	-1675
27	VSS_P_ALT	J3	-939.5	-1458.45
28	PCM_IN	H3	-814.5	-1675
29	UART_TXD	L4	-689.5	-1458.45
30	D[7]	K4	-537	-1675
31	D[1]	J4	-412	-1458.45
32	A[15]	L5	-287	-1675
33	D[11]	K5	-162	-1458.45
34	D[3]	J5	-37	-1675
35	MFP[2]	L6	88	-1458.45
36	A[12]	K6	213	-1675
37	D[4]	J6	338	-1458.45
38	A[11]	L7	463	-1675
39	A[5]	K7	588	-1458.45

Die Bump No.	Net Name	Ball No. See Note 1	X (µm) See Note 2	Y (µm) See Note 2
40	GND	J7	713	-1675
41	VDD_C	L8	838	-1458.45
42	VBATT_DIG	L9	990.5	-1675
43	D[5]	K8	1115.5	-1458.45
44	A[6]	K9	1240.5	-1675
45	OE_N	L10	990.5	-1241.9
46	A[3]	K10	1490.5	-1675
47	A[1]	L11	1241.85	-1123
48	VDD_P	K11	1675	-1373
49	VSS_P	J8	1458.4	-1248
50	FCS_N	J10	1675	-1123
51	A[16]	J11	1241.85	-873
52	D[6]	J9	1675	-873
53	D[0]	H10	1241.85	-623
54	A[9]	H11	1675	-623
55	D[8]	H9	1458.4	-498
56	D[9]	G10	1675	-373
57	D[10]	G11	1458.4	-248
58	AUX_TXD	G9	1675	-123
59	MFP[3]	F10	1458.4	2
60	A[14]	F11	1675	127
61	D[2]	F9	1458.4	252
62	A[17]	E11	1675	377
63	D[12]	E10	1458.4	502
64	VSS_P	E9	1675	627
65	VDD_P	D11	1458.4	752
66	A[2]	D10	1675	877
67	GND	D9	1458.4	1002
68	VDD_C	C11	1675	1127
69	A[4]	C10	1241.85	877
70	D[13]	B10	1675	1377
71	A[7]	B11	1458.4	1252
72	A[8]	A11	1207.5	1241.9
73	A[10]	A10	1457.5	1675
74	D[14]	C9	1082.5	1458.45
75	D[15]	A9	1207.5	1675
76	MFP[4]	B9	957.5	1241.9
77	MFP[5]	C8	957.5	1675
78	A[13]	B8	832.5	1458.45
79	WE_N	A8	707.5	1675

Die Bump No.	Net Name	Ball No. See Note 1	X (µm) See Note 2	Y (µm) See Note 2
80	MFP[6]	C7	582.5	1458.45
81	MFP[7]	C6	457.5	1675
82	XTAL_N	B7	332.5	1446.95
83	XTAL_P/CLK	A7	105	1675
84	VCC	B6	-20	1458.45
85	VTUNE	A6	-145	1675
86	GND	A5	-180.5	1241.9
87	GND	B5	-395	1675
88	VCC	C4	-644.5	1241.9
89	TX_BIAS	A4	-645	1675
90	GND	B4	-770	1458.45
91	GND	A3	-895	1675
92	RF_IO	A2	-1145	1675
93	GND	B2	-1399.15	1458.5
94	VCC	A1	-1526	1675

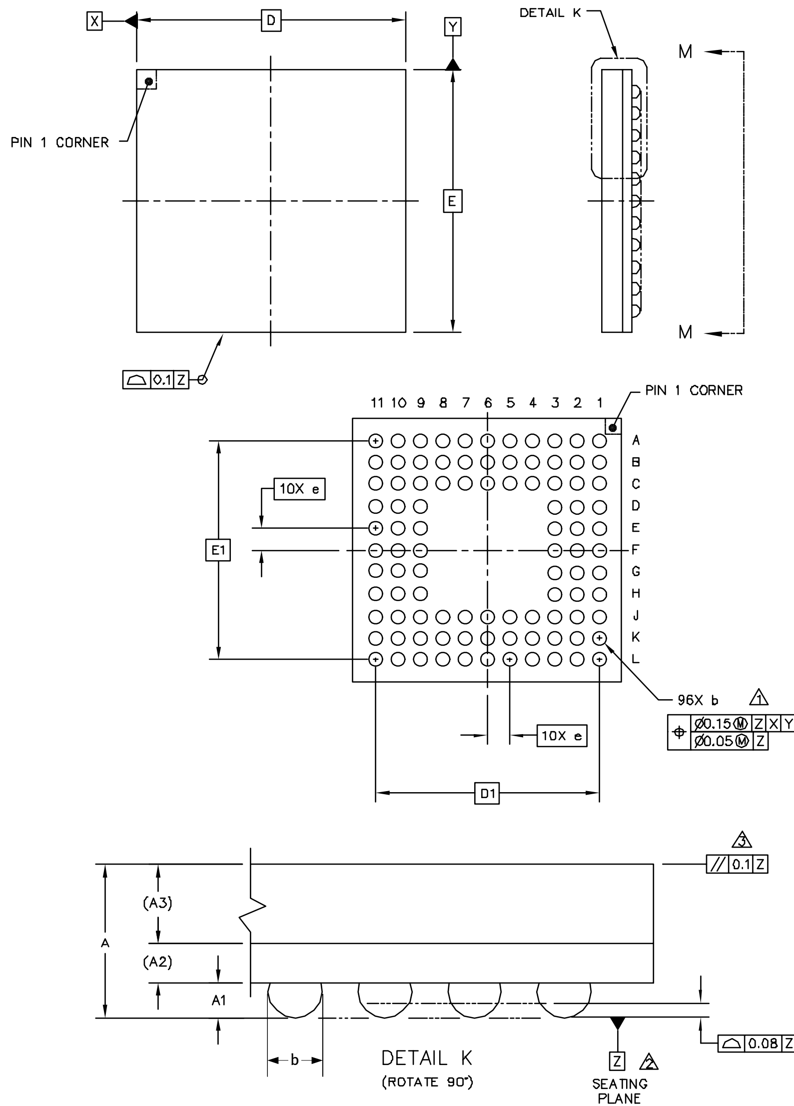
1 Ball number information is provided as a reference to the 6-by-6-mm BGA packaged device.

2 X, Y bump locations are referenced to the center of the die.

Packaging and Product Marking

Package Drawing

Green package, 96-Pin, 6 mm x6 mm, VFBGA Drawing and Dimensions



Symbol	Min	Max
A	0.8	1.0
A1	0.2	0.3
A2	0.22 REF	
A3	0.45 REF	
b	0.25	0.35
D	6 BSC	
E	6 BSC	
e	0.5 BSC	
D1	5 BSC	
E1	5 BSC	

Notes:

1. Dimension b is measured at the maximum solder ball diameter, parallel to datum plane Z.

2. Datum Z is defined by the spherical crowns of the solder balls.

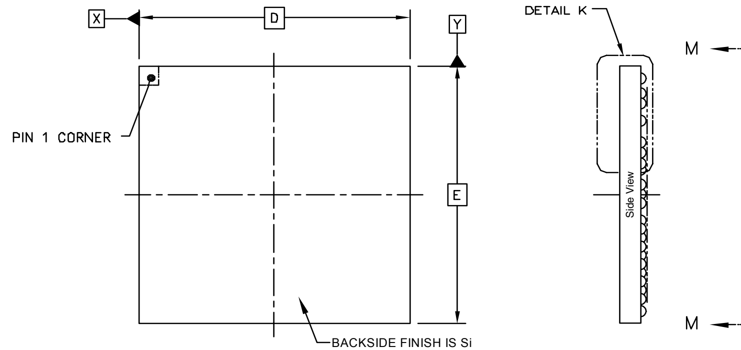
3. Parallelism measurement shall exclude any effect of mark on top surface of package.

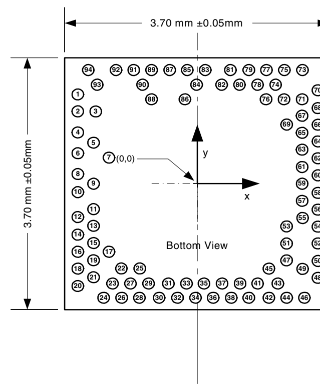
4. All dimensions are in millimeters.

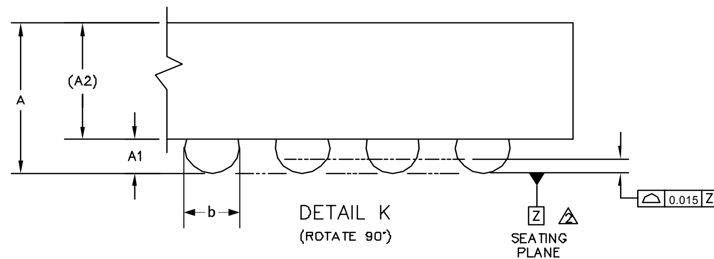
5. VFBGA green package solder ball material: 95.5% Sn, 4% Ag, 0.5% Cu.

Packaging and Product Marking

Green package, Known Good Die, Drawing and Dimensions



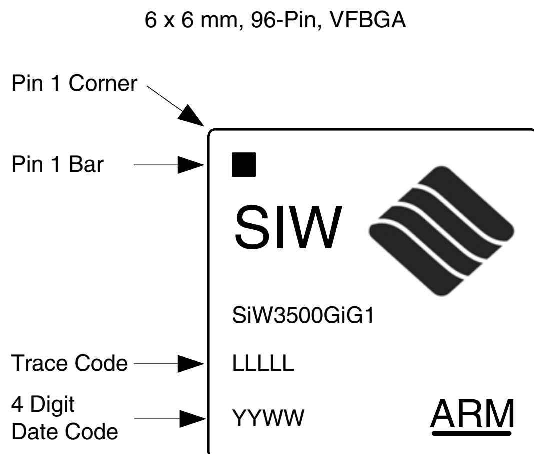




Symbol	Min (µm)	Max (µm)	Notes:
A	375	415	1. Dimension b is measured at the solder bump diameter at the bump base, parallel to datum plane Z.
A1	100 µm ± 15 µm		2. Datum Z is defined by the spherical crowns of the solder bumps.
b	130 nom		3. All dimensions are in micrometers except as noted.
D	3.70 mm ±0.05mm		4. KGD solder bump material: 97.7% Sn, 2.3% ± 0.5% Ag
E	3.70 mm ±0.05mm		5. Pitch: Minimum bump pitch: some bumps exhibit greater than 250 µm pitch.
Bump Pitch	250	–	

Product Marking

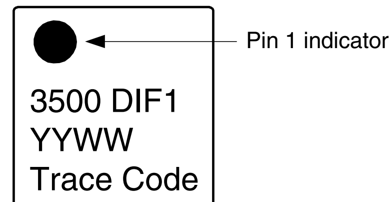
6 x 6 mm, 96-Pin, VFBGA



3.7 x 3.7 mm, Known Good Die

Marking Technique to be used:

- [x] Laser Marking
- [ ] Ink Marking



Notes:

1) Assembly house to fill in YYWW with the Date Code:
   - YY = Year
   - WW = Week
2) Trace code determined at assembly time.
3) The laser marking depth is 1 - 2 μm typical, 3 μm maximum.
4) The laser marking shall be visible at 10X magnification.

Carriers

Tape and Reel

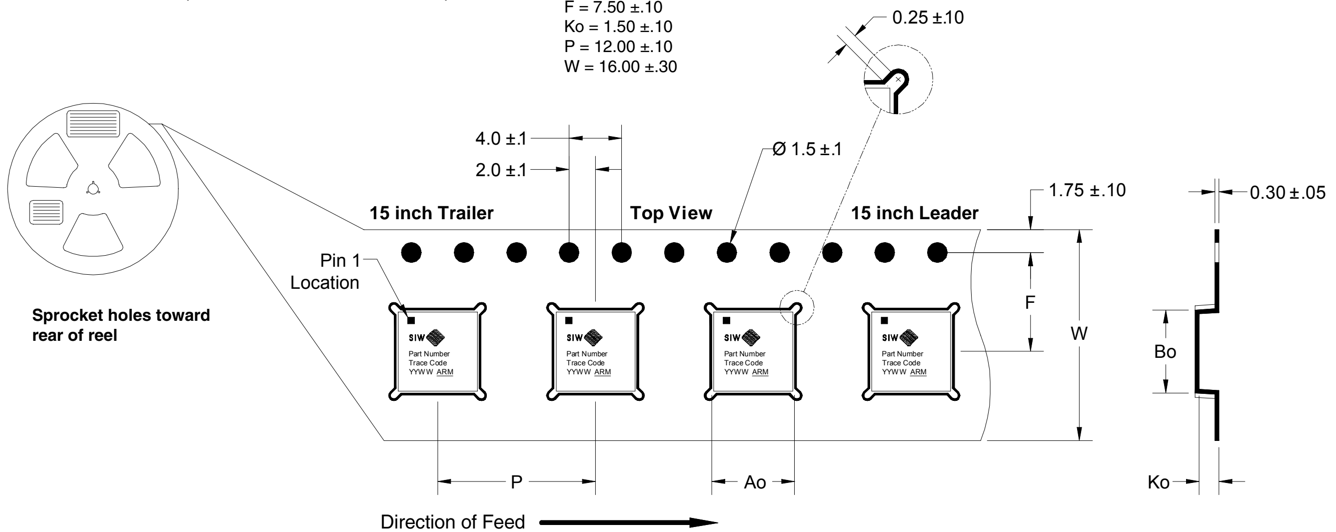
SIW3500GIG, 6 X 6 mm 96-Pin, VFBGA, Tape Details

Carrier tape basic dimensions are based on EIA481. The pocket is designed to hold the part for shipping and loading onto SMT manufacturing equipment, while protecting the body and the solder terminals from damaging stresses. The individual pocket design can vary from vendor to vendor, but width and pitch will be consistent.

Carrier tape is wound or placed onto a shipping reel either 330 mm (13 inches) in diameter or 178 mm (7 inches) in diameter. The center hub design is large enough to ensure the radius formed by the carrier tape around it does not put unnecessary stress on the parts.

Prior to shipping, moisture sensitive parts (MSL-3) are baked and placed into the pockets of the carrier tape. A cover tape is sealed over the top of the entire length of the carrier tape. The reel is sealed in a moisture barrier, ESD bag, which is placed in a cardboard shipping box. It is important to note that unused moisture sensitive parts need to be resealed in the moisture barrier bag. If the reels exceed the exposure limit and need to be rebaked, carrier tape and shipping reels are not bakeable at 125°C. If baking is required, devices may be baked according to section 4, table 4-1, column 8 of Joint Industry Standard IPC/JEDEC J-STD-033A.

RFMD Part Number	Reel Diameter Inch (mm)	Hub Diameter Inch (mm)	Width (mm)	Pocket Pitch (mm)	Feed	Units per Reel
SiW3500GIG1-TR13	13 (330)	4 (102)	16	12	Single	2500



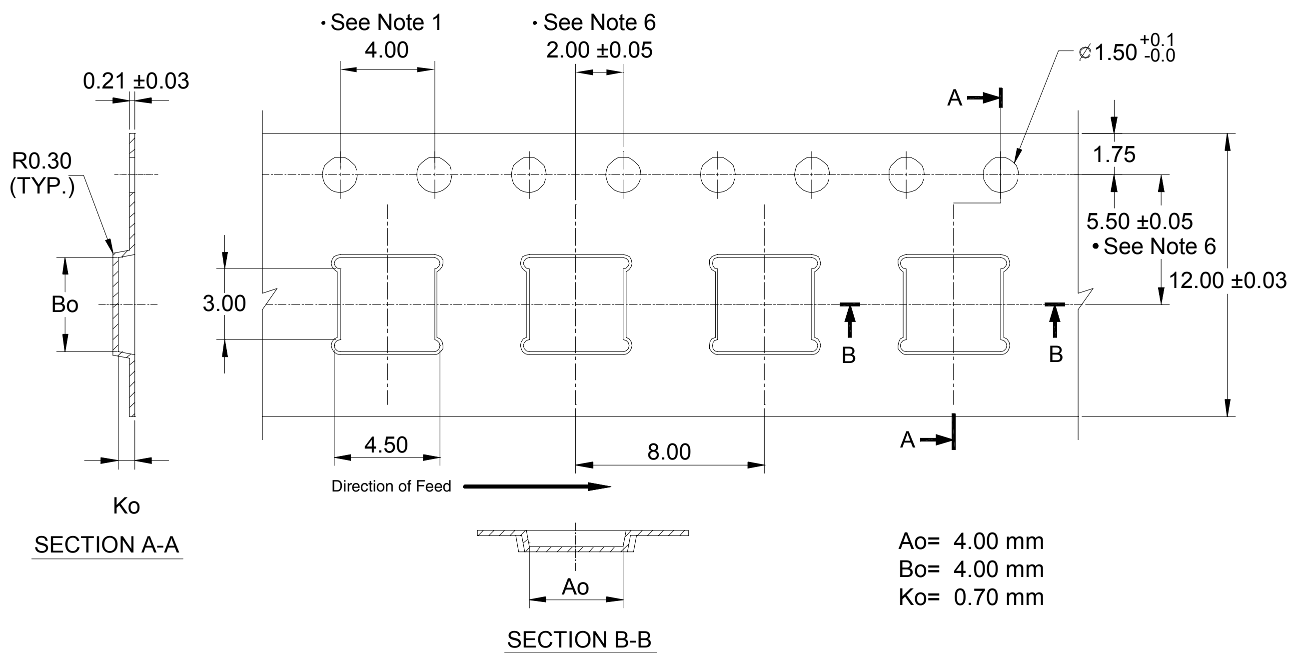
SiW3500DIF, Known Good Die, Tape Details

Carrier tape basic dimensions are based on EIA481. The pocket is designed to hold the part for shipping and loading onto SMT manufacturing equipment, while protecting the body and the solder terminals from damaging stresses. The individual pocket design can vary from vendor to vendor, but width and pitch will be consistent.

Carrier tape is wound or placed onto a shipping reel 330 mm (13 inches) in diameter. The center hub design is large enough to ensure the radius formed by the carrier tape around it does not put unnecessary stress on the parts.

Prior to shipping, parts are placed into the pockets of the carrier tape. A cover tape is sealed over the top of the entire length of the carrier tape. The reel is sealed in a moisture barrier ESD bag with a dry N2 backfill, which is placed in a cardboard shipping box. It is important to note that unused parts need to be resealed in the moisture barrier bag. If baking is required, devices may be baked according to section 4, table 4-1, column 8 of Joint Industry Standard IPC/JEDEC J-STD-033A.

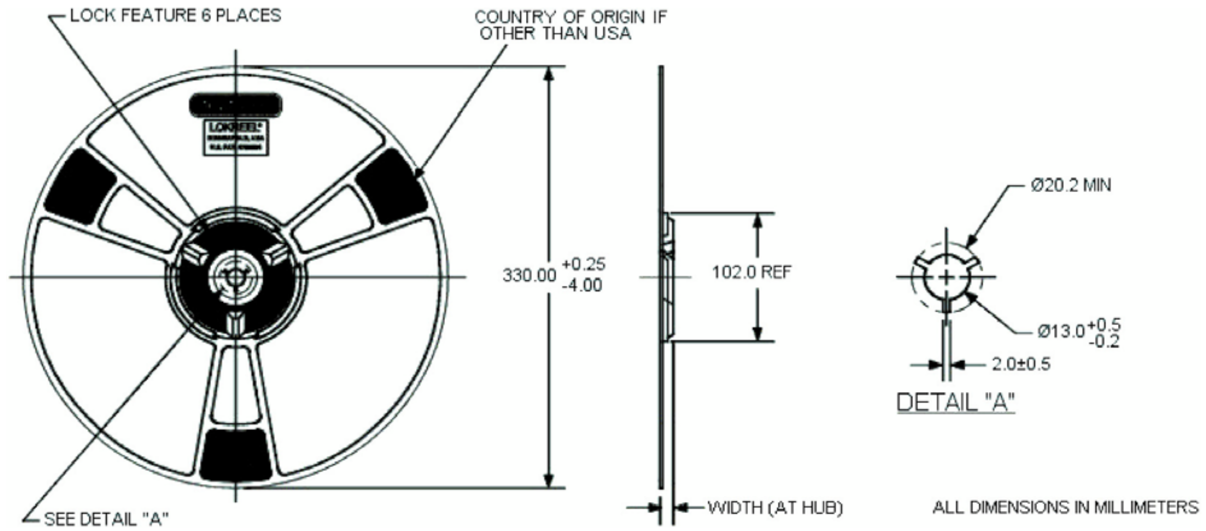
RFMD Part Number	Reel Diameter Inch (mm)	Hub Diameter Inch (mm)	Width (mm)	Pocket Pitch (mm)	Feed	Units per Reel
SiW3500DIF1-TR13	13 (330)	4 (102)	–	–	Single	2500



Notes:

1. 10 sprocket hole pitch cumulative tolerance ±0.2
2. Camber not to exceed 1 mm in 100 mm.
3. Material: black advantek polystyrene.
4. Ao and Bo measured on a plane 0.3 mm above the bottom of the pocket.
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.
7. All dimensions in millimeters.
8. Tolerances (except as noted): decimal ±0.1.

SiW3500DIF, Known Good Die, Reel Details



Peel Test	Peel Angle	Cover Tape	Leader	Trailer	Peel Speed
10–50 grams	165-180º	RS Standard (anti-static)	500 mm (minimum 400 mm)	250 mm (minimum 160 mm)	300 mm/minute

Ordering Information

Part Number	Operational Temperature Range[1]	Package	Solder Ball/Bump Composition	Ordering Quantity
SIW3500GIG1	Industrial	6x6, 96-pin VFBGA, green package	95.5% Sn, 4% Ag, 0.5% Cu	25 pcs on cut tape
SIW3500GIG1SB	Industrial	6x6, 96-pin VFBGA, green package	95.5% Sn, 4% Ag, 0.5% Cu	5 pcs on cut tape
SIW3500GIG1SR	Industrial	6x6, 96-pin VFBGA, green package	95.5% Sn, 4% Ag, 0.5% Cu	100 pcs on short reel
SIW3500GIG1-T13	Industrial	6x6, 96-pin VFBGA, green package	95.5% Sn, 4% Ag, 0.5% Cu	2500 on 13” reel
SiW3500DIF1	Industrial	Known good die[2], green	97.7% Sn, 2.3% ± 0.5% Ag	25 pcs on cut tape
SiW3500DIF1SB	Industrial	Known good die[2], green	97.7% Sn, 2.3% ± 0.5% Ag	5 pcs on cut tape
SiW3500DIF1SR	Industrial	Known good die[2], green	97.7% Sn, 2.3% ± 0.5% Ag	100 pcs on short reel
SiW3500DIF1-T13	Industrial	Known good die[2], green	97.7% Sn, 2.3% ± 0.5% Ag	2,500 on 13” reel

1. Industrial temperature range: -40°C to +85°C.
2. For additional technical details about known good die, please refer to RF Micro Devices document 60 0071 SiW3500DIF Bumped Die Manufacturing Notes.

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