ST20196

ADSL2+ UTOPIA DMT TRANSCEIVER FOR CPE APPLICATIONS

1   Overview

The ST20196 is the digital component of the ST20190 Utopia chipset. The chipset allows equipment manufacturers to develop flexible platforms showing high performance, fully leveraging the ADSL2+ 24 Mbps wireline speed. These platforms can quickly adapt to the rapidly changing requirements of the emerging ADSL2+ Triple-play market covering data, voice and video applications.

2   Features

- ADSL2+ DMT modem with embedded controller allowing easy, straight forward integration with external network processors
- Multi-standard support
  – G.992.1 annexA,B,C (SBM/DBM) & I
  – G.992.2 - g.lite
  – G.992.3 annexA,B,I,J,L (extended reach), M (double upstream)
  – G.992.4 - g.lite.bis
  – G.992.5 annexA,B,C,I,J,M
  – ANSI T1.413 Issue2
  – ETSI TS 101 388 ADSL-over-ISDN
- DS bitrates above 24 Mbps and US bitrates upto 2.5 Mbps in annexM (1.2 in annexA)
- Designed to meet standardized and specific operator requirements.
- CATII functionality with Echo canceling and Trellis coding
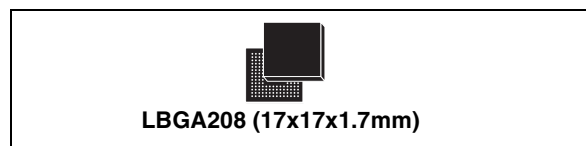- Advanced equalization techniques like Per

Figure 1. Package

LBGA208 (17x17x1.7mm)

Table 1. Order Codes

| Part Number	Package
ST20196	LBGA208 (17x17x1.7mm)

Tone Equalization
- Standard Utopia level1 and 2 ATM interface
- Parallel and serial modem control interface (Ctrl-E) for glue-less connection to a management entity.
- Supply Voltage : 3.3V and 1.2V
- Typical power consumption : 700mW
- Temperature range : I-range (-40°C to 85°C)

3   Applications

- Medium/high end routers
- Business routers with modular and/or multiple WAN access
- Security applications
- Voice and data gateways
- Wireless access points
- Convergence of gateways and IP SetTopBox
- Home servers with storage capabilities, smart card interfaces, unified mailboxes, …

Figure 2. Block Diagram
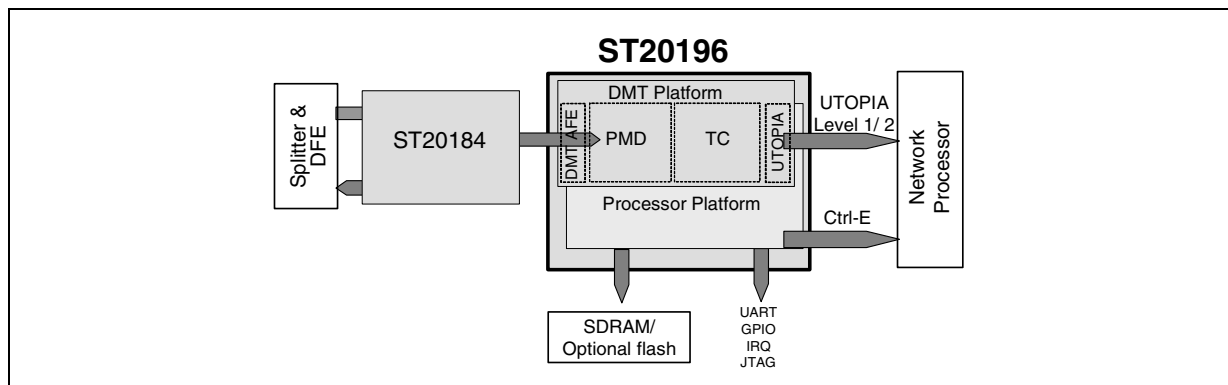
4 General Description

The new ADSL2+ standards will accelerate Broadband applications way beyond always-on data streaming, mainly used for web-browsing and e-mailing. Internet Service Providers are exploring several ways to increase their revenues by offering new services and applications and enlarging their customer base. This can be realized using the large number of new features and different annexes of ADSL2+.

The ST20196 is designed in a main stream digital CMOS technology. The major building blocks are the DMT engine including the PMD and TC layer, the ARM™ microcontroller and the different interfaces like Utopia Level I&II, Ctrl-E, interfacing to the ST20184 and memory. The DMT engine is compliant with the new ADSL2+ standards and supports features like diagnostics mode, enhanced power management (L2), 1 bit constellation, relocatable and modulated pilot, …

On top of the mandatory new features, the DMT engine includes several differentiating, advanced and unique techniques like an innovative Per Tone Equalizer (PTEQ) optimizing short loop and bridge tap performances and reducing the impact of RFI in ADSL2+ mode.

A highly performant echo canceller (EC) and a fully digital clock recovery scheme (TDI) further differentiate the ST20190 ADSL2+ performances.

To be prepared for Triple-play applications a flexible TC-layer has been implemented.

The cached ARM™ micro-controller allows further improvement of the performances and allows fast and easy integration with the major third party network processors. Data is exchanged over the Utopia level1 or 2 interface and the commands via the ST Ctrl-E modem control command protocol.

5 Processor Platform

Figure 3. Processor Platform diagram
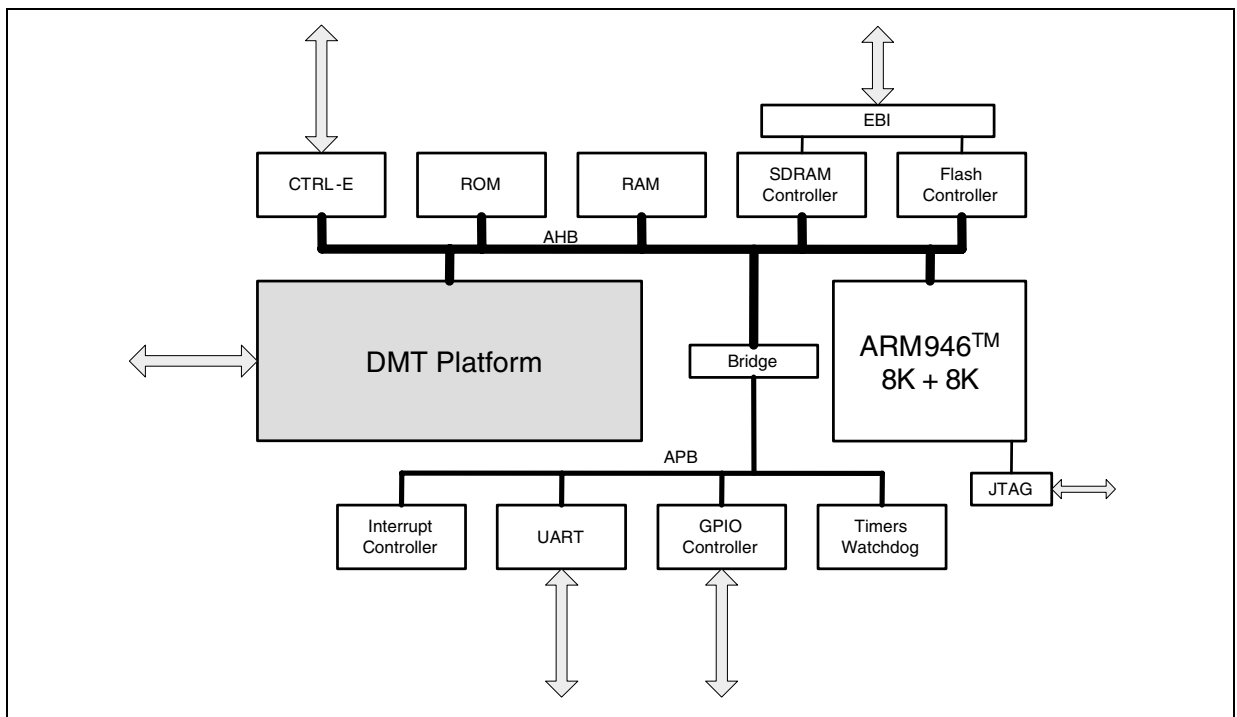
5.1 Micro-controller

The micro-controller is made of an ARM946™ microprocessor with 8Kbytes instruction and 8Kbytes data caches. He is connected to 16Kbytes internal RAM and 512bytes ROM.

5.2 ROM and boot procedure

The ROM contains the boot sequence needed for code download at startup from UART or CTRL-E interface. The use of the ROM by the ARM946™ microprocessor is defined by the state of the TROM pin during reset.

TROM = '1': The processor boots directly from the external Flash.

TROM = '0': The processor boots from internal ROM. The communication settings for the UART are then fixed to 38400 bauds, no parity, 8 data bits, 2 stop bits.

5.3 Memory Interface

The ST20196 implements a shared interface for external memories. The SDRAM and Flash I/O pins are muxed by the EBI module

Table 2.

Pin Name	Size	Type	SDRAM	Flash
E_D[15:0]	16	IO	D[15:0]	D[15:0]
E_A[15:0]	16	IO	A[15:0] (output)	A[15:0] (output)
S_DQM[1:0]	2	O	DQMask[1:0]	A[17:16]
S_nCAS	1	O	nCAS	A18
S_nRAS	1	O	nRAS	A19
SF_nWE	1	O	nWE	nWr
S_CLK	1	IO	CLK	
S_nCS	1	O	nCS	
F_nCS	1	O		nCS
F_nOE	1	O		nRd, nOe

5.3.1 SDRAM

ST20196 supports SDRAM access through a SDRAM Controller, which supports

- 16 bit SDRAM access
- SDRAM sizes up to 512Mbits

The SDRAM Controller has a built in refresh timer. Refresh and access times can be modified through firmware to support different SDRAM requirements.

All SDRAM actions are triggered at the rising edge of its clock. Timing diagrams for a burst of four 16-bit accesses to 16-bit SDRAM show the basic behavior of the control signals.

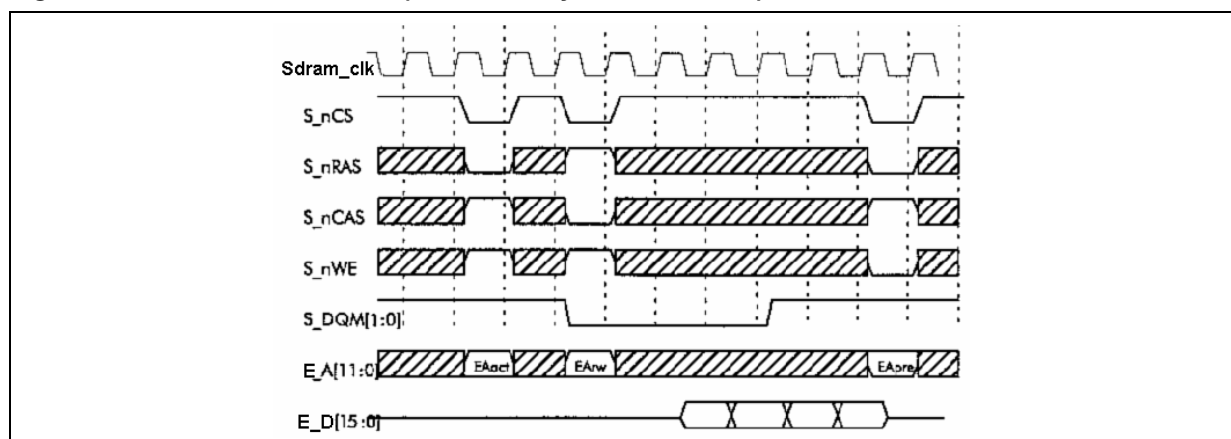**Figure 4. SDRAM Read access (CAS Latency = 3 , Burst = 4)**

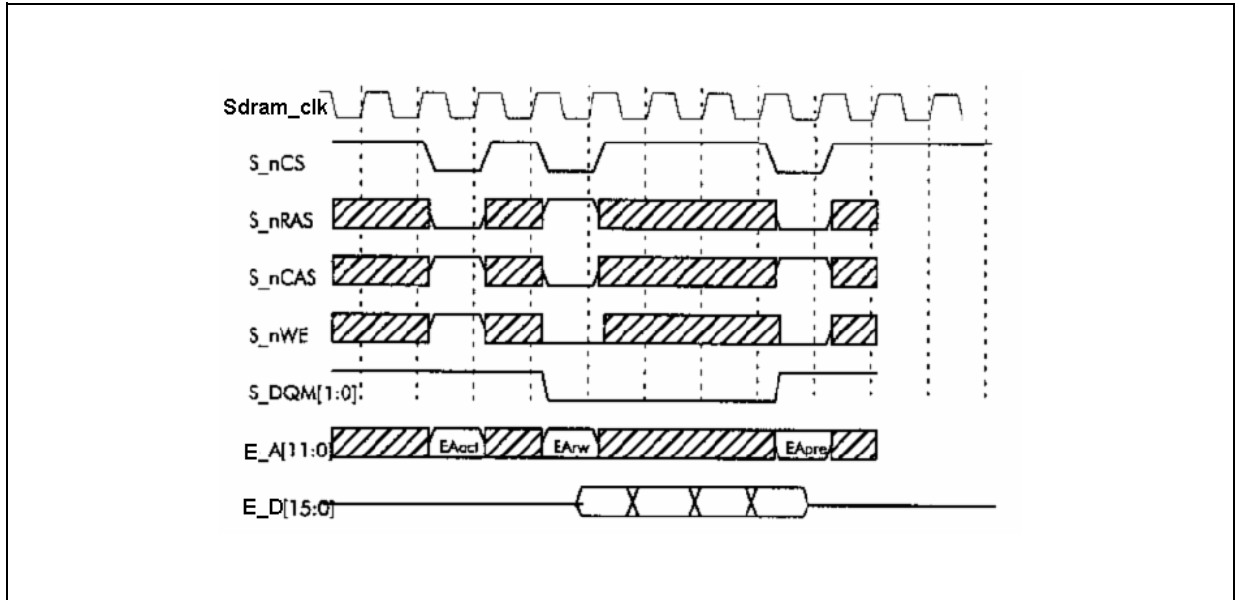**Figure 5. SDRAM Write access (CAS Latency = 3 , Burst = 4)**
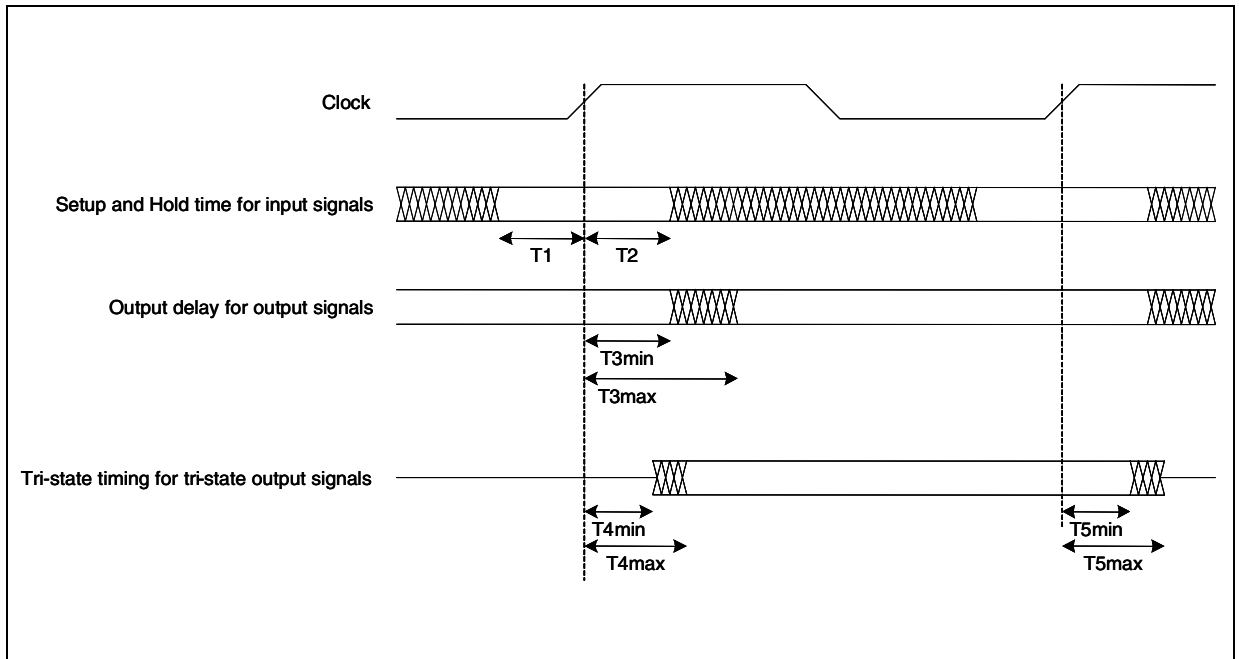

Figure 6. SDRAM Interface Timing

Table 3.

Signal			Description	Min.	Max.
S_CLK	clock		SDRAM clock	35.328 MHz	
			Duty cycle	40%	60%
S_nCS	Output	T3	Output delay from S_CLK	2.8 ns	7.5 ns
S_nRAS	Output	T3	Output delay from S_CLK	2.8 ns	7.5 ns
S_nCAS	Output	T3	Output delay from S_CLK	2.8 ns	7.5 ns
S_DQM[1:0]	Output	T3	Output delay from S_CLK	2.8 ns	7.5 ns
SF_nWE	Output	T3	Output delay from S_CLK	2.8 ns	7.5 ns
E_A[15:0]	Output	T3	Output delay from S_CLK	2.8 ns	7.5 ns
E_D[15:0]	Input	T1	Input setup to S_CLK	1 ns	-
		T2	Input hold from S_CLK	1 ns	-
E_D[15:0]	Output	T3	Output delay from S_CLK	2 ns	9.5 ns
		T4	Signal going low impedance from S_CLK	2 ns	9.5 ns
		T5	Signal going high impedance from S_CLK	2 ns	9.5 ns

Note:
- The timing values are given for best to worst case operating conditions.
- Setup and hold times for input signals are based 1.5 ns input transition time.
- The output delays are based on 25pF loading capacitance.

5.3.2 Flash

ST20196 Flash interface supports

– 8-bit Flash access
– Flash sizes up to 8Mbit (1M x 8bit)
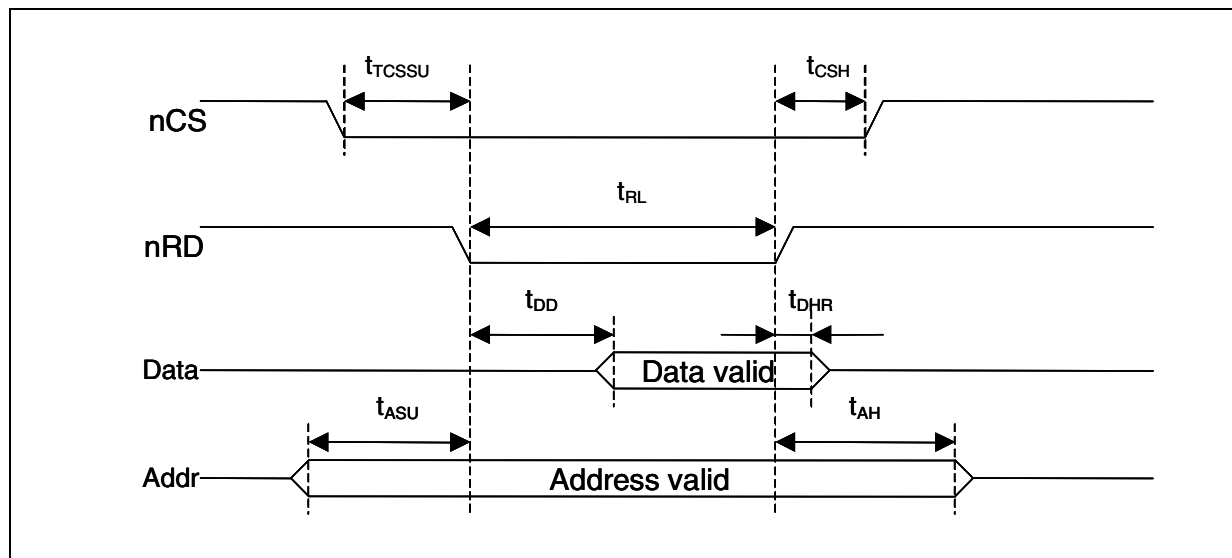
Figure 7. Flash Read Timing
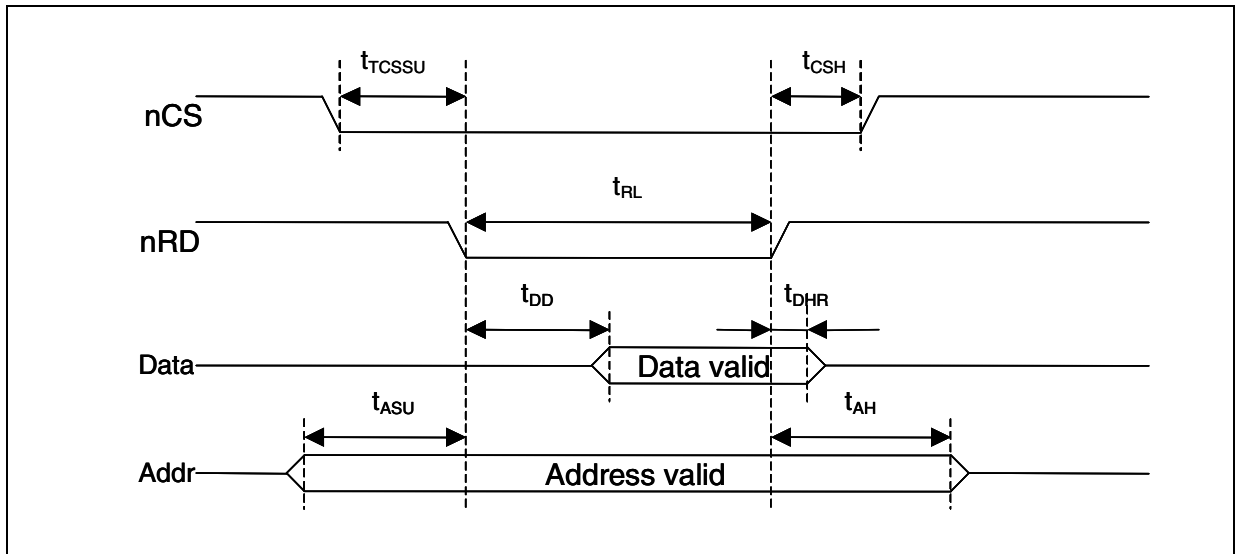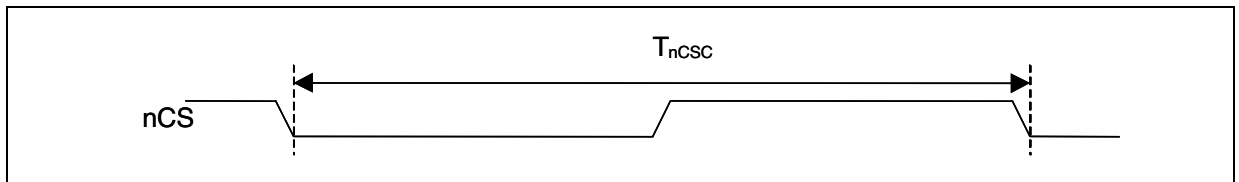
Figure 8. Flash Write Timing

Figure 9. Flash Chip Select Timing

Flash Timing parameters, programmable to some extent by steps of clock cycles (typically 35.328MHz).

Table 4. Flash Timing parameters

Name	Min (ns)	Max (ns)	Number of clock cycles			
				Default	Min	Max
T_{CSSU}	0	-	ISA_TCSSU	4	0	15
T_{CSH}	0	-	ISA_HARW	2	0	15
t_{RL}	0	-	ISA_TRL	15	0	15
t_{DD}	-	150	-	-	-	-
t_{DHR}	-	40	-	-	-	-
t_{DSU}	0	-	ISA_TDSU	12	0	15
t_{DHW}	0	-	ISA_HARW	2	0	15
t_{ASU}	0	-	ISA_TASU	4	0	15
t_{AH}	0	-	ISA_HARW	2	0	15
T_{nCSC}	50	-	5	-	-	-

5.4 CTRL-E

The Ctrl-E interface controller is a generic mailbox system to exchange control and status messages between ST-20196 (over AHB bus) and an external controller (over Ctrl-E interface). It consists of a mailbox and a physical interface. Although the two 8-bit command registers are intended for use in one direction (ARM™ to Ctrl-E or Ctrl-E to ARM™) they are fully accessible in read and write from both sides. So it is up to the software to guarantee consistency of register values. Two control registers only accessible by

the ARM™ core allow configuration of the status update mechanism and of interrupt generation.

The Ctrl-E physical interface between the mailbox and an external controller is implemented as a generic parallel bus interface. The Ctrl-E Mailbox and its interfaces are all running synchronous to the AHB clock.

Figure 10. CTRL-E Interface Controller principle
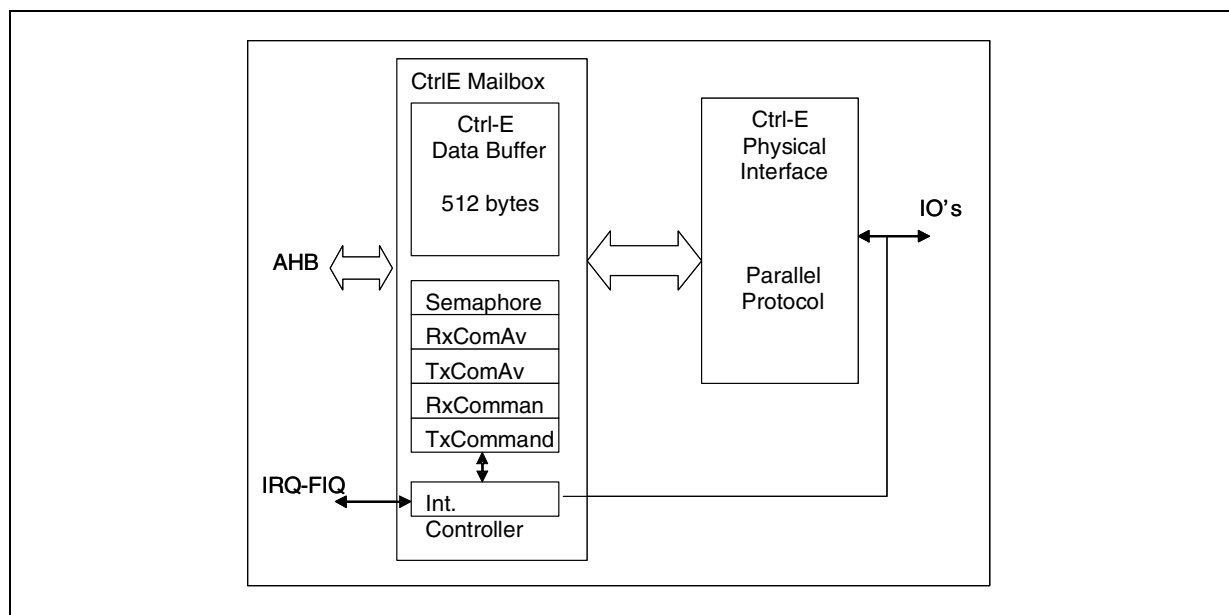
5.4.1 CTRL-E Mail Box

The Ctrl-E Mailbox occupies a 512 byte memory map accessible by the Ctrl-E physical interface and by the AHB bus. The mailbox memory map is given in the Table below. Two addresses are shown in the memory map: CtrlE A[8:0] as generated by the Ctrl-E physical interface and the LSBs of the AHB address bus AhbAddress[8:0]. The two configuration registers Ctrl-E Control and Ctrl-E Interrupt are only accessible by the AHB bus.

The Mailbox interrupt controller generates two interrupts: an internal interrupt towards the ARM™ interrupt controller (Ctrl-E IntArm), and an external interrupt towards the external controller (Ctrl-E IntExt). Depending on the configuration an interrupt-based or polling-based communication protocol can be implemented.

Table 5. CTRL-E Mail Box Memory Map

Field	ARM™ Address	Ctrl-E Address	Size	Function
TxCommand	000h	000h	8	Transmit commands
RxCommand	001h	001h	8	Receive commands
TxComAv	002h	002h	1	1 = Tx Command is available
RxComAv	003h	003h	1	1 = Rx Command is available
Semaphore	004h	004h	2	Semaphore
Data buffer	005h ◊ 1FFh	005h ◊ 1FFh	8	507 x 8bit data buffer
StatusCtrl	200h	NA	8	Status control register
InterruptCtrl	201h	NA	8	Interrupt control

5.4.2 CTRL-E Semaphore

A simple semaphore mechanism is provided to allow control of the data consistency of the Ctrl-E Data Buffer and Command registers. If there would be unlimited accesses to all mailbox addresses over the two interfaces by the two independent controllers there would be no possibility to implement a semaphore mechanism in software. Therefore one mailbox address is defined as a two-bit semaphore register protected by control logic to prevent illegal write accesses to this register.

Before a read/write access by one of the two interfaces (AHB or Ctrl-E) this interface should perform a 'P-operation' on the semaphore. After a read or write of the data buffer, the interface should do a 'V-operation' releasing the semaphore. P and V operations are performed by write and read accesses to the semaphore register. The semaphore will be updated as shown in Table 10.

Each semaphore operation (P or V) consists of two consecutive actions:

   a.   Write the correct value to the semaphore address (see Table below)

   b.   Read the value in the semaphore address.

If the value read is different from the value written the P or V operation was not successful and should be tried again.

Table 6. Semaphore P and V operations

Semaphore	Originator	Value written	Free	Taken by ARM™	Taken by Ctrl-E
			00	01	11
P	ARM™	01	01	01	11
	Ctrl-E	11	11	01	11
V	ARM™	00	00	00	11
	Ctrl-E	00	00	01	00

The data buffers can be accessed without using the semaphore mechanism if data consistency is guaranteed in another way. If other values are written to the semaphore address than the values listed, the write will not be performed.

5.4.3 CTRL-E PHYSICAL INTERFACE

Physical interface implements a generic parallel interface with 9 bit Address and 8 bit Data bus. Two parallel bus modes are defined to support both Motorola-compatible and Intel-compatible timing and control signals.

This interface specification is compliant to ATM Forum Physical Layer Control Parallel interface.

The parallel bus mode section is done with the C_Mode input pin:

Table 7.

C_Mode	Description
0	Motorola-type parallel interface
1	Intel-type parallel interface (SRAM like)

The two parallel bus modes differ only in the definition of 3 control signals:

   – Bus mode 0 provides a read/write selector, a data strobe and a ready acknowledge.
   – Bus mode 1 provides a read strobe, a write strobe and a ready acknowledge.

The signal definition is shown in following table:

Table 8.

Intel-like	Motorola-like	Type	Description
C_A[8:0]	C_A[8:0]	I	Address
C_D[7:0]	C_D[7:0]	IO	Data bus
C_notCS	C_notCS	I	Chip select
C_notInt	C_notInt	OZ	Interrupt output (inverted)
C_notWr	C_Rd/notWr	I	Write command or Write enable
C_notRd	C_notDS	I	Read command or Data strobe
C_notRdy	C_notDtAck	OZ	Ready signal or Ack
C_Mode	C_Mode	I	Mode select (= 0 or 1)

All input signals are registered internally using the AHB clock. But there is no need to synchronize the interface to the main clock. Due to this fact, the interface will behave faster in case of AHB higher clock frequency. All timings are preliminary.

5.4.4 CTRL-E Write Access
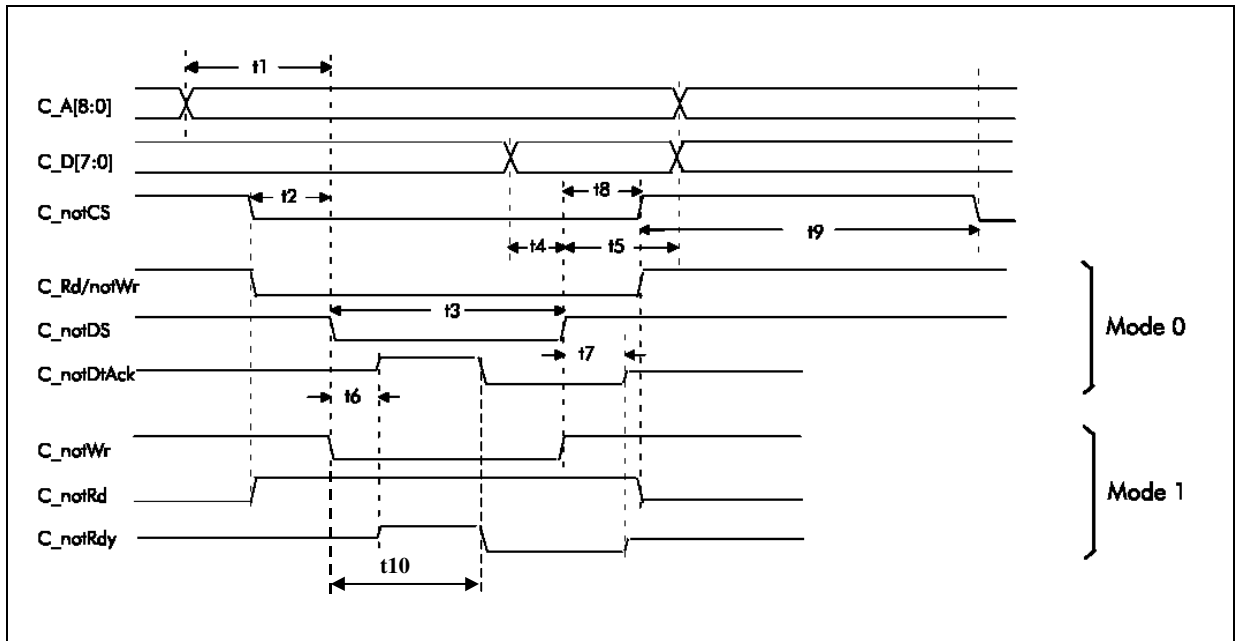
Figure 11. CTRL-E Write Access Timing diagram

Table 9. CTRL-E Write Access Timing

Symbol	Description	AHB clock cycles		AHB at 35.328MHz (ns)	
		Min	Max	Min	Max
t1[1]	C_A Setup to C_notDS (C_notWr) low	0	-	0	-
t2[1]	C_notCS, C_Rd/notWr setup to C_notDS (C_notWr) low	0	-	0	-
t3[1]	C_notDS (C_notWr) pulse width	5[*]	-	153[3]	-
t4[1]	C_D setup to C_notDS (C_notWr) high	0	-	0	-
t5[1]	C_A, C_D hold from C_notDS (C_notWr) high	0	-	0	-
t6[2]	C_notDtAck (C_notRdy) valid from C_notDS (C_notWr) low	-	0	-	10[3]
t7[2]	C_notDtAck (C_notRdy) tri-state from C_notDS (C_notWr) high	-	0		10[3]
t8[1]	C_notCS, C_Rd/notWr hold from C_notDS (C_notWr) high	0	-	0	-
t9 [1]	C_notCS high to C_notCS Low	3	-	96[3]	-
t10 [2]	C_notDs low to C_notDtAck low	5	6	143	182[3]

(*): This is a minimal value. In case c_notDtAck(C_notRdy) is used to synchronize the process, one should wait until c_notDtAck(C_notRdy) becomes low (t10)
(1): Timings fully defined by the CTRL-E Master: these timings are considered as necessary to make the interface work
(2): Timings fully dependable of the CTRL-E slave
(3): 10ns is added to the theoretical value in order to include the input and output delays

5.4.5 Ctrl-E Read access
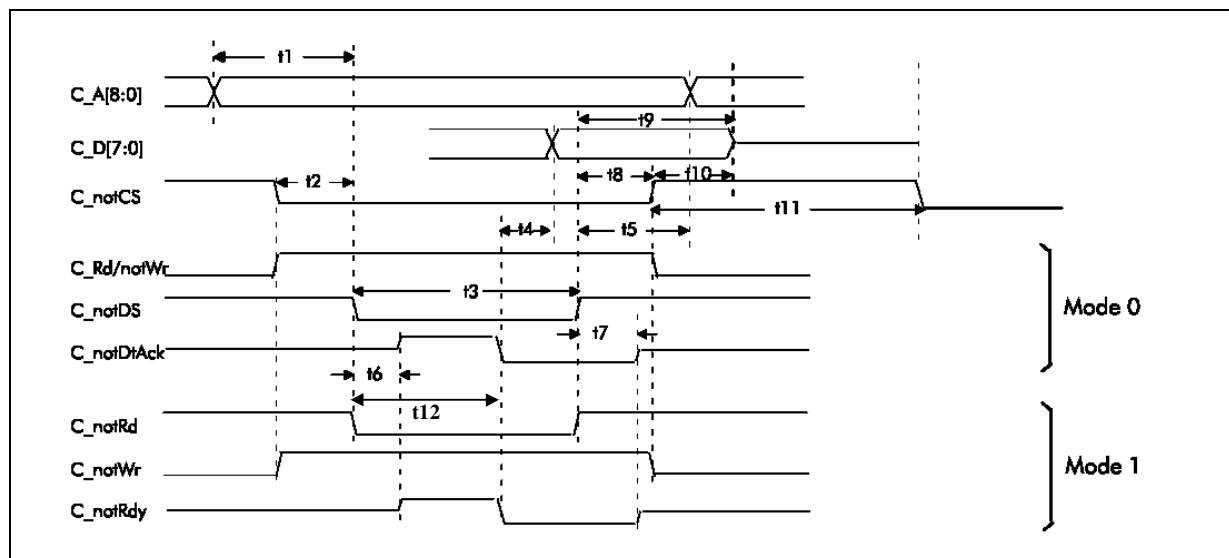
Figure 12. Ctrl-E Read Access Timing diagram

Table 10. CTRL-E Read Access Timing

Symbol	Description	AHB clock cycles		AHB at 35.328MHz (ns)	
		Min	Max	Min	Max
t1[1]	C_A Setup to C_notDS (C_notRd) low	0	-	0	-
t2[1]	C_notCS, C_Rd/notWr setup to C_notDS (C_notRd) low	0	-	0	-
t3[1]	C_notDS (C_notRd) pulse width	7	-	210[3]	-
t4[2]	C_D valid from C_notDtAck (C_notRdy) low	-	0	-	5
t5[1]	C_A hold from C_notDS (C_notRd) high	0		0	
t6[2]	C_notDtAck (C_notRdy) volid from C_notDS (C_notRd) high	-	0	-	10[3]
t7[2]	C_notDtAck (C_notRdy) tri-state from C_notDS(C_notRd) high	-	0	-	10[3]
t8[1]	C_notCS, C_Rd/notWr hold from C_notDS (C_notRd) high	0	-	0	-
t9[2]	Data tri-state from C_notDS (C_notRd) high	3	4	86	124[3]
t10[2]	Data tri-state from C_notCS high	0	4	0	124[3]
t11[1]	C_notCS high to C_notCS low (min. time between 2 Accesses)	3	-	86	-
t12[2]	C_notDS low to C_notRdy low	6	7	172	210[3]

(1): Timings fully defined by the CTRL-E Master: these timings are considered as necessary to make the interface work
(2): Timings fully dependable of the CTRL-E slave
(3): 10ns was added to the theoretical value in order to include the input and output delays.

5.5 Peripherals

ST20196 processor platform includes different peripherals located on a second level bus, connected to the main AHB bus through a bridge.

5.5.1 Watchdog

The watchdog is actually a 32-bit real-time counter configured as watchdog. It generates both an interrupt signal sent to the interrupt controllers and a reset signal sent to the reset controller.

5.5.2 Real time counters

There are 2 general-purpose 32-bit real time counters. It consists of single 32-bit down-counters that generate interrupts if the counters reach zero.

5.5.3 Interrupt controllers

There are 2 interrupt controllers. One is connected with the ARM™ IRQ and one with the ARM™ FIQ. All ST-20196 interrupts are connected at the same time to both controllers to allow SW to decide which ones to handle as fast and which to handle as slow interrupts.

5.5.4 UART

There is one UART for RS232 interfacing to external systems. The UART is capable of full-duplex data transfer at user defined baud rates. Most common baud rates are supported. FIFOs with configurable depth store the received and the data to be transmitted. The UART offers parity checking, stop bit length control and hardware handshake.
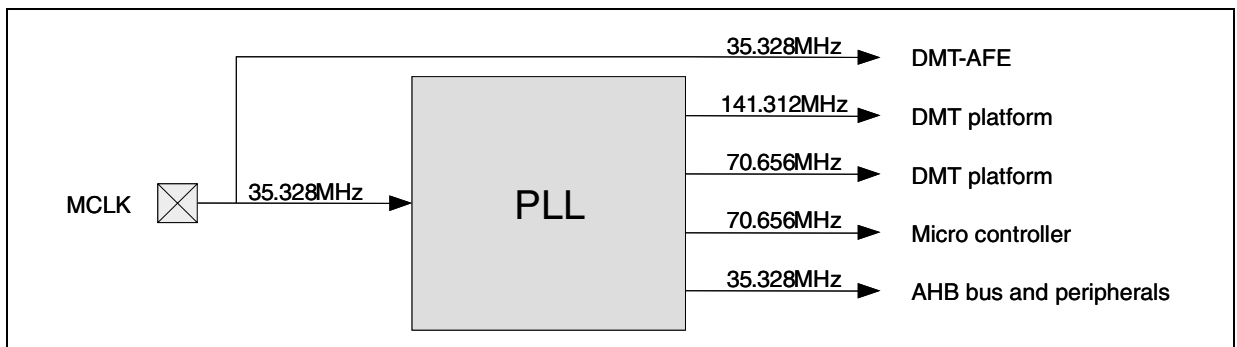
When booting from the internal ROM, the communication settings are: 38400 bauds, no parity, 8 data bits, 2 stop bits.

5.5.5 GPIO controller

There is 1 GPIO controller driving 8 external GPIO's.

6 Clocking scheme

Figure 13. Clocking scheme

Internal clocks are derived from the MCLK input clock via a PLL.

7 DMT platform

The following section essentially describes the sequence of actions performed by the DMT platform.

7.1 DMT-AFE (ST20184)

The DMT-AFE module is taking care of the interface with the analog front end device. The module is supporting only the ST20184 device.

In the receive direction, the DMT-AFE module gets the signal multiplexed on 10 inputs and transmit it with

a first decimation to the DMT-PMD module.

In the transmit direction, the DMT-AFE module transfers the signal multiplexed on 4 output signals.

The module includes test loop-backs.
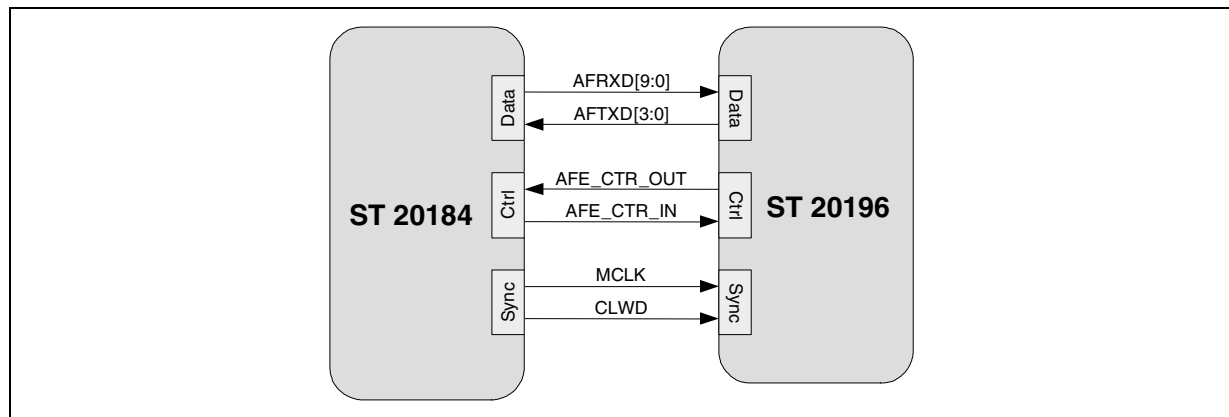
7.1.1 DMT-AFE Interface signals

Figure 14.

Table 11.

Signal	Description
MCLK	35.328MHz clock.
CLWD	Synchronization signal generated on MCLK rising edge (in ST-20184) and sampled on MCLK falling edge (in ST-20196).
AFRXD[9:0]	AFE receive data bus: 5 PDM's at 70MHz multiplexed on 10 pins at 35MHz. Signals are generated on MCLK rising edge (in ST-20184) and sampled on MCLK falling edge (in ST-20196).
AFTXD[3:0]	AFE transmit data bus: 16bit samples at 8.8MHz, split on 4*4 signals at 35MHz, synchronized with CLWD. Signal are generated on MCLK rising edge (in ST-20196) and sampled on MCLK rising edge (in ST-20184).
AFE_CTR_IN	AFE Control response serial bit. Sampled on MCLK rising edge when CLWD goes high.
AFE_CTR_OUT	AFE Control transmit serial bit. Generated on MCLK rising edge when CLWD goes low.

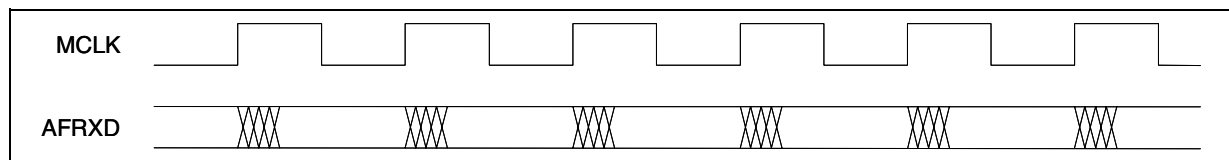### 7.1.2 DMT-AFE Interface timing

Figure 15. AFE Receive data bus

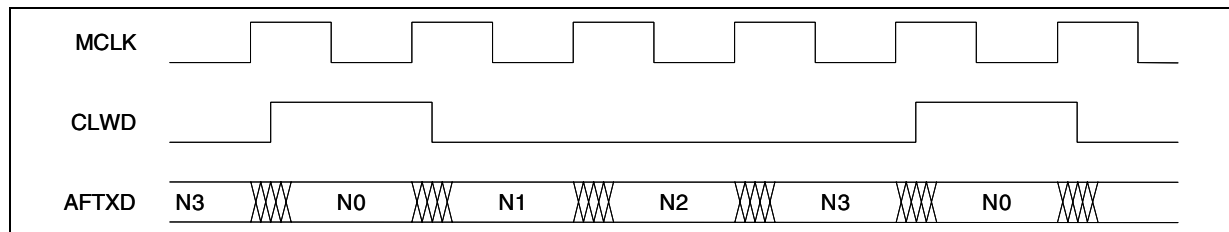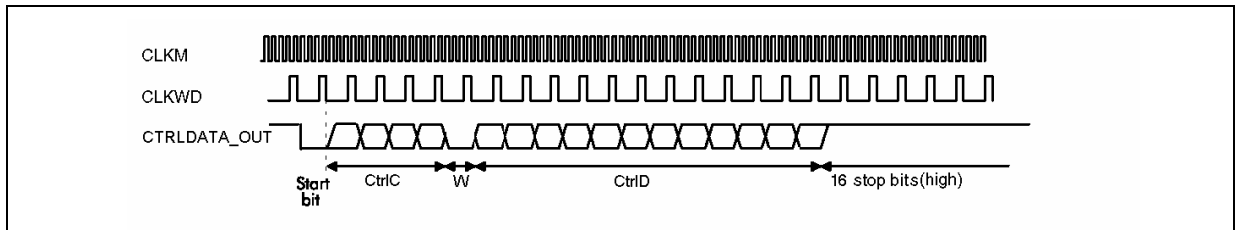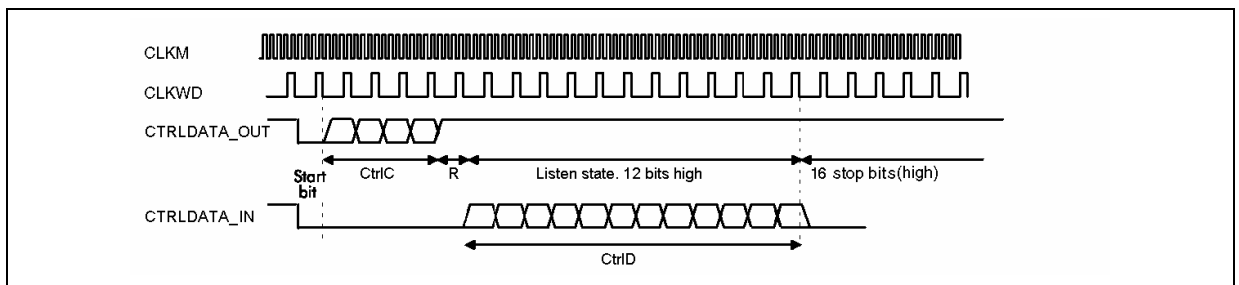
Figure 16. AFE Transmit data bus

Figure 17. AFE Control Write protocol

The write protocol is composed of 5 parts, at the rate defined by CLWD:

– 1 leading start bit

– 4 bits representing an address, MSB first

– 1 logic zero bit to indicate it is a write access

– 12 bits of data, MSB first

– 16 stop bits

Figure 18. AFE Control Read protocol

The read protocol is composed of 5 parts, at the rate defined by CLWD:

– 1 leading start bit on AFE_CTR_OUT

– 4 bits representing an address, MSB first, on AFE_CTR_OUT

– 1 logic one bit to indicate it is a read access, on AFE_CTR_OUT

– 12 bits, listen state on AFE_CTR_OUT, data MSB first on AFE_CTR_IN

– 16 stop bits on AFE_CTR_OUT

Table 12.

Signal		Description	Min	Max
AFRXD[9:0]	input	Setup time to MCLK falling edge	0.5 ns	-
		Hold time from MCLK falling edge	0.2 ns	-
AFTXD[3:0]	output	Output delay from MCLK rising edge	0.5 ns	4 ns
CLWD	input	Setup time to MCLK falling edge	0.5 ns	-
		Hold time from MCLK falling edge	0.2 ns	-
AFE_CTR_OUT	output	Output delay from MCLK rising edge	0.5 ns	4 ns
AFE_CTR_IN	input	Setup time to MCLK rising edge	0.5 ns	-
		Hold time from MCLK rising edge	0.2 ns	-

Note:

- The timing values are given for best to worst case operating conditions.
- Setup and hold times for input signals are based 1.5 ns input transition time.
- The output delays are based on 25pF loading capacitance.

7.2 DMT-PMD

Figure 19.
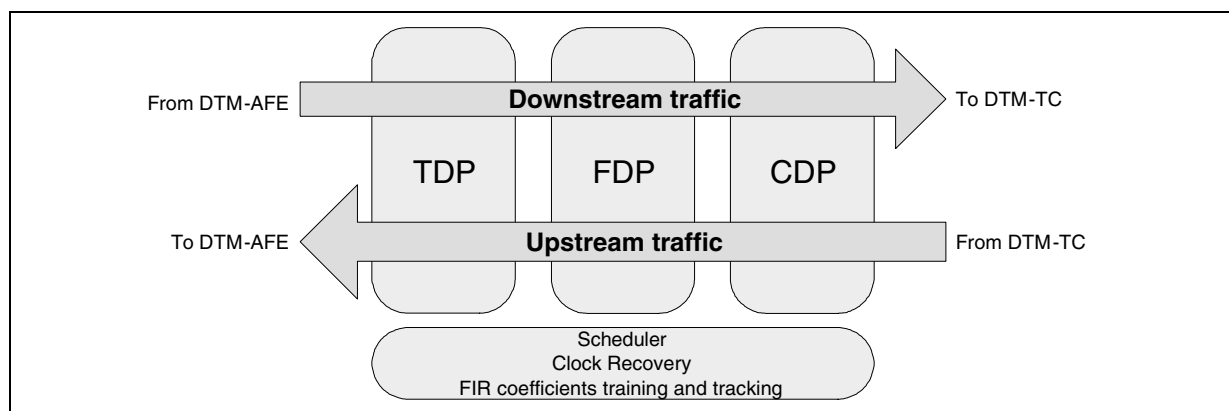
7.2.1 Time Domain Processing (TDP)

The TDP contains in the receive direction: time domain interpolator (TDI), IIR filters, decimators and echo suppression. The TDI receives 8.8 MHz (17.6 MHz for ADSL+) samples and performs a Lagrange interpolation. The Decimators receives then the interpolated samples and reduces this rate to 2.2 MHz (4.4 MHz in ADSL+).

In the transmit direction, the TDP includes: side-lobe filtering, clipping, delay equalization, interpolation and time domain interpolation. The side-lobe filtering and delay equalization are implemented by IIR filters, reducing the effect of echo in FDM systems. Clipping is a statistical process limiting the amplitude of the output signal, optimizing the dynamic range of the AFE. The interpolator receives data at 2.2 MHz and generates samples at a rate of 8.8 MHz. The transmitted samples are interpolated.

The echo is computed via a 256 taps FIR.

7.2.2 Frequency Domain Processing (FDP)

In Rx path, the module is based on programmable DSP and FFT module working as a coprocessor.

The instruction set enables functions like FFT, per tone equalizer (PTEQ), Scaling, and frequency equalization (FEQ). This block implements the core of the DMT algorithm as specified in ANSI T1.413.

The 512-points FFT (1024 points in ADSL+) transforms the time-domain DMT symbol into a frequency domain representation which can be further decoded by the subsequent demapping stages. After FFT and PTEQ blocks - an essentially ICI (Inter Carrier Interference) - free carrier information stream has been obtained.

This stream is still affected by carrier specific channel distortion resulting in an attenuation of the signal amplitude and a rotation of the signal phase. To compensate for these effects, the FFT+PTEQ is followed by a frequency domain equalizer (FEQ). In case of Annex C mode, 2 different FEQ coefficient tables are used for FEXT and NEXT.

In the TX path, the IFFT transforms the DMT symbol generated in the frequency domain by the Mapper into a time domain representation. The IFFT block is preceded by a fine tune gain. In case of Annex C mode, 2 different FTG coefficient tables are used for FEXT and NEXT.

7.2.3 Constellation Domain Processing (CDP): (De)Mapper, Monitor, Trellis (De)Coding

The Demapper converts the constellation points computed by the FDP to a list of bits. This essentially consists in identifying a point in a 2D QAM constellation plane. The Demapper supports trellis coded demodulation and provides a Viterbi maximum likelihood estimator. When the trellis is active, the Demapper receives an indication for the most likely constellation subset to be used.

In the transmit direction, the Mapper performs the inverse operation, mapping a block of bits into one constellation point (in a complex x+jy representation) which is passed to the IFFT block. The Trellis Encoder

generates redundant bits to improve the robustness of the transmission, using a 4-Dimensional Trellis Coded Modulation scheme.

The Monitor computes error parameters for carriers specified in the Demapper process. Those parameters can be used for updates of adaptive filters coefficients, clock phase adjustments, error detection, etc. A series of values is constantly monitored, such as signal power, pilot phase deviations, symbol erasures generation, loss of frame, etc.

A special Reverb-Segue detector allows an easy detection of L2-exit sequence in ADSL2(+) applications.

In case of Annex C mode, 2 different (De)Mapper tables are used for FEXT and NEXT, as 2 different Monitoring memories for FEXT and NEXT.

7.2.4 FIR coefficients training and tracking

FEQ coefficients are trained and kept up-to-date by a specific block reading the carrier errors coming out of the monitoring process.

The Echo-Canceller and PTEQ FIR coefficients are updates are in frequency domain via a dedicated DSP based on a floating point data-path.

7.2.5 Clock recovery

A Digital PLL module receives a metric for the phase error of the pilot tone. In general, the clock frequencies at CO and CPE do not match exactly. The phase error is filtered and integrated by a low pass filter, yielding an estimation of the frequency offset. The phase error can be compensated in the time domain by interpolating samples

7.2.6 DMT Symbol Timing Unit (DSTU)

The DSTU interfaces with various modules. It consists of a real time and a scheduler module. The real time unit generates a time base for the DMT symbols (sample counter), super-frames (symbol counter) and hyper-frames (sync counter). The time bases can be modified by various control features. They are continuously fine tuned by the DPLL module. The DSTU schedulers execute a program, controlled by program op-codes and a set of variables, the most important of which are real time counters. The transmit and receive sequencers are completely independent and run different programs. An independent set of variables is assigned to each of them. The sequencer programs can be updated in real time.

In case of Annex C mode, the DSTU take care also of the hyper-frame synchronization, the table switch for FEXT and NEXT period and the control of the dummy bits insertion/extraction.

7.3 DMT-TC

Figure 20.
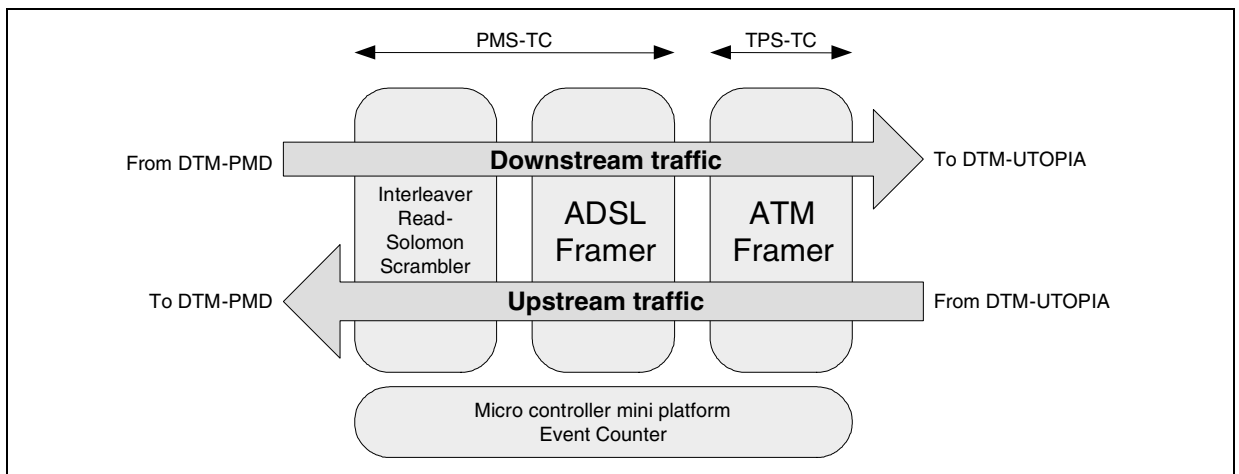
7.3.1 Interleaver, Reed-Solomon, Scrambler, ADSL framer

Based on an ARM7TDMI™ processor associated with a dedicated programmable data-path.

These functions relate to byte oriented data streams. They are completely described in ANSI T1.413. Additions described in the Issue 2 of this specification are also supported.

The data received from the DMT-PMD is split into two paths: interleaved and non-interleaved data flow G.DMT mode, latency 0 and latency 1 data flow in G.DMT.Bis mode.

In case of Annex C mode, a rate adaptation is also performed in order to average the different bit rates during FEXT/NEXT at PMD layer into a fixed rate at TC layer.

In the receive direction, the de-interleaving is used to increase the error correcting capability of block codes for error bursts. After de-interleaving (if applicable), the data flow enters a Reed-Solomon error correcting code decoder, able to correct a number of bytes containing bit errors. The decoder also uses the information of previous receiving stages that may have detected the errored bytes and have labeled them with an "erasure" indication. After leaving the Reed-Solomon decoder, the corrected byte stream is descrambled and the CRC verified.

After, the data flows are processed by programmable machine. The different framing types (G.DMT and G.DMT.Bis) are managed by specific micro-codes loaded into the byte oriented machine. The different type of data is routed toward the Atm Framer or the Adsl-Message-Manager.

The Adsl-Message-Manager take care of EOC bytes (Embedded Operations Channel), AOC bytes (ADSL Overhead Control), HDLC bytes and the indicators bits.

In the transmit direction, similar tasks are performed.

7.3.2 ATM Framer

In the receive direction, two byte streams (fast/slow or bearer channel 0/1) are received from the PMS-TC unit. When ATM cells are transported, this block provides basic cell functions such as cell synchronization, cell payload descrambling, idle/unassigned cell filter, cell header error correction (HEC) and detection. The cell processing happens according to ITU-T I.163 standard. Provision is also made for BER measurements at this ATM cell level. The module provide some flexibility in order to be able to transport non ATM cell oriented byte streams, to be able to support IMA system and to be able to support Bonding system.

ATM cells are stored in fifo's from which they are extracted by a Utopia level 1 interface or a Utopia level 2 interface.

In the transmit direction, similar tasks are performed, including idle insertion.

7.3.3 Micro controller mini-platform and Event counter

The DMT-TC module is controlled by a local processor platform containing an ARM7TDMI™, an interrupt controller and some memories.

The Event counter module accumulates DMT-TC statistics: Reed-Solomon corrections, CRC errors, HEC errors …

7.3.4 NTR

Based on the information received within the ADSL frame and based on the digital DPLL output, a network reference clock (typically 8 KHz) can be regenerated. A low-pass filtering is performed on the local micro controller.

7.4 DMT-UTOPIA

Reference spec: Utopia Specification. Level1, Version 2.01, March 1994. Level 2, Version 1.0, June 1995.

See www.atmforum.com

The ST20196 supports both Utopia Level 2 and Level 1 cell based data interface between the PHY layer (within ST20196) and the ATM layer chip. The ATM layer is considered as the reference and all transfers are seen from the ATM layer's point of view. Hence the Transmit direction would be data flow from ATM layer to the PHY layer, while data flow from PHY layer to ATM layer is referred to as Receive direction. In both cases ATM layer is the master.

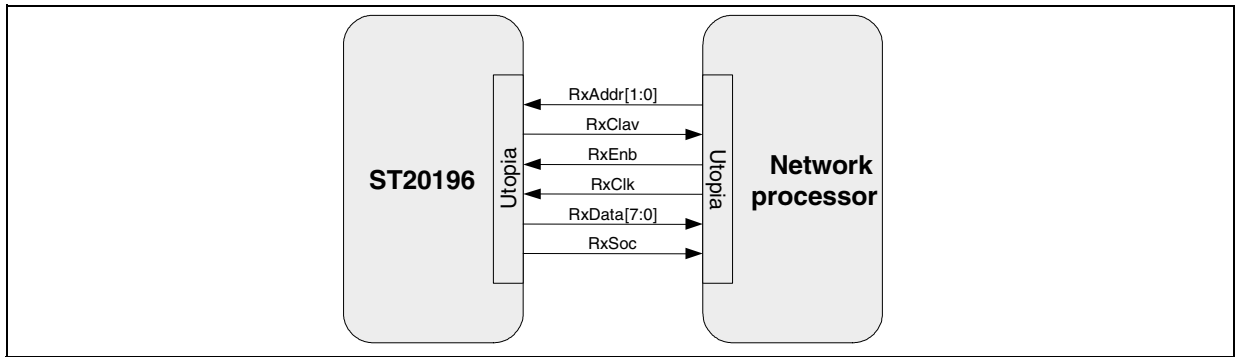**Figure 21. Signals at Utopia Level2 Receive Interface**

Table 13. Receive Interface Signals

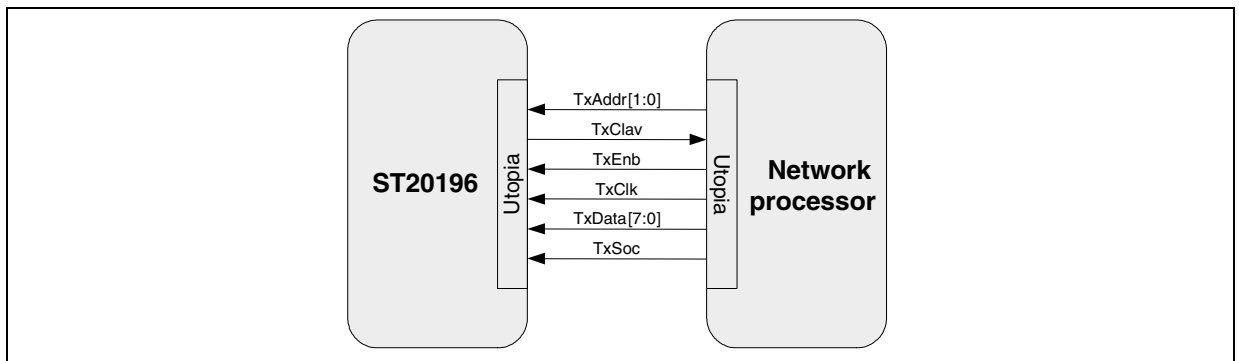| Signal	Description
RxAddr[1:0]	Address used to select the port that will be active or polled
RxData[7:0]	Receive Data Bus, ATM cell data to ATM layer
RxSoc	Start of Cell, indicates the first byte of the cell
RxEnb	Enable (active low), indicates to the ST-20196 when to output cell data
Rxclav	Cell Available, indicates to the ATM layer that the ST-20196 has cell ready for transfer
RxClk	Receive byte clock generated by ATM layer

Figure 22. Signals at Utopia Level2 Transmit Interface

Table 14. Transmit Interface Signal

Signal	Description
TxAddr[1:0]	Address used to select the port that will be active or polled
TxData[7:0]	Transmit Data Bus, ATM cell data from ATM layer
TxSoc	Start of Cell, indicates the first byte of the cell
TxEnb	Enable (active low), indicates to the ST-20196 that TxData and TxSoc are valid
Txclav	Cell Available, indicates to the ATM layer that the ST-20196 has cell ready to accept cell
TxClk	Transmit byte clock generated by ATM layer

Signals are latched on the rising edge of their respective clocks: RxClk or TxClk.

The Utopia Level 2 specification assigns 5 address lines for Receive and Transmit. ST-20196 provides the 2 LSB Rx and Tx address lines to support 2 ATM channels and the required "Idle" channel.

The 3 MSB Receive and Transmit address lines are tied high internally, so that 3 addresses are available: 28, 29 and 30. When the 2 LSB address lines are high ('11') the ST-20196 ATM channel is set to "Idle" channel and 7 addresses are available for other devices (addresses 3, 7, 11, 15, 19, 23 and 27).

7.4.1 UTOPIA Interface Timing
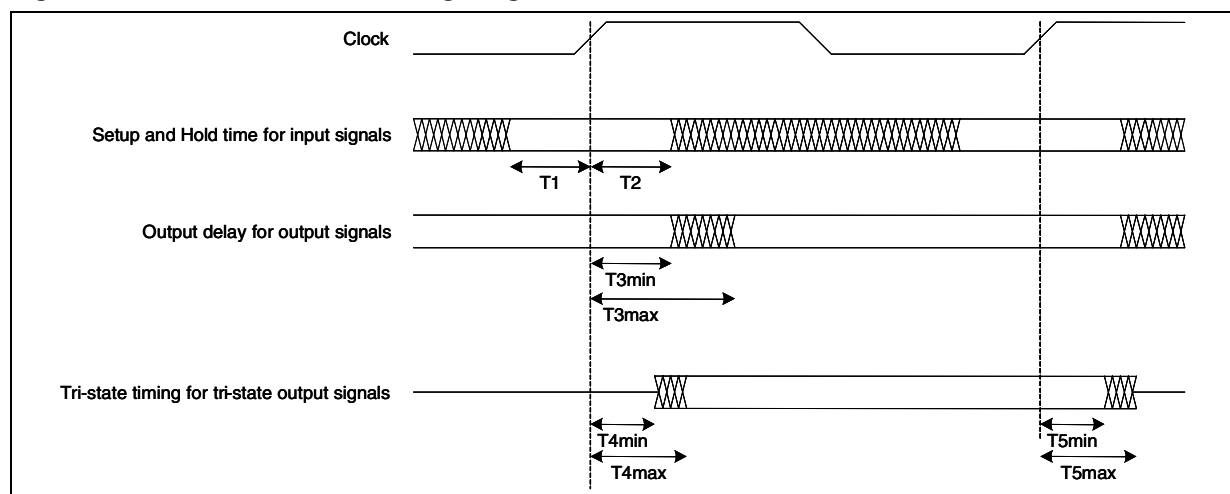
Figure 23. UTOPIA Interface Timing Diagram

Table 15.

Signal			Description	Min.	Max.
RxClk	clock		RxClk frequency	1MHz	50MHz
			RxClk duty cycle	40%	60%
RxEnb	Input	T1	Input setup to RxClk	4 ns	-
		T2	Input hold from RxClk for RxEnb	1.6 ns	-
RxAddr[1:0]	Input	T1	Input setup to RxClk	4 ns	-
		T2	Input hold from RxClk for RxAddr	1 ns	-
RxClav	Output	T3	Output delay from RxClk	1.5 ns	12 ns
		T4	Signal going low impedance from RxClk	1.5 ns	12 ns
		T5	Signal going high impedance from RxClk	1.5 ns	12 ns
RxSOC	Output	T3	Output delay from RxClk	1.5 ns	12 ns
		T4	Signal going low impedance from RxClk	1.5 ns	12 ns
		T5	Signal going high impedance from RxClk	1.5 ns	12 ns
RxData[7:0]	Output	T3	Output delay from RxClk	1.5 ns	12 ns
		T4	Signal going low impedance from RxClk	1.5 ns	12 ns
		T5	Signal going high impedance from RxClk	1.5 ns	12 ns
TxClk	clock		TxClk frequency	1MHz	50MHz
			TxClk duty cycle	40%	60%
TxEnb	Input	T1	Input setup to TxClk	4 ns	-
		T2	Input hold from TxClk	1 ns	-
TxSoc	Input	T1	Input setup to TxClk	4 ns	-
		T2	Input hold from TxClk	1 ns	-
TxAddr[1:0]	Input	T1	Input setup to TxClk	4 ns	-
		T2	Input hold from TxClk	1 ns	-
TxData[7:0]	Input	T1	Input setup to TxClk	4 ns	-
		T2	Input hold from TxClk	1 ns	-
TxClav	Output	T3	Output delay from TxClk	1.5 ns	12 ns
		T4	Signal going low impedance from TxClk	1.5 ns	12 ns
		T5	Signal going high impedance from TxClk	1.5 ns	12 ns

Note:
"The timing values are given for best to worst case operating conditions.
"Setup and hold times for input signals are based 1.5 ns input transition time.
"The output delays are based on 25pF loading capacitance.

8 Electrical Data - General Specifications

8.1 Absolute maximum ratings

Maximum voltage stress without impacting the reliability of the device:

Symbol	Parameter	Value	Unit
VDD IO	Power Supply	3.6	V
VDD CORE	Power Supply	1.32	V

8.2 Operating conditions

Operating ranges define the limits for functional operation and schematic characteristics of the device. Functionality outside these limits is not implied.

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD IO	Power supply	3.0	3.3	3.6	V
VDD CORE	Power supply	1.08	1.2	1.32	V
Tamb	Ambient Temperature	-40		85	degC
Tj	Junction Temperature	-40		125	degC

8.3 Power dissipation

Power dissipation corresponding to an ADSL2+ "show-time" state with maximum throughput and all DMT features activated.

	+0% 25degC	+5% 70degC	+5% 85degC	+10% 70degC	+10% 85degC
Total power (mW)	700	950	1000	1050	1150
I-core (mA)	520	700	740	740	800
I-io (mA)	17	18.5	18.5	20	20

'0%': VDD-IO = 3.3V, VDD-Core = 1.2V
'5%': VDD-IO = 3.47V, VDD-Core = 1.26V
'10%': VDD-IO = 3.6V, VDD-Core = 1.32V

8.4 Thermal characteristics, as per JEDEC JSD51

Thermal resistance junction to ambient	Theta j-a	38.4 degC/W
Thermal resistance junction to case	Theta j-c	9.1 degC/W
Psi junction to top case	Psi j-c	1 degC/W

8.5 IO Characteristics

Table 16. General Interface Electrical Characteristics*

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Vdd	Core Power Supply Voltage		1.08 [1]	1.2	1.32	V
Vdde3v3	3.3V IO Power Supply Voltage		3	3.3	3.6	V
T_j	Operating Junction Temperature		-40	25	85	°C
Ilatchup	I/O Latch-Up Current		200			mA
Vesd [2]	Electrostatic Protection	Leakage < 1u	4000		V	2

Notes: 1. 1.08V is the minimum core voltage to fit electrical specifications. But these IOs functional for a core voltage down to 0.8V (and even 0.7V if vdde3v3 does not exceed 3.3V for 3.3V capable IOs)
2. Human Body Model
3. The 3.3V IOs are functional until 2.2V.
4. The 3.3V IOs comply with the EIA/JEDEC standard JESD8-B

Table 17. LVTTL DC Input Specification (3V<vdde3v3<3.6V)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Vil	Low level Input Voltage				0.8	V
Vih	High level Input Voltage		2			V
Vhyst	Schmitt trigger hysteresis		0.495		0.620	V

Table 18. LVTTL DC Output Specification (3V<vdde3v3<3.6V)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Vcl	Low level output voltage	Iol = XmA [1]			0.15	V
Vch	High level output voltage	Ioh = -XmA [1]	Vdde3v3-0.15			

Notes: 1. X is the source/sink current under worst case contitions and is reflected in the name of the I/O cell according to the drive capability.

Table 19. Pull-up & Pull-down Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Ipu	Pull-up current	Vi = 0V	40	60	110	μA
Ipd	Pull-down current	Vi = Vdde3v3	30	60	133	μA
Rup	Equivalent pull-up resistance	Vi = 0V	32	50	75	kΩ
Rpd	Equivalent pull-down resistance	Vi = Vdde3v3	27	50	100	kΩ

Min condition: Vdde3v3 = 3V, 125°C, min process, Max condition: Vdde3V3 = 3.6V, -40°C, fast process.

8.6 Power-up sequence

8.6.1 CORE-OFF mode

If the 1.2V core supply (VDD-Core) is powered down, whilst there is external activity at the 3.3V interfaces the Output transistors do not experiences stress voltages. In other words external 3.3V activity doesn't damage the IOs, but signals cannot be received or transmitted.

During COREOFF MODE the buffer remains in tri-state mode.

8.6.2 IO-OFF mode

If the 3.3V supply (VDD-IO) is powered down, external activity at the 3.3V interfaces cannot be allowed. Such a mode supports the presence of the 1.2V supply whilst the 3.3V supply is powered down, but doesn't allow activity at the external interface to the pad.

As a result of Core-off and IO-off features, no particular power on/off sequencing between core and IO is required.

Figure 24. Typical power-up sequence
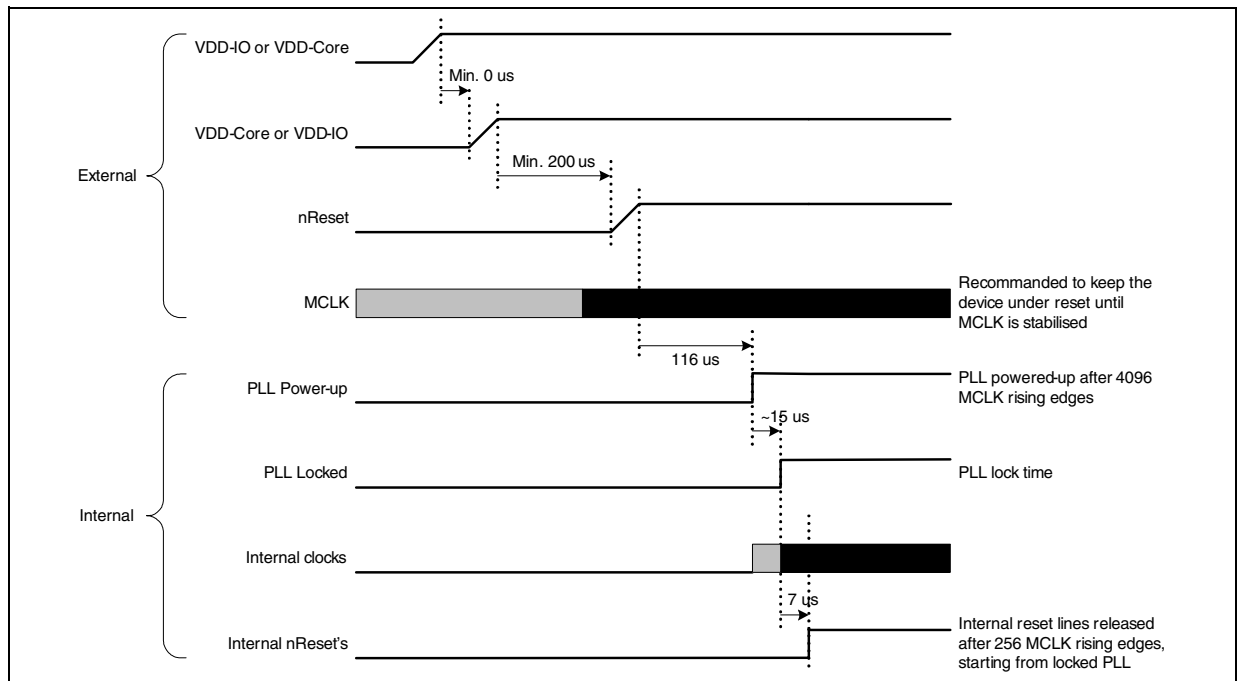
9 Pin description

Table 20. Pin Description

Ball	Signal name	Pad Type		Description
B1	nReset	in	Pull-up SCHMIT	Chip Reset, active low. Minimum reset pulse width: 30 ns. With shorter pulse, ST-20196 behavior is unpredictable.
N13	MCLK	in	SCHMIT	Master clock 35.328 MHz
C3	ProcSpeed	in		ARM946™ clock speed. To be strapped to VDD
D3	AhbSpeed	in		Internal AHB Bus speed. To be strapped to GND
D1	TROM	in		Boot mode: GND: from internal ROM VDD: from external Flash EPROM
R14	IRQ	in		General purpose IRQ used for Dying Gasp detection
J14	NTR	out	Tri-state	NTR, 8KHz Network Reference clock
E1	PA[0]	inout		GPIO A bit[0]
D2	PA[1]	inout		GPIO A bit[1] (used for LED indication)
E4	PA[2]	inout		GPIO A bit[2] (used for LED indication)
E2	PA[3]	inout		GPIO A bit[3]
G3	PA[4]	inout		GPIO A bit[4]
G4	PA[5]	inout		GPIO A bit[5]
H1 (H2)	PA[6]	inout		GPIO A bit[6]
H3 (J3)	PA[7]	inout		GPIO A bit[7]
C2	F_nCS	out	Tri-state	FLASH Chip select
N10	F_nOE	out	Tri-state	FLASH output enable
T11	S_nCS	out	Tri-state	SDRAM chip select
E3	S_CLK	inout		SDRAM clock, 35.328MHz
F1 (F2)	SF_nWE	out	Tri-state	SDRAM-FLASH write enable
F3	S_nRAS	out	Tri-state	SDRAM Row Address strobe / Flash A19
F4	S_nCAS	out	Tri-state	SDRAM Column Address strobe / Flash A18
G1	S_DQM[0]	out	Tri-state	SDRAM Lower DQ mask enable / Flash A17
G2	S_DQM[1]	out	Tri-state	SDRAM Upper DQ mask enable / Flash A16
R3 (P4)	E_A[0]	inout		EBI address bus
T1 (T2)	E_A[1]	inout		EBI address bus
N4 (N3)	E_A[2]	inout		EBI address bus
P2 (P3)	E_A[3]	inout		EBI address bus
R1 (R2)	E_A[4]	inout		EBI address bus
M3 (M4)	E_A[5]	inout		EBI address bus
P1 (N2)	E_A[6]	inout		EBI address bus
N1	E_A[7]	inout		EBI address bus
L4	E_A[8]	inout		EBI address bus
M2	E_A[9]	inout		EBI address bus
M1	E_A[10]	inout		EBI address bus
L3	E_A[11]	inout		EBI address bus
L2	E_A[12]	inout		EBI address bus
L1	E_A[13]	inout		EBI address bus

Table 20. Pin Description (continued)

Ball	Signal name	Pad Type		Description
K4	E_A[14]	inout		EBI address bus
K3	E_A[15]	inout		EBI address bus
T3 (R4)	E_D[0]	inout		EBI data bus
P5 (N5)	E_D[1]	inout		EBI data bus
T4 (R5)	E_D[2]	inout		EBI data bus
P6 (N6)	E_D[3]	inout		EBI data bus
T5 (R6)	E_D[4]	inout		EBI data bus
T7 (T6)	E_D[5]	inout		EBI data bus
R7 (P7)	E_D[6]	inout		EBI data bus
N7 (P8)	E_D[7]	inout		EBI data bus
T8	E_D[8]	inout		EBI data bus
R8	E_D[9]	inout		EBI data bus
T9	E_D[10]	inout		EBI data bus
R9	E_D[11]	inout		EBI data bus
P9	E_D[12]	inout		EBI data bus
T10	E_D[13]	inout		EBI data bus
R10	E_D[14]	inout		EBI data bus
P10	E_D[15]	inout		EBI data bus
P15	AFRXD[0]	in		AFE receive data bus
R16	AFRXD[1]	in		AFE receive data bus
P14	AFRXD[2]	in		AFE receive data bus
R15	AFRXD[3]	in		AFE receive data bus
T13	AFRXD[4]	in		AFE receive data bus
N11	AFRXD[5]	in		AFE receive data bus
R12	AFRXD[6]	in		AFE receive data bus
T12	AFRXD[7]	in		AFE receive data bus
P11	AFRXD[8]	in		AFE receive data bus
R11	AFRXD[9]	in		AFE receive data bus
T15	AFTXD[0]	out	Tri-state	AFE transmit data bus
R13	AFTXD[1]	out	Tri-state	AFE transmit data bus
T14	AFTXD[2]	out	Tri-state	AFE transmit data bus
P12	AFTXD[3]	out	Tri-state	AFE transmit data bus
T16	CLWD	in		AFE data word clock
P13	AFE_CTR_OUT	out	Tri-state	AFE serial control data out
N12	AFE_CTRL_IN	in		AFE serial control data in
B5	Power_Down	out	Tri-state	AFE power down
P16	TxAddr[0]	in		UTOPIA Tx Address
N14	TxAddr[1]	in		UTOPIA Tx Address
N15	TxData[0]	in		UTOPIA Tx Data
M13	TxData[1]	in		UTOPIA Tx Data
N16	TxData[2]	in		UTOPIA Tx Data
M15	TxData[3]	in		UTOPIA Tx Data
M14	TxData[4]	in		UTOPIA Tx Data

Table 20. Pin Description (continued)

Ball	Signal name	Pad Type		Description
L13	TxData[5]	in		UTOPIA Tx Data
M16	TxData[6]	in		UTOPIA Tx Data
L16	TxData[7]	in		UTOPIA Tx Data
L15	TxEnb	in		UTOPIA Tx Enable
L14	TxClav	out	Tri-state	UTOPIA Tx Cell Available
K16	TxSoc	in		UTOPIA Tx Start Of Cell
K15	TxClk	in	SCHMIT	UTOPIA Tx Clock
G13	RxAddr[0]	in		UTOPIA Rx address
C16	RxAddr[1]	in		UTOPIA Rx address
E14	RxData[0]	out	Tri-state	UTOPIA Rx data
D16	RxData[1]	out	Tri-state	UTOPIA Rx data
F13	RxData[2]	out	Tri-state	UTOPIA Rx data
E15	RxData[3]	out	Tri-state	UTOPIA Rx data
E16	RxData[4]	out	Tri-state	UTOPIA Rx data
F14	RxData[5]	out	Tri-state	UTOPIA Rx data
F15	RxData[6]	out	Tri-state	UTOPIA Rx data
F16	RxData[7]	out	Tri-state	UTOPIA Rx data
K14	RxEnb	in		UTOPIA Rx Enable
K13	RxClav	out	Tri-state	UTOPIA Rx Cell Available
J16	RxSoc	out	Tri-state	UTOPIA Rx Start Of Cell
J15	RxClk	in	SCHMIT	UTOPIA Rx Clock
A13	C_A[0]	in (inout)		Ctrl-E address bus
B14	C_A[1]	in (inout)		Ctrl-E address bus
A14	C_A[2]	in (inout)		Ctrl-E address bus
B15	C_A[3]	in (inout)		Ctrl-E address bus
A15	C_A[4]	in (inout)		Ctrl-E address bus
C14	C_A[5]	in (inout)		Ctrl-E address bus
B16	C_A[6]	in (inout)		Ctrl-E address bus
E13	C_A[7]	in (inout)		Ctrl-E address bus
D15	C_A[8]	in (inout)		Ctrl-E address bus
B10	C_D[0]	inout		Ctrl-E data bus
A10	C_D[1]	inout		Ctrl-E data bus
B11	C_D[2]	inout		Ctrl-E data bus
A11	C_D[3]	inout		Ctrl-E data bus
B12	C_D[4]	inout		Ctrl-E data bus
A12	C_D[5]	inout		Ctrl-E data bus
C12	C_D[6]	inout		Ctrl-E data bus
B13	C_D[7]	inout		Ctrl-E data bus
C10	C_notCS	in (inout)		Ctrl-E chip select
A9	C_notWr	in (inout)		Ctrl-E write indication
A8	C_notRd	in (inout)		Ctrl-E read indication
B7	C_notRdy	out	Tri-state	Ctrl-E ready indication
A6	C_notInt	out	Tri-state	Ctrl-E interface interrupt
C5	C_mode	in		Ctrl-E mode select

Table 20. Pin Description (continued)

Ball	Signal name	Pad Type		Description	
A4	U1_RXD	in	Pull-up	Processor platform UART RXD	
B4	U1_TXD	out	Tri-state	Processor platform UART TXD	
C7	U1_RTS	out	Tri-state	Processor platform UART RTS	
A7	U1_CTS	in	Pull-up	Processor platform UART CTS	
H16	U2_RXD	in	Pull-up	ADSL TC UART RXD	For FW Development. Typically unconnected.
H15	U2_TXD	out	Tri-state	ADSL TC UART TXD	
H14	U2_CTS	in	Pull-up	ADSL TC UART CTS	
G16	U2_RTS	out	Tri-state	ADSL TC UART RTS	
C6	Scan_enable	in		Test scan enable. For test purpose. To be strapped to GND.	
G15	JMODE[0]	in	Pull-up	JTAG ports configuration.	For FW Development. Typically unconnected.
G14	JMODE[1]	in	Pull-up	JTAG ports configuration.	
A5	MODE[0]	in		Mode of operation. For test purpose. To be strapped to GND.	
B6	MODE[1]	in			
A3	MODE[2]	in			
C4	nTRST	in	Pull-down	JTAG port 1, reset	Typically connected to BSCAN logic.
B3	TCK	in	Pull-up	JTAG port 1, clock	
B2	TMS	in	Pull-up	JTAG port 1, mode select	
A1	TDI	in	Pull-up	JTAG port 1, data in	
D4	TDO	out	Tri-state	JTAG port 1, data out	
J1	J2_nTRST	in	Pull-down	JTAG port 2, reset	For FW Development. Typically unconnected.
J2	J2_TCK	in	Pull-up	JTAG port 2, clock	
K1	J2_TMS	in	Pull-up	JTAG port 2, mode select	
K2	J2_TDI	in	Pull-up	JTAG port 2, data in	
C1	J2_TDO	out	Tri-state	JTAG port 2, data out	
J4 N9 H13 D8	VDD Core	power		Internally connected together	
H4 N8 J13 D9	VDD IO	power		Internally connected together	

Table 20. Pin Description (continued)

Ball	Signal name	Pad Type		Description
H8 J8 J9 H9 G7 H7 J7 K7 K8 K9 K10 J10 H10 G10 G9 G8	VSS IO/Core	ground		Internally connected together
B8	VDD PLL A	power		analog supply for PLL, 3.3V
B9	VDD PLL D	power		digital supply for PLL, 1.2V
C9	VSS PLL A	ground		analog ground for PLL, 3.3V
C8	VSS PLL D	ground		digital ground for PLL, 1.2V
A2 D5 D6 D7 D10 C11 D11 D12 C13 D13 D14 C15 A16	Unused			To be kept unconnected

Notes:
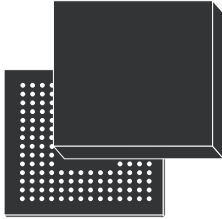
1. A few signals are bonded to 2 balls. Keep unconnected the balls specified between parentheses. Example: "H1 (H2)" ' keep un-connect ball H2. It will be then in line with the BSDL file that can be delivered on request.
2. Some CTRL-E input pins are based on bidirectional IO's for test purpose. Example: signal C_A[0] ' pad type "in (inout)".
3. Decoupling strategy recommended:
     - VDD-IO plane bulk decoupling: 10 uF
     - VDD-Core plane bulk decoupling: 10 uF
     - VDD-IO high frequency decoupling: 10 nF as close as possible of each respective balls
     - VDD-Core high frequency decoupling: 10 nF as close as possible of each respective balls
     - VDD-PLL-A: separate track with 10 uF and 10 nF decoupling
     - VDD-PLL-D: can be connected to the same plane as VDD-Core, with also the 10nF decoupling
     - VSS-IO, VSS-Core, VSS-PLL-A, VSS-PLL-D can be connected to a common ground plane.
4. It's recommended to foresee access to the processor platform UART (balls U1_xxx) even if not use by the application in order to allow "DSP-info" tool for prototyping debugging.

10 Package Information

Figure 25. LBGA208 Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**
A	1.210		1.700	0.048		0.067
A1	0.270			0.011		
A2		1.120			0.044	
b	0.450	0.500	0.550	0.018	0.020	0.022
D	16.80	17.00	17.20	0.661	0.669	0.677
D1		15.00			0.590	
E	16.80	17.00	17.20	0.661	0.669	0.677
E1		15.00			0.590	
e	0.90	1.00	1.10	0.035	0.039	0.043
f	0.75	1.00	1.250	0.029	0.039	0.049
ddd			0.200			0.008

OUTLINE AND MECHANICAL DATA

**LBGA208 (17x17x1.70)
Low Profile Ball Grid Array**

NOTE 1
- The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heatslug.
- A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner.
- Exact shape of each corner is optional.

LBGA208M

7184626B
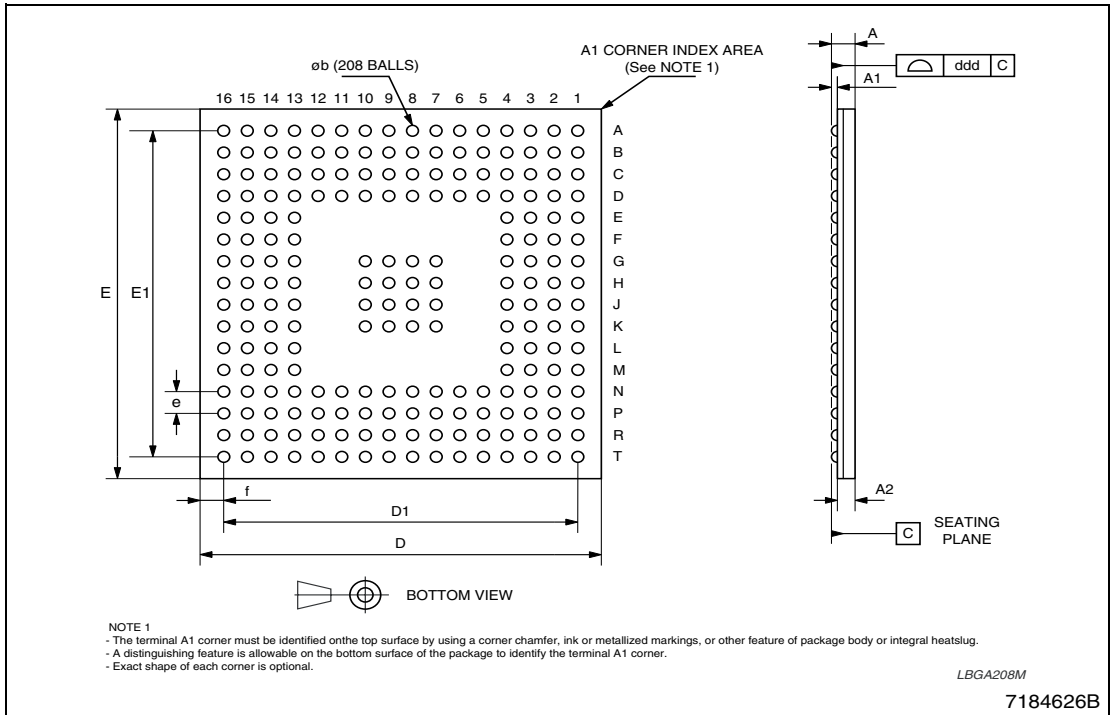
11 Revision History

Table 21. Revision History

Date	Revision	Description of Changes
February 2005	1	First Issue

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