NEC

MOS INTEGRATED CIRCUIT

μPD72001-11, 72001-A8

MULTI-PROTOCOL SERIAL CONTROLLERS

DESCRIPTION

The μPD72001-11 is an MPSC (Multi-Protocol Serial Controller) which is a general-purpose communication LSI equipped with two sets of bidirectional parallel/serial converter circuits for data communication. This controller has a transmitter function to convert the parallel data output by a data terminal into serial data and transmit this data to a data transmission system such as a modem, and a receiver function to convert the serial data output by the data transmission system into parallel data.

The MPSC can be used with data communications equipment with a variety of communication modes such as the generally and widely used start-stop synchronization mode, and the HDLC mode which is used for high-speed communication.

The μPD72001-A8 is a low-voltage model.

For this product, the following documents are separately available. Read these documents as well as this Data Sheet.

- User's Manual (S12472E)
- Application Notes
  - (I) (S12753E)
  - (II) (On preparation)
  - (III) (On preparation)

FEATURES

- Two sets of parallel/serial circuits supporting three modes: start-stop synchronization, character synchronization, and bit synchronization modes
  → Easy application to a system supporting two or more communication protocols such as a protocol converter or ISDN terminal adapter
- DPLL (Digital Phase Locked Loop), baud rate generator, and crystal oscillation circuit for transmission/reception clock
  → Helps reduce cost by decreasing the number of external circuits
- Many variations with power-saving features and small package size
  → Easy application to portable terminals and high-accuracy portable terminals

The features common to the μPD72001-11 and 72001-A8 are explained as the features of the MPSC in this document.

Document No. S12184EJ7V0DS00 (7th edition)
Date Published November 1997 N
Printed in Japan

The mark ★ shows major revised points.

ORDERING INFORMATION

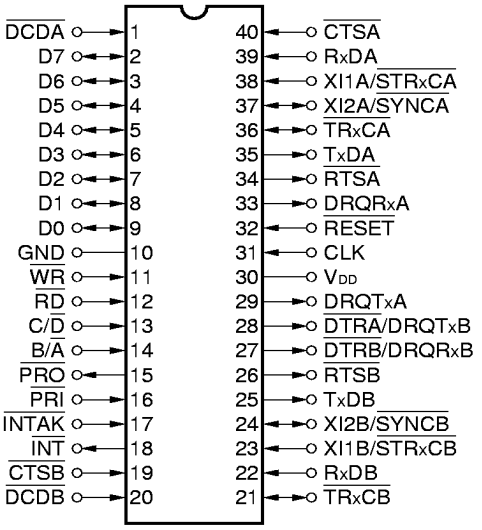
Part Number	Package
μPD72001C-11	40-pin plastic DIP (600 mil)
μPD72001G-11-22	44-pin plastic QFP (10 × 10 mm) (resin thickness: 1.45 mm)
μPD72001GC-11-3B6	52-pin plastic QFP (14 × 14 mm) (resin thickness: 2.7 mm)
μPD72001L-11	52-pin plastic QFJ (750 × 750 mil)
μPD72001C-A8	40-pin plastic DIP (600 mil)
μPD72001G-A8-22	44-pin plastic QFP (10 × 10 mm) (resin thickness: 1.45 mm)
μPD72001GC-A8-3B6	52-pin plastic QFP (14 × 14 mm) (resin thickness: 2.7 mm)

SPECIFICATIONS

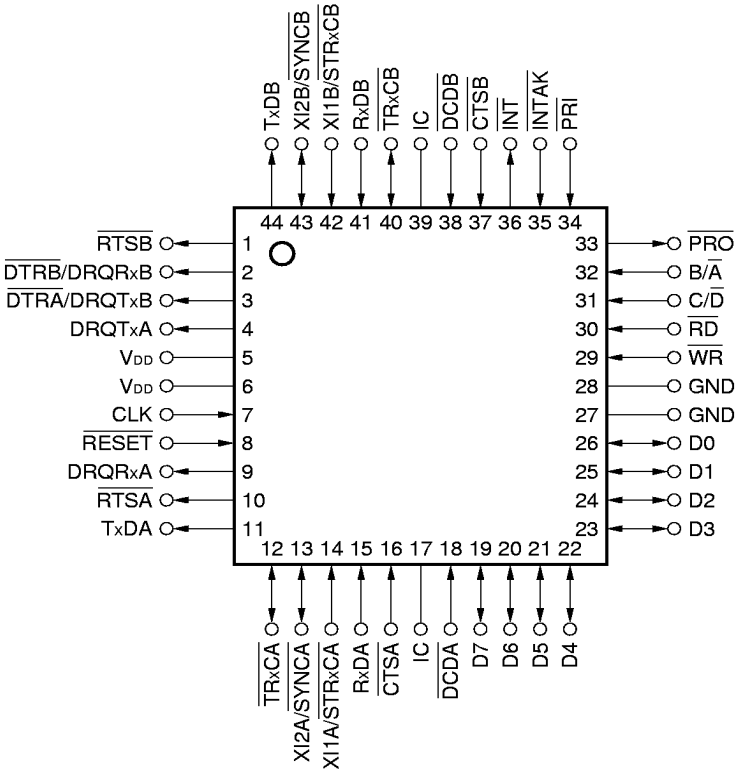
Item	Specifications	
Part number	μPD72001-11	μPD72001-A8
Supply voltage	5 V ±10 %	3.3 V ±0.3 V
★ System clock frequency	11 MHz MAX.	8 MHz MAX. (at T_A = –10 to +70 °C) 7.14 MHz MAX. (at T_A = –40 to +85 °C)
★ Maximum transfer rate	2.2 Mbps	1.6 Mbps (at T_A = –10 to +70 °C) 1.43 Mbps (at T_A = –40 to +85 °C)
Process	CMOS	
Internal circuit	Parallel/serial converter circuit: Full-duplex channel × 2 Transmit buffer : Double Receive buffer : Quadruple Interrupt control function DMA request signal output: 2 for transmission, 2 for reception Overrun error detection DPLL Baud rate generator Crystal oscillation circuit for transmission/reception clock generation Self-loopback test function Standby function General-purpose I/O pin: 4 pins × 2	
Communication protocol	Start-stop synchronization	Character bit length: 5, 6, 7, 8 Stop bit length: 1, 1.5, 2 Clock rate: ×1, ×16, ×32, ×64 Parity generation, check Framing error detection Break generation, detection
	COP (Character Oriented Protocol)	Operation mode: Mono-sync, Bi-sync, External sync Character bit length: 5, 6, 7, 8 SYNC character bit length: 6, 8 Character synchronization: Internal/external BCS (Block Check Sequence) generation, check: CRC-16 CRC-CCITT Parity generation, check SYNC character automatic transmission, detection, rejection
	BOP (Bit Oriented Protocol)	Operation mode: HDLC (High-level Data Link Control) SDLC (Synchronous Data Link Control) SDLC Loop Flag transmission, detection Zero insertion, rejection Address field detection (1 byte) FCS (Frame Check Sequence) generation, detection Short frame detection Abort automatic transmission, detection Idle detection Go Ahead detection Transmit number data control
Processing data format	Encode/decode of NRZ (Non-Return to Zero) Encode/decode of NRZI (Non-Return to Zero Inverted) Encode/decode of FM (Frequency Modulation) Decode in Manchester mode	

PIN CONFIGURATION (Top View)

- **40-pin plastic DIP (600 mil) : μPD72001C-11, μPD72001C-A8**

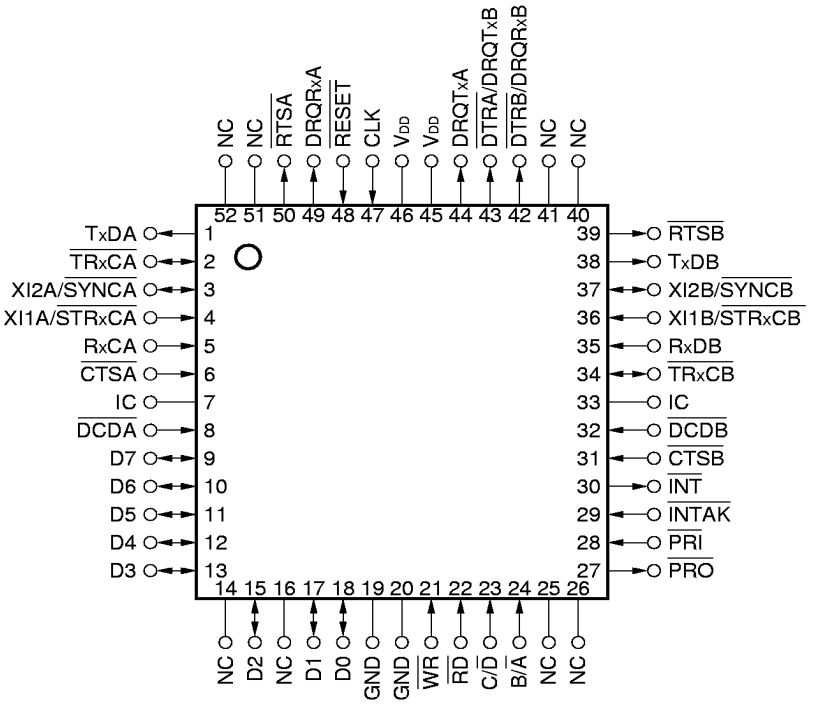


- **44-pin plastic QFP (10 × 10 mm) : μPD72001G-11-22, μPD72001G-A8-22**



IC: Internally Connected (Leave this pin unconnected)

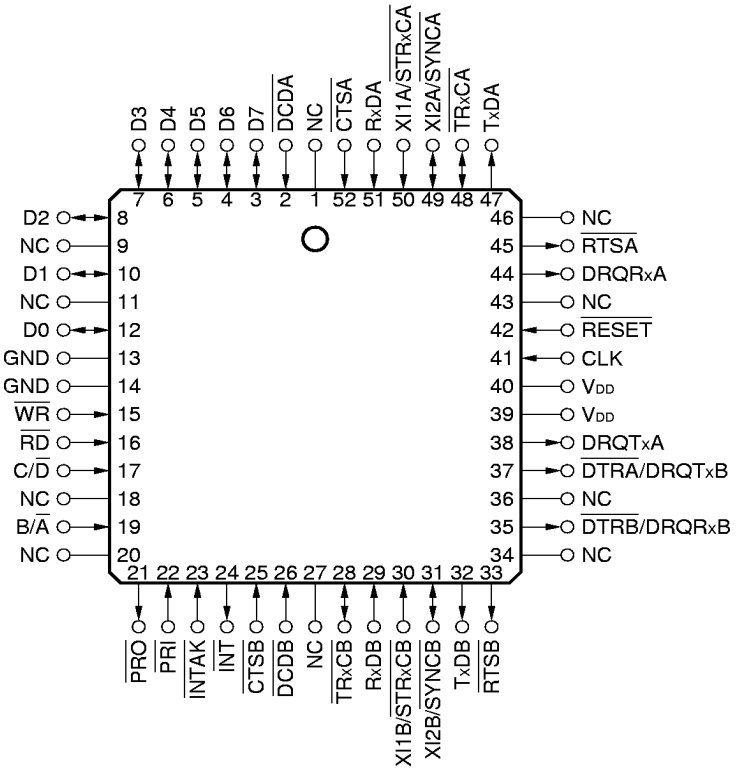
• **52-pin plastic QFP (14 × 14 mm) : μPD72001GC-11-3B6, μPD72001GC-A8-3B6**



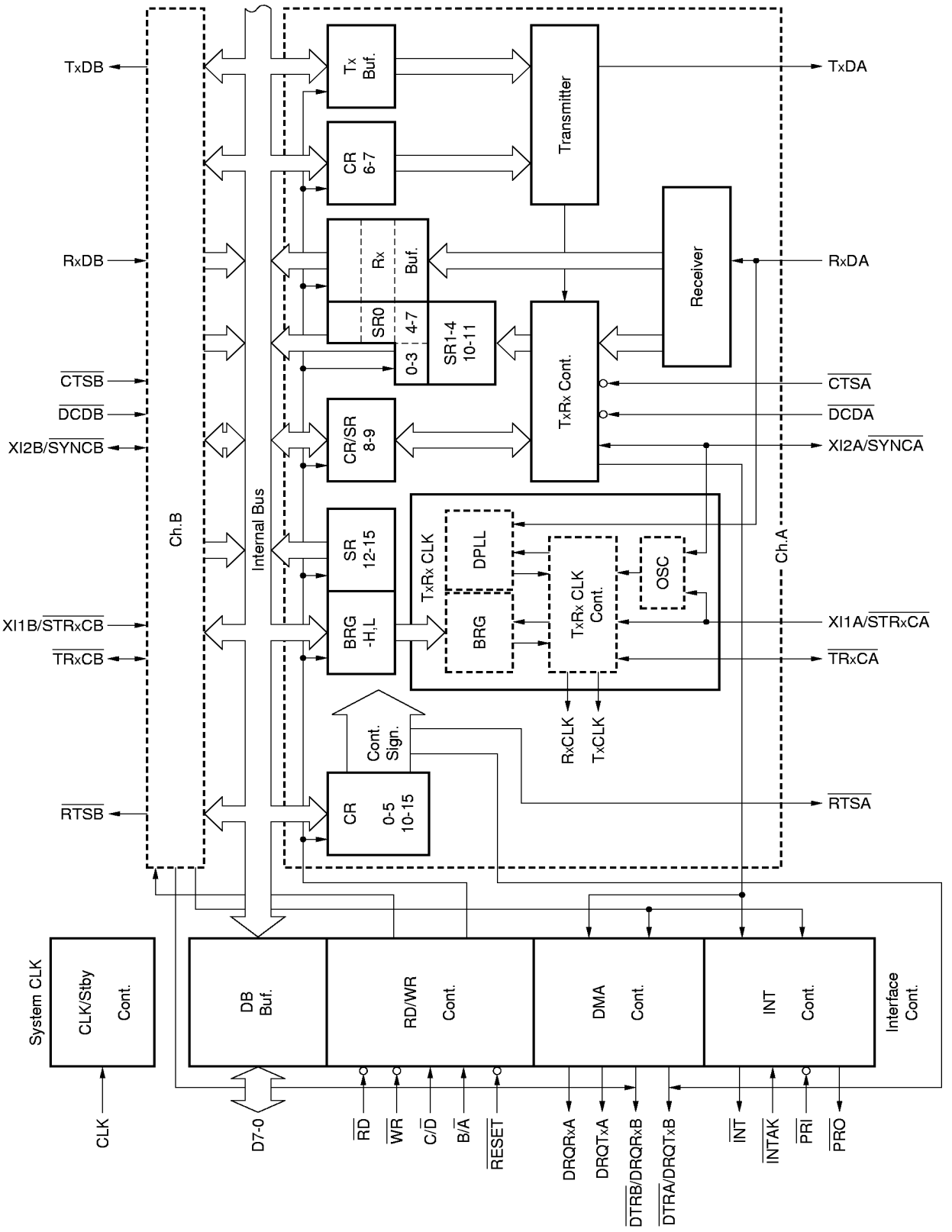
NC: No Connection

IC : Internally Connected (Leave this pin unconnected.)

• **52-pin plastic QFJ (750 × 750 mil) : μPD72001L-11**



BLOCK DIAGRAM



1. PIN FUNCTIONS

The functions of the MPSC can be broadly classified into "system interface functions" that control interfacing with the host system, and "transmission/reception functions" to transmit or receive data. This section explains the functions of the pins of the MPSC by classifying the pins into those related to system interfacing and those related to transmission and reception.

Hereafter, "H" (voltage level satisfying V_{IH} in the case of an input pin, or voltage level satisfying V_{OH} in the case of an output pin) and "L" (voltage level satisfying V_{IL} in the case of an input pin, or voltage level satisfying V_{OL} in the case of an output pin) are used to indicate the input/output status of a pin.

1.1 Pins Related to System Interface

(1) V_{DD}
Supply voltage pin

(2) GND
GND pin

(3) $\overline{RESET}$ ... Input
This pin inputs a signal from an external device to reset the MPSC. When "L" is input to this pin for the duration of 2 clock cycles ($2t_{CYK}$) or longer, the MPSC is reset (this is called system reset).
As a result of system reset, the transmitter, receiver, and interrupt/DMA functions of the MPSC are disabled, and the TxD pin and general-purpose output pins go high. In this case, because all bits of the control register (CR) are also reset, CR must be set again if a system reset has been executed.
Table 1-1 shows the status of each pin at system reset, in comparison with the pin status at channel reset (CR0: D5, D4, D3 = "0, 1, 1").
The MPSC automatically enters the standby mode at system reset, lowering the power consumption from that in the normal operation mode.

Table 1-1. Pin Status at Reset

Pin Name	I/O	Pin Status	
		$\overline{\text{RESET}}$ (system reset)	Channel reset
$\overline{\text{WR}}$	I	–	–
$\overline{\text{RD}}$	I	–	–
B/$\overline{\text{A}}$	I	–	–
C/$\overline{\text{D}}$	I	–	–
D7 to D0	I/O	–	–
$\overline{\text{INT}}$	O	High impedance	High impedance
$\overline{\text{INTAK}}$	I	–	–
$\overline{\text{PRI}}$	I	–	–
$\overline{\text{PRO}}$	O	Depends on $\overline{\text{PRI}}$	Depends on $\overline{\text{PRI}}$
DRQTxA	O	"L"	"L"
DRQRxA	O	"L"	"L"
$\overline{\text{DTRA}}$/DRQTxB, $\overline{\text{DTRB}}$/DRQRxB	O	$\overline{\text{DTR}}$ function, "H"	Retains current status
TxDA, TxDB	O	"H"	"H"
RxDA, RxDB	I	–	–
$\overline{\text{TRxCA}}$, $\overline{\text{TRxCB}}$	I/O	Input status	Retains current status
XI1A/$\overline{\text{STRxCA}}$ XI1B/$\overline{\text{STRxCB}}$	I	–	–
XI2A/$\overline{\text{SYNCA}}$ XI2B/$\overline{\text{SYNCB}}$	I/O	Input status	Retains current status
$\overline{\text{RTSA}}$, $\overline{\text{RTSB}}$	O	"H"	"H"
$\overline{\text{CTSA}}$, $\overline{\text{CTSB}}$	I	–	–
$\overline{\text{DCDA}}$, $\overline{\text{DCDB}}$	I	–	–

– : Undefined

(4) CLK (System Clock) ... Input

This pin inputs the system clock. The input frequency must be five times that of the data transfer rate or higher.

(5) $\overline{\text{WR}}$ (Write) ... Input

This pin inputs a write control signal for control words and transmit data. This pin is active-low.

(6) $\overline{\text{RD}}$ (Read) ... Input

This pin inputs a read control signal for status and receive data. This pin is active-low.

(7) B/$\overline{\text{A}}$ (Channel B/Channel A) ... Input

This pin inputs a signal to select a channel to be accessed when data is written or read. When this pin is "L", channel A is selected; when it is "H", channel B is selected.

(8) C/$\overline{\text{D}}$ (Control/Data) ... Input

This pin inputs a signal that determines the type of the data on the data bus when the data is written or read.

Table 1-2 shows the selection operations by $\overline{WR}$, $\overline{RD}$, B/$\overline{A}$, and C/$\overline{D}$.

Table 1-2. MPSC Control Signals and Operations

$\overline{WR}$	$\overline{RD}$	B/$\overline{A}$	C/$\overline{D}$	Operation	
L	H	L	L	Channel A	Writes transmit data to Tx buffer
		H		Channel B	
H	L	L	L	Channel A	Reads receive data from Rx buffer
		H		Channel B	
L	H	L	H	Channel A	Writes control register
		H		Channel B	
H	L	L	H	Channel A	Reads status register
		H		Channel B	
H	H	×	×	High-impedance state or $\overline{INTAK}$ sequence	
L	L	×	×	Setting prohibited	

× : Don's Care

(9) D7 through D0 (Data Bus) ... I/O

These pins constitute a three-state 8-bit bidirectional data bus. This data bus is connected to the data bus of the host processor to transfer control words, status, and transmit/receive data.

(10) $\overline{INT}$ (Interrupt) ... Output (open drain)

This pin outputs an interrupt request signal. If an interrupt occurs in the MPSC, it goes low (active). Because this is an open-drain output pin, it must be pulled up.

(11) $\overline{INTAK}$ (Interrupt Acknowledge) ... Input

This pin inputs a signal to acknowledge interrupt request signals issued by the MPSC. This pin is active-low. This pin is used when the vector mode (CR2A: D7 = "1") is selected, and must be pulled up to "H" when the non-vector mode (CR2A: D7 = "0") is selected.

(12) $\overline{PRI}$ (Priority Input) ... Input

This input pin is used for an interrupt generation request signal and for an output control signal for interrupt vectors. In the normal operation mode, this pin provides an interrupt generation control function. During the INTAK sequence, it provides an output control function for interrupt vectors. How this pin is used differs depending on the interrupt mode.

(a) In vector mode (CR2A: D7 = "1")

In the normal operation mode, the $\overline{PRI}$ pin is used to control generation of interrupts. When interrupt vector output mode of Type A-3 or Type B-2 (CR2A: D5, D4, D3 = "0, 1, 0" or "1, 0, 0") is selected, interrupts can be generated regardless of whether the $\overline{PRI}$ pin is "L" or "H".

If any other interrupt vector output mode is selected, the $\overline{PRI}$ pin must be kept "L" to enable generation of interrupts.

During the INTAK sequence, an interrupt vector is output if "L" is input to the $\overline{PRI}$ pin in any interrupt vector output mode, and output of the interrupt vector is disabled if "H" is input to $\overline{PRI}$.

(b) Non-vector mode (CR2A: D7 = "0")

In this mode, the $\overline{PRI}$ pin controls only the generation of interrupts because the INTAK sequence is not used. If an interrupt vector output mode other than Type A-3 and Type B-2 is selected, generation of an interrupt signal is enabled if "L" is input to the $\overline{PRI}$ pin. The interrupt signal is not generated if "H" is input to $\overline{PRI}$. If an interrupt daisy chain is configured, inputting "L" to this pin indicates that a device having a higher priority does not acknowledge interrupt processing or does not have an interrupt request, and only the MPSC with "L" input to its $\overline{PRI}$ pin can generate an interrupt.

(13) $\overline{PRO}$ (Priority Output) ... Output

This pin is used when an interrupt daisy chain is configured. This output pin is active-low, and controls generation of interrupts requests from a device with a lower priority. Usually, this pin is used along with the $\overline{PRI}$ pin, and its operation is as follows:

When $\overline{PRI}$ = "H", $\overline{PRO}$ = "H"

When $\overline{PRI}$ = "L", $\overline{PRO}$ goes "H" if there is an interrupt request, and goes "L" if there is no interrupt request.

(14) DRQTxA (DMA Request TxA) ... Output

This pin outputs a DMA request to a DMA controller. This pin is active-high. It goes "H" if the transmitter of channel A has entered the Tx Buffer Empty status. The condition under which this pin goes "H" differs as follows depending on the setting of the CR1 and D2 bits.

CR1: D2 = "0": The DRQTxA pin goes "H" when the transmitter has entered the Tx Buffer Empty status after the first transmit data has been written. It does not go "H" when the transmitter has entered the Tx Buffer Empty status after reset.

CR1: D2 = "1": The DRQTxA pin goes "H" when the transmitter has entered the Tx Buffer Empty status.

This signal is reset when transmit data has been written to channel A.

(15) DRQRxA (DMA Request RxA) ... Output

This pin outputs a DMA request to a DMA controller. This pin is active-high and goes "H" if the receiver of channel A has entered the Rx Character Available status. This signal is reset only when receive data has been read from channel A.

(16) $\overline{DTRA}$/DRQTxB (Data Terminal Ready A/DMA Request TxB) ... Output

The function of this pin is changed as follows depending on the setting of CR2A: D1 and D0.

(a) When CR2A: D1, D0 = "0, 0" or "0, 1"

This pin functions as the $\overline{DTRA}$ pin. This pin is a general-purpose output pin and can be used to control a modem, etc. The operation of the $\overline{DTRA}$ pin is as follows:

When CR5A: D7 = "0", $\overline{DTRA}$ = "H"

When CR5A: D7 = "1", $\overline{DTRA}$ = "L"

(b) When CR2A: D1, D0 = "1, 0"

This pin functions as the DRQTxB output pin. The function of this pin is the same as the DRQTxA pin, except this pin is used with channel B.

(17) $\overline{DTRB}$/DRQRxB (Data Terminal Ready B/DMA Request RxB) ... Output

The function of this pin changes as follows depending on the setting of CR2A: D1 and D0.

(a) When CR2A: D1, D0 = "0, 0" or "0, 1"
This pin functions as the $\overline{DTRB}$ output pin. The function of this pin is the same as the $\overline{DTRA}$ pin, except this pin is used with channel B.

(b) When CR2A: D1, D0 = "1, 0"
This pin functions as the DRQRxB output pin. The function of this pin is the same as the DRQRxA pin, except this pin is used with channel B.

(18) $\overline{CTSA}$ (Clear to Send A) and $\overline{CTSB}$ (Clear to Send B) ... Input
This pin is a general-purpose input pin and can be used to control a modem, etc. Changes in the status of this pin affect the latching operation of the E/S bit. When E/S INT is enabled (CR1: D0 = "1"), the E/S interrupt is generated.
If the Auto Enable mode (CR3: D5 = "1") is set, the transmitter can be controlled by using the Tx Enable bit (CR5: D3) and this pin. This is illustrated in Table 1-3.

Table 1-3. Auto Enable Mode and $\overline{CTS}$ Pin

$\overline{CTS}$ Pin	Tx Enable Bit	Transmitter Status
L	1	Enabled
H	1	Disabled
H or L	0	Disabled

(19) $\overline{DCDA}$ (Data Carrier Detect A) ... Input
$\overline{DCDB}$ (Data Carrier Detect B) ... Input
These are general-purpose input pins and can be used to control a modem, etc. Changes in the status of this pin affect the latching operation of the E/S bit. When E/S INT is enabled (CR1: D0 = "1"), the E/S interrupt is generated.
If the Auto Enable mode (CR3: D5 = "1") is set, the receiver can be controlled by using the Rx Enable bit (CR3: D0) and this pin. This is illustrated in Table 1-4.

Table 1-4. Auto Enable Mode and $\overline{DCD}$ Pin

$\overline{DCD}$ Pin	Rx Enable Bit	Receiver Status
L	1	Enabled
H	1	Disabled
H or L	0	Disabled

(20) $\overline{RTSA}$ (Request to Send A) ... Output
$\overline{RTSB}$ (Request to Send B) ... Output
These are general-purpose output pins and can be used to control a modem, etc. The operations of these pins differ depending on the setting of the operation protocol and the setting of the Auto Enable bit, as shown in Table 1-5.

Table 1-5. Auto Enable Bit and $\overline{\text{RTS}}$ Pin

Function / Protocol	Auto Enable Bit	RTS Cont. Bit	$\overline{\text{RTS}}$ Pin Status
Start-stop synchronization	0	0	H
		1	L
	1	When "0" from beginning	H
		If set to "1" once and then reset to "0"	If "L" while All Sent[Note] = "0", and "H" if All Sent = "1"
		1	L
COP/BOP	Don't Care	0	H
		1	L

Note SR1: D2

1.2 Pins Related to Transmission/Reception

(1) TxDA (Transmit Data A) and TxDB (Transmit Data B) ... Output
These pins output transmit data.

(2) RxDA (Receive Data A) and RxDB (Receive Data B) ... Input
These pins input receive data.

(3) XI1A/$\overline{\text{STRxCA}}$ (Crystal Input 1A/Source of Transmit Receive Clock A) ... Input
XI1B/$\overline{\text{STRxCB}}$ (Crystal Input 1B/Source of Transmit Receive Clock B) ... Input
The functions of these pins change depending on the setting of CR15: D7.

(a) When CR15: D7 = "0"
These pins function as the $\overline{\text{STRxC}}$ pins, and input the transmission and reception clocks, or input source clocks to the internal BRG (Baud Rate Generator) and DPLL (Digital Phase Locked Loop).

(b) When CR15: D7 = "1"
These pins function as XI1 pins and connect one end of the crystal for transmission/reception clock source oscillation.

(4) XI2A/$\overline{\text{SYNCA}}$ (Crystal Input 2A/Synchronization A) ... I/O
XI2B/$\overline{\text{SYNCB}}$ (Crystal Input 2B/Synchronization B) ... I/O
The functions of these pins change depending on the setting of CR15: D7.

(a) When CR15: D7 = 0
These pins function as $\overline{\text{SYNC}}$ pins. The functions of the $\overline{\text{SYNC}}$ pins differ as shown in Table 1-6, depending on the setting of CR4.

(b) When CR15: D7 = "1"
These pins function as XI2 pins and connect one end of the crystal for transmission/reception clock source oscillation.

Table 1-6. Functions of $\overline{\text{SYNC}}$ Pins and Setting of CR4 (when CR15: D7 = "0")

Operation Protocol	Synchronization Detection Mode	$\overline{\text{SYNC}}$ Pin Function	CR4 D7	CR4 D6	CR4 D5	CR4 D4	CR4 D3	CR4 D2	Function
Start-stop synchro-nization		Input	×		×		0 1 1	1 0 1	The $\overline{\text{SYNC}}$ pins function as general-purpose input pins. Changes in the status of these pin ("H" → "L" or "L" → "H") affect the latch operation of the Sync/Hunt bit (SR1: D4), and cause the E/S interrupt.
COP	Internal synchro-nization	Output	×		0	0			If a SYNC character is detected in the receive character, the SYNC pins go "L" for the duration of 1RxC cycle.
					0	1			
	External synchro-nization	Input	0	0	1	1	0	0	The $\overline{\text{SYNC}}$ pins input a signal for establishing character synchronization. When these pins go "L" from "H", execution exits from the Hunt Phase and character synchronization is established. While $\overline{\text{SYNC}}$ input is "L", character synchronization is maintained. Assembling a receive character is started at the rising edge of the receive clock preceding the falling of the $\overline{\text{SYNC}}$ input.
			0	1					
BOP		No function	×		1	0			The $\overline{\text{SYNC}}$ pins do not function.

× : Don't Care

Caution If a pattern in which 1 bit ("0" or "1") is inserted in between the "Sync character assigned to CR7" and "Sync character assigned to CR6" is received while data is being assembled in the Bi-Sync mode, an "L" pulse of about 1 bit may be generated on the $\overline{\text{SYNC}}$ pin. If the Enter Hunt command is issued while this "L" pulse is present, the command is invalid. However, the recieve operation of the MPSC is not affected at all by the reception of this pattern.

(5) $\overline{\text{TRxCA}}$ (Transmit Receive Clock A) ... I/O
$\overline{\text{TRxCB}}$ (Transmit Receive Clock B) ... I/O

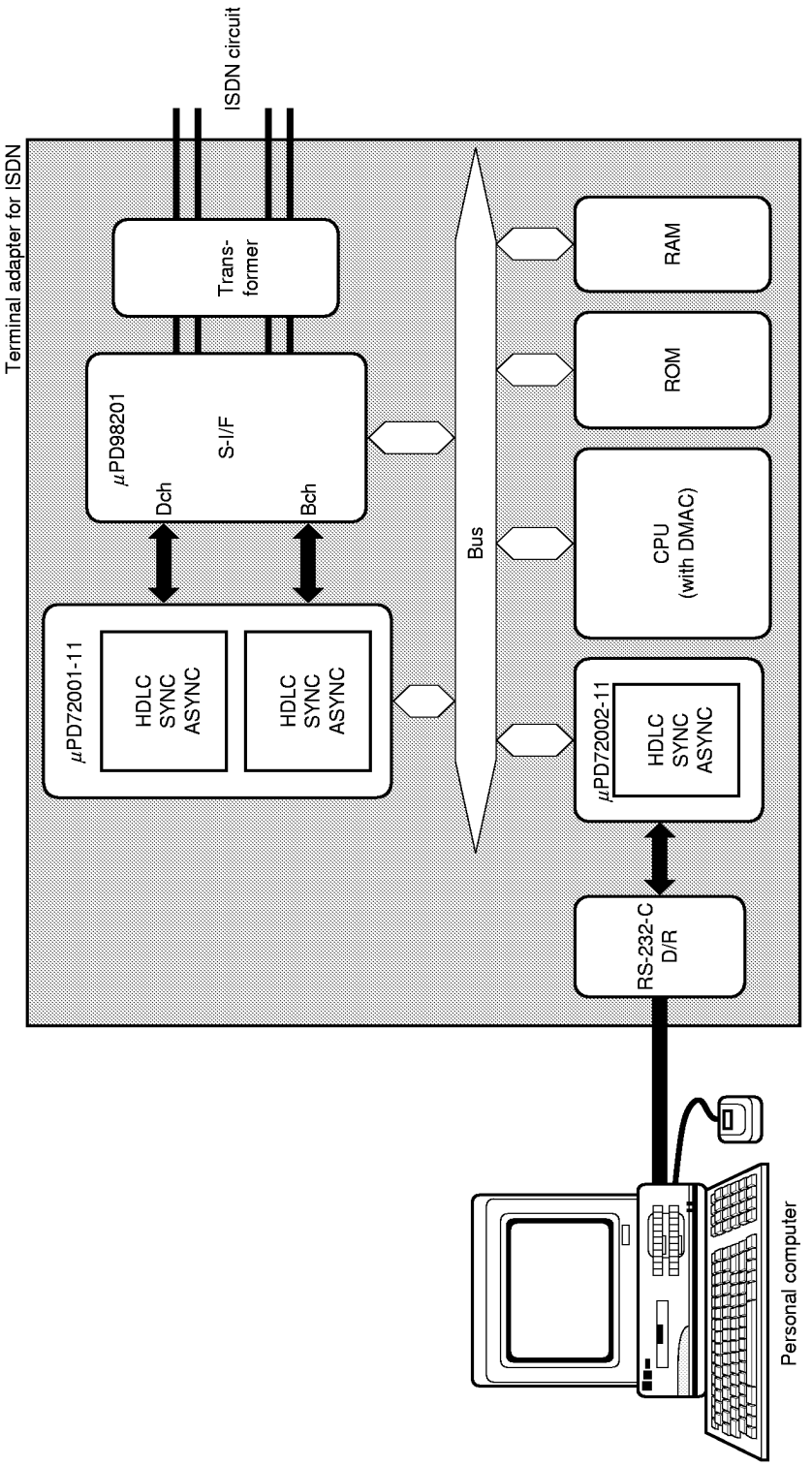
(a) When CR15: D2 = "0"
These pins input the transmit and receive clocks. They are used to supply external transmit and receive clocks.

[Exception] If either CR15: D6, D5 = "0, 1" or D4, D3 = "0, 1", or both are set, the $\overline{\text{TRxCA}}$ and $\overline{\text{TRxCB}}$ pins function as input pins, even if CR15: D2 = "1".

(b) When CR15: D2 = "1"
These pins function as output pins. The source of the output clock can be selected from a crystal oscillation circuit, BRG, DPLL, or transmit clock, depending on the setting of CR15: D1, D0. Under the conditions explained in [Exception] in (a) above, they unconditionally serve as input pins, and the setting of CR15: D2, D1, D0 is invalid.

2. SYSTEM CONFIGURATION EXAMPLE

An example of a system where the μPD72001-11 is used for a terminal adapter for ISDN is shown below.



3. ELECTRICAL SPECIFICATIONS

(1) μPD72001-11

Absolute Maximum Ratings (T_A = 25 °C)

Parameter	Symbol	Condition	Ratings	Unit
Supply voltage	V_{DD}		–0.5 to +7.0	V
Input voltage	V_I		–0.5 to V_{DD} + 0.5	V
Output voltage	V_O		–0.5 to V_{DD} + 0.5	V
Operating temperature	T_A		–40 to +85	°C
Storage temperature	T_{stg}		–65 to +150	°C

Caution If any of the parameters exceeds the absolute maximum ratings, even momentarily, the quality of the product may be impaired. The absolute maximum ratings are values that may physically damage the product(s). Be sure to use the product(s) within the ratings.

DC Characteristics

μPD72001-11 (T_A = –40 to +85 °C, V_{DD} = 5 V ± 10 %)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High-level input voltage	V_{IHC}	CLK, $\overline{STRxC}$, $\overline{TRxC}$	3.3		V_{DD} + 0.5	V
	V_{IH}	Other pins	2.2		V_{DD} + 0.5	V
Low-level input voltage	V_{ILC}	CLK, $\overline{STRxC}$, $\overline{TRxC}$	–0.5		+0.6	V
	V_{IL}	Other pins	–0.5		+0.8	V
High-level output voltage	V_{OH}	I_{OH} = –400 μA	0.7 V_{DD}			V
Low-level output voltage	V_{OL}	I_{OL} = 2.0 mA			0.45	V
High-level input leakage current	I_{LIH}	V_I = V_{DD}			10	μA
Low-level input leakage current	I_{LIL}	V_I = 0 V			–10	μA
High-level output leakage current	I_{LOH}	V_O = V_{DD}			10	μA
Low-level output leakage current	I_{LOL}	V_O = 0 V			–10	μA
Supply current	I_{DD}	At 11 MHz		20	40	mA
		In standby mode[Note]			1	mA

Note System clock : 11 MHz
Input pin : Inactive
- High-level input voltage : (V_{DD} – 0.3 V) to (V_{DD} + 0.5 V)
- Low-level input voltage : 0 V to 0.3 V

Output pin : Leave unconnected.

Capacitance (T_A = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input capacitance	C_{IN}	f_C = 1 MHz		10	pF
I/O capacitance	C_{IO}	Pins other than test pin: 0 V		20	pF

AC Characteristics

μPD72001-11 (T_A = –40 to +85 °C, V_{DD} = 5 V ± 10 %)

System interface:

Parameter	Symbol	Condition	Rated Value		Unit
			MIN.	MAX.	
Clock cycle	t_{CYK}		90	2 000	ns
Clock high-pulse width	t_{WKH}		40	1 000	ns
Clock low-pulse width	t_{WKL}		40	1 000	ns
Clock rise time	t_{KR}	1.5 V → 3.0 V		10	ns
Clock fall time	t_{KF}	3.0 V → 1.5 V		10	ns
Address setup time (vs. $\overline{RD}$ ↓)	t_{SAR}		0		ns
Address hold time (vs. $\overline{RD}$ ↑)	t_{HRA}		0		ns
$\overline{RD}$ pulse width	t_{WRL}		120		ns
Address → data output delay time	t_{DAD}	T_A = –10 to +70 °C		100	ns
		T_A = –40 to +85 °C		110	
$\overline{RD}$ → data output delay time	t_{DRD}	T_A = –10 to +70 °C		100	ns
		T_A = –40 to +85 °C		110	
$\overline{RD}$ → data float delay time	t_{FRD}		10	85	ns
Address setup time (vs. $\overline{WR}$ ↓)	t_{SAW}		0		ns
Address hold time (vs. $\overline{WR}$ ↑)	t_{HWA}		0		ns
$\overline{WR}$ pulse width	t_{WWL}		120		ns
Data setup time (vs. $\overline{WR}$ ↑)	t_{SDW}	T_A = –10 to +70 °C	100		ns
		T_A = –40 to +85 °C	90		
Data hold time (vs. $\overline{WR}$ ↑)	t_{HWA}		0		ns
Recovery time between $\overline{RD}$ and $\overline{WR}$	t_{RV}		140		ns

Serial control:

Parameter		Symbol	Condition	Rated Value MIN.	Rated Value MAX.	Unit
Transmit/receive data cycle		t_{CYD}		5		t_{CYK}
$\overline{STRxC}$, $\overline{TRxC}$ input clock cycle		t_{CYC}		90		ns
$\overline{STRxC}$, $\overline{TRxC}$ input clock pulse width	High	t_{WCH}		40		ns
	Low	t_{WCL}	T_A = −10 to +70 °C	40		ns
			T_A = −40 to +85 °C	45		
$\overline{STRxC}$, $\overline{TRxC}$ ↓ → TxD delay time		t_{DTCTD1}	×1 mode, COP, BOP		100	ns
		t_{DTCTD2}	×16, 32, 64 mode		300	ns
$\overline{TRxC}$ ↓ → TxD delay time		t_{DTCTD3}	$\overline{TRxC}$ is output	0	100	ns
RxD setup time (vs. $\overline{STRxC}$, $\overline{TRxC}$ ↑)		t_{SRDRC}	When DPLL is not used	0		ns
RxD hold time (vs. $\overline{STRxC}$, $\overline{TRxC}$ ↑)		t_{HRCRD}	When DPLL is not used	120		ns
RxD → TxD delay time		t_{DRDTD1}	ECHO BACK mode		100	ns
		t_{DRDTD2}	Without SDLC Loop delay		100	ns
TxD → $\overline{INT}$ delay time		t_{DTDIQ}	Tx INT mode	4	6	t_{CYK}
TxD → DRQTx delay time		t_{DTDDQ}	Tx DMA mode	4	6	t_{CYK}
$\overline{RxC}$ ↑ Note → $\overline{INT}$ delay time		t_{DRCIQ}	Rx INT mode	7	11	t_{CYK}
$\overline{RxC}$ ↑ Note → DRQRx delay time		t_{DRCDQ}	Rx DMA mode	7	11	t_{CYK}
$\overline{RD}$ ↓ → DRQRx ↓ delay time		t_{DRDQ}			120	ns
$\overline{WR}$ ↓ → DRQTx ↓ delay time		t_{DWDQ}			120	ns

Note Of $\overline{STRxC}$ and $\overline{TRxC}$, the one used as the receive clock.

Interrupt control:

Parameter	Symbol	Condition	Rated Value MIN.	Rated Value MAX.	Unit
$\overline{INTAK}$ low-pulse width	t_{WIAL}		120		ns
$\overline{INTAK}$ high-pulse width	t_{WIAH}		120		ns
$\overline{PRI}$ → $\overline{PRO}$ delay time	t_{DPIPO}			50	ns
$\overline{INT}$ ↓ → $\overline{PRO}$ ↑ delay time	t_{DIQPO}		−20	+50	ns
2nd $\overline{INTAK}$ ↓ → $\overline{INT}$ ↑ delay time	t_{DIAIQ}	$\overline{INT}$ output level = 0.8 V Note		120	ns
		$\overline{INT}$ output level = 2.2 V Note		300	ns
SR2B read $\overline{RD}$ ↓ → $\overline{INT}$ ↑delay time	t_{DRDIQ}	$\overline{INT}$ output level = 0.8 V Note		150	ns
		$\overline{INT}$ output level = 2.2 V Note		300	ns
$\overline{PRI}$ setup time (vs. $\overline{INTAK}$ ↓)	t_{SPIIA1}	When vector output is enabled	0		ns
$\overline{PRI}$ hold time (vs. $\overline{INTAK}$ ↑)	t_{HIAPI1}		20		ns
$\overline{PRI}$ setup time (vs. $\overline{INTAK}$ ↓)	t_{SPIIA2}	When vector output is disabled	20		ns
$\overline{PRI}$ hold time (vs. $\overline{INTAK}$ ↑)	t_{HIAPI2}		20		ns
$\overline{INTAK}$ → data output delay time	t_{DIAD}			120	ns
$\overline{INTAK}$ → data float delay time	t_{FIAD}		10	85	ns

Note Measured value with 2-kΩ pull-up resistor and 100-pF load capacitance connected

Modem control:

Parameter		Symbol	Condition	Rated Value MIN.	Rated Value MAX.	Unit
$\overline{CTS}$, $\overline{DCD}$, $\overline{SYNC}$ pulse width	High	t_{WMH}		2		t_{CYK}
	Low	t_{WML}		2		t_{CYK}
$\overline{CTS}$, $\overline{DCD}$, $\overline{SYNC}$ → $\overline{INT}$ delay time		t_{DMIQ}			2	t_{CYK}
$\overline{STRxC}$, $\overline{TRxC}$ ↑ → $\overline{SYNC}$ setup time		T_{SSYRC}	COP external synchronization	0	2	t_{CYK}

Communication control:

Parameter	Symbol	Condition	Rated Value MIN.	Rated Value MAX.	Unit
Transmit enable command ($\overline{WR}$ ↑, $\overline{CTS}$ ↓) → TxD delay time	t_{DTETD1}	ASYNC, COP		3	t_{CYC}
	t_{DTETD2}	BOP	4	7	t_{CYC}
Receive enable command ($\overline{DCD}$ ↓) setup time (vs. start bit, $\overline{STRxC}$ ↑, $\overline{TRxC}$ ↑ of sync character)[Note]	t_{SRERC}		1		t_{CYC}
Receive enable command ($\overline{DCD}$ ↓) hold time (vs. $\overline{STRxC}$ ↑, $\overline{TRxC}$ ↑)[Note]	t_{HRCRE1}	ASYNC	7		t_{CYK}
	t_{HRCRE2}	COP	$20t_{CYC}$ + $8t_{CYK}$		
	t_{HRCRE3}	BOP	$3t_{CYC}$ + $8t_{CYK}$		
Receive clock ($\overline{STRxC}$, $\overline{TRxC}$)[Note] hold time (vs. stop bit, MSB of CRC, MSB of end flag)	t_{HRDRC1}	ASYNC	1		Bit
	t_{HRDRC2}	COP	22		t_{CYC}
	t_{HRDRC3}	BOP	5		t_{CYC}
Receive clock ($\overline{STRxC}$, $\overline{TRxC}$)[Note] setup time (vs. start bit, sync character)	t_{SRCRD1}	ASYNC	1		Bit
	t_{SRCRD2}	COP, BOP	1		t_{CYC}

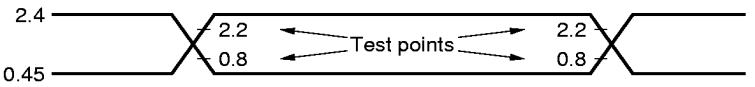
Note Of $\overline{STRxC}$ and $\overline{TRxC}$, the one used as the receive clock.

Crystal oscillation and reset

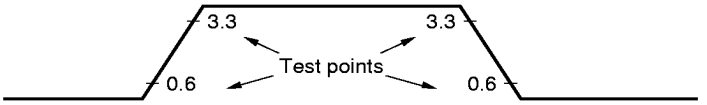
Parameter	Symbol	Condition	Rated Value MIN.	Rated Value MAX.	Unit
XI1 input cycle time	t_{CYX}		90	2000	ns
$\overline{RESET}$ pulse width	t_{WRSL}		2		t_{CYK}

Caution The system clock cycle in all modes must be five times that of the data rate.

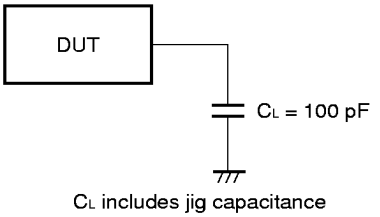
AC Test Input/Output Waveform (except clock)



AC Test Clock Input Waveform



Load Condition



CL includes jig capacitance

Caution If the load capacitance exceeds 100 pF due to the configuration of the circuit, keep the load capacitance of this device to within 100 pF by inserting a buffer or by some other means.

Remark DUT: Tested device

(2) μPD72001-A8

Absolute Maximum Ratings (T_A = 25 °C)

Parameter	Symbol	Condition	Ratings	Unit
Supply voltage	V_{DD}		–0.5 to +7.0	V
Input voltage	V_I		–0.5 to V_{DD} + 0.5	V
Output voltage	V_O		–0.5 to V_{DD} + 0.5	V
★ Operating temperature	T_A		–40 to +85	°C
Storage temperature	T_{stg}		–0 to +150	°C

Caution If any of the parameters exceeds the absolute maximum ratings, even momentarily, the quality of the product may be impaired. The absolute maximum ratings are values that may physically damage the product(s). Be sure to use the product(s) within the ratings.

DC Characteristics (T_A = –40 to +85 °C, V_{DD} = 3.3 V ± 0.3 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High-level input voltage	V_{IHC}	CLK, $\overline{STRxC}$, $\overline{TRxC}$	0.8 V_{DD}		V_{DD} + 0.5	V
	V_{IH}	Other pins	1.8		V_{DD} + 0.5	V
Low-level input voltage	V_{ILC}	CLK, $\overline{STRxC}$, $\overline{TRxC}$	–0.5		0.15 V_{DD}	V
	V_{IL}	Other pins	–0.5		+0.6	V
High-level output voltage	V_{OH}	I_{OH} = –400 μA	2.2			V
Low-level output voltage	V_{OL}	I_{OL} = 2.0 mA			0.5	V
High-level input leakage current	I_{LIH}	V_I = V_{DD}			10	μA
Low-level input leakage current	I_{LIL}	V_I = 0 V			–10	μA
High-level output leakage current	I_{LOH}	V_O = V_{DD}			10	μA
Low-level output leakage current	I_{LOL}	V_O = 0 V			–10	μA
Supply current	I_{DD}	At 8 MHz		5	20	mA
		In standby mode[Note]			1	mA

Note System clock : 8 MHz (T_A = –10 to +70 °C)/7.14 MHz (T_A = –40 to +85 °C)
Input pin : Inactive
- High-level input voltage : (V_{DD} – 0.3 V) to (V_{DD} + 0.5 V)
- Low-level input voltage : 0 V to 0.3 V

Output pin : Leave unconnected.

Capacitance (T_A = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input capacitance	C_{IN}	f_C = 1 MHz		10	pF
I/O capacitance	C_{IO}	Pins other than test pin: 0 V		20	pF