Supertex inc.

P-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
			TO-39	TO-92
-160V	100Ω	-100mA	VP1316N2	VP1316N3
-200V	100Ω	-100mA	VP1320N2	VP1320N3

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

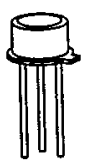
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Motor control
- ☐ Convertors
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options (Note 1)



TO-39

TO-92

Note 1: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

T-37-25

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}	I_{DRM}*
TO-39	-0.10A	-0.40A	3.0W	125	41	-0.1A	-0.4A
TO-92	-0.06A	-0.30A	0.8W	170	155	-0.06A	-0.3A

* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

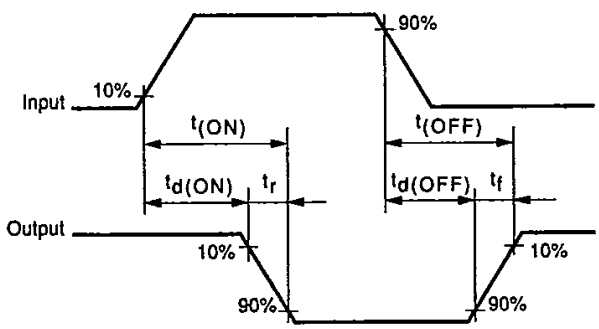
(Notes 1 and 2)

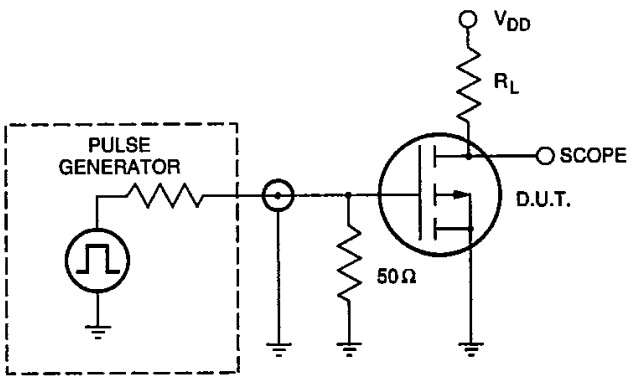
Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VP1320	-200			V	I_D = -1mA, V_{GS} = 0
		VP1316	-160				
$V_{GS(th)}$	Gate Threshold Voltage		-1.5		-3.5	V	V_{GS} = V_{DS}, I_D = -1mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-4.0	-5.0	mV/°C	V_{GS} = V_{DS}, I_D = -1mA
I_{GSS}	Gate Body Leakage			0.1	100	nA	V_{GS} = ±20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				-10	µA	V_{GS} = 0, V_{DS} = Max Rating
					-500		V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		-50	-100		mA	V_{GS} = -5V, V_{DS} = -25V
			-100	-400		mA	V_{GS} = -10V, V_{DS} = -25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			65	100	Ω	V_{GS} = -5V, I_D = -40mA
				60	100	Ω	V_{GS} = -10V, I_D = -150mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.6	1.0	%/°C	I_D = -50mA, V_{GS} = -10V
G_{FS}	Forward Transconductance		20	30		m℧	V_{DS} = -25V, I_D = -150A
C_{ISS}	Input Capacitance			35	40	pF	V_{GS} = 0, V_{DS} = -25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			10	15		
C_{RSS}	Reverse Transfer Capacitance			2	5		
$t_{d(ON)}$	Turn-ON Delay Time			1.5	5	ns	V_{DD} = -25V, I_D = -200mA, R_S = 50Ω
t_r	Rise Time			2.5	5		
$t_{d(OFF)}$	Turn-OFF Delay Time			1.5	5		
t_f	Fall Time			2.5	5		
V_{SD}	Diode Forward Voltage Drop			1.6	2.0	V	I_{SD} = -1A, V_{GS} = 0
t_{rr}	Reverse Recovery Time			350		ns	I_{SD} = -1A, V_{GS} = 0

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

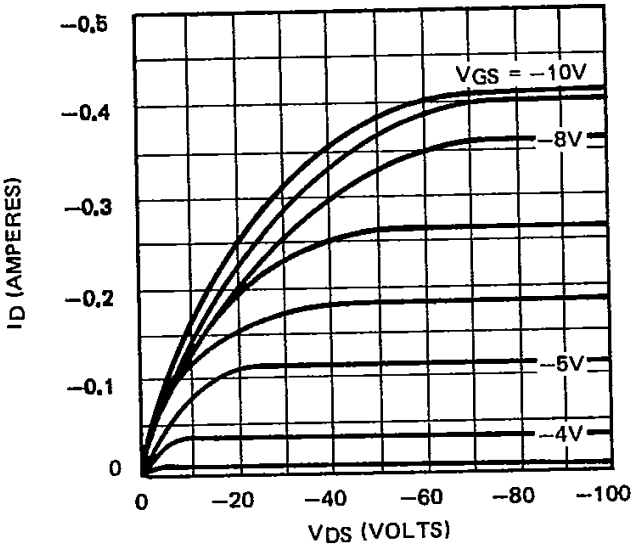




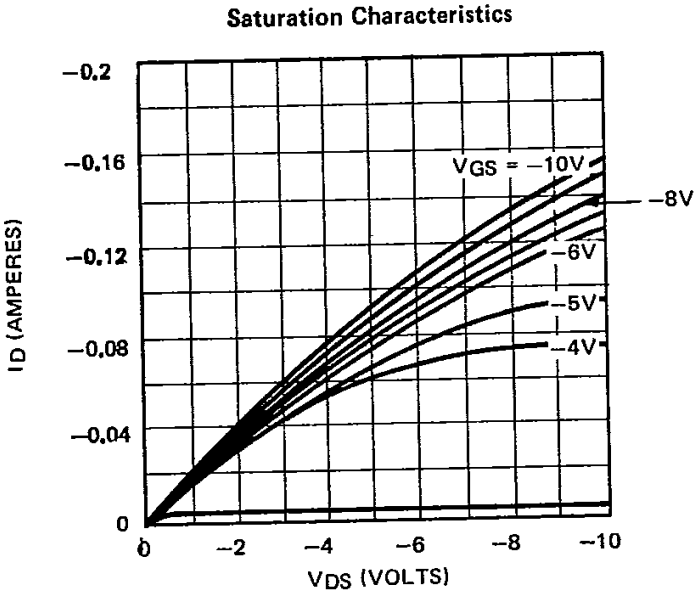
Typical Performance Curves

T-37-25

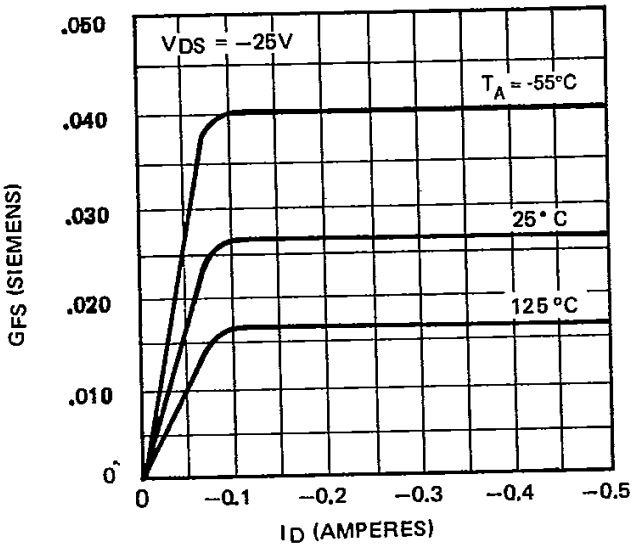
Output Characteristics



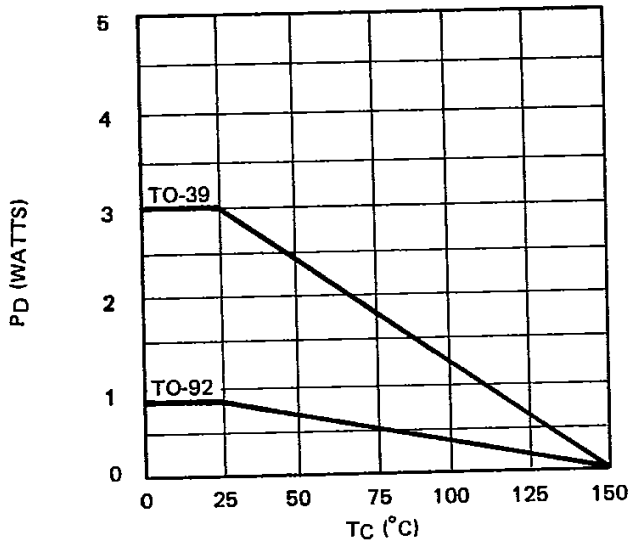
Saturation Characteristics



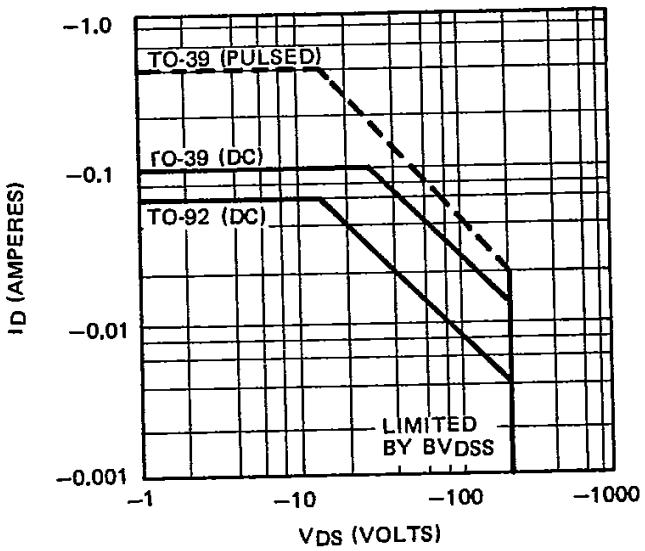
Transconductance Vs. Drain Current



Power Dissipation Vs. Case Temperature

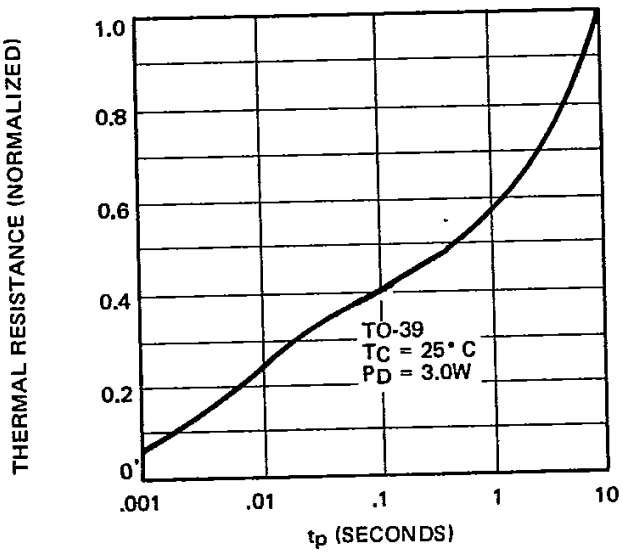


Maximum Rated Safe Operating Area

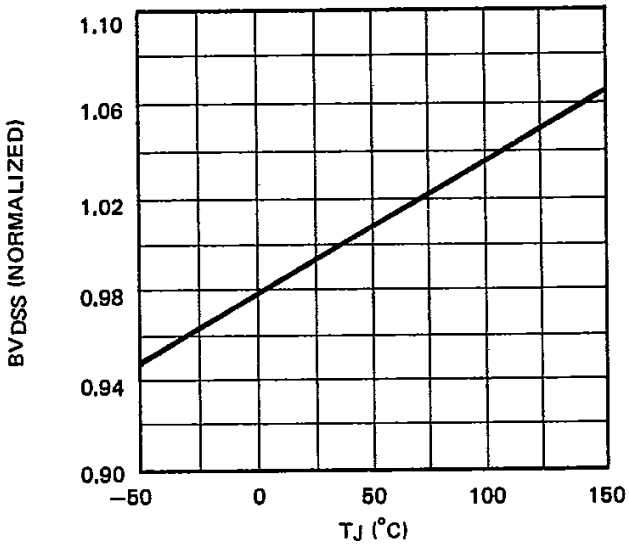


Pulse Condition: 300 μs ,2% dutycycle.

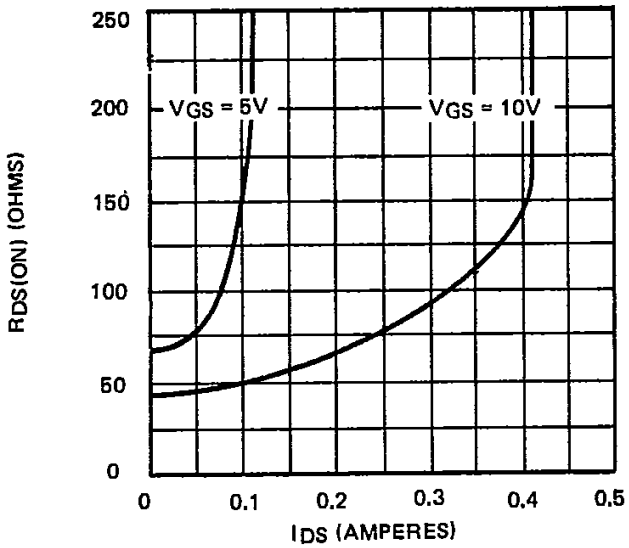
Thermal Response Characteristics



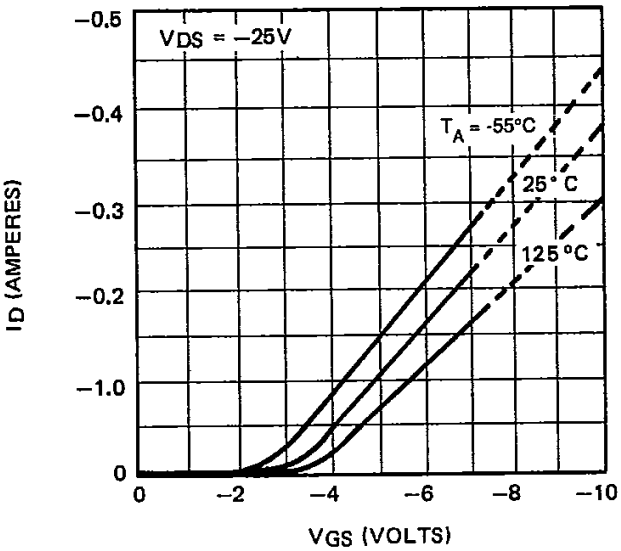
BVDSS Variation with Temperature



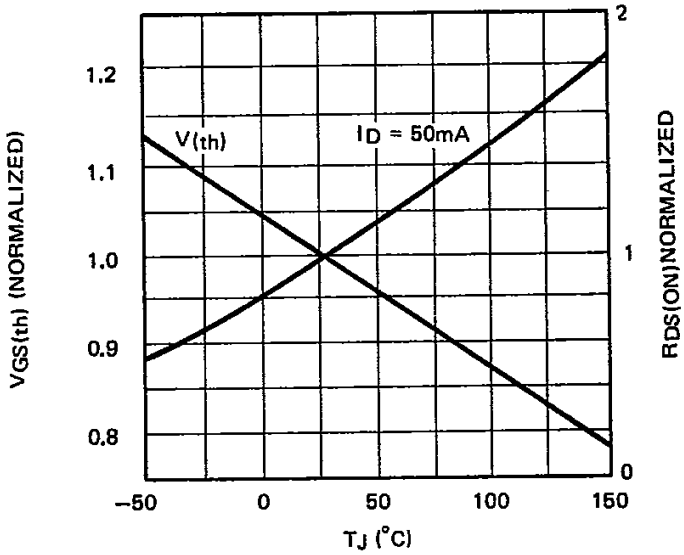
ON- Resistance Vs .Drain Current



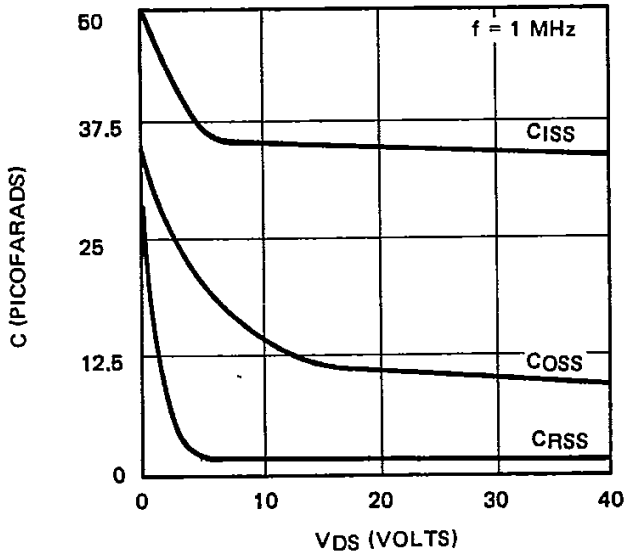
Transfer Characteristics



V(th) and RDS Variation with Temperature



Capacitance Vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics