



Binary to 1-8 Decoder (High)

ELECTRICALLY TESTED PER: MPG 10H562

The 10H562 provides parallel decoding of a three bit binary word to one of eight lines. The 10H562 is useful in high-speed multiplexer/demultiplexer applications.

The 10H562 is designed to decode a three bit input word to one of eight output lines. The 10H562 output will be low when selected while all other outputs are low. The enable inputs, when either or both are high, force all outputs low.

The 10H562 is a true parallel decoder. This eliminates unequal parallel path delay times found in other decoder designs. These devices are ideally suited for multiplexer/demultiplexer applications.

- Propagation Delay, 1.5 ns Typical
- 460 mW Max/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

PIN ASSIGNMENTS				
FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V _{CC1}	1	5	2	GND
$\overline{E}_0$	2	6	3	OPEN
Q ₃	3	7	4	V _{TT}
Q ₂	4	8	5	V _{TT}
Q ₁	5	9	7	V _{TT}
Q ₀	6	10	8	V _{TT}
A	7	11	9	GND
V _{EE}	8	12	10	V _{EE}
B	9	13	12	OPEN
Q ₇	10	14	13	V _{TT}
Q ₆	11	15	14	V _{TT}
Q ₅	12	16	15	V _{TT}
Q ₄	13	1	17	V _{TT}
C	14	2	18	OPEN
$\overline{E}_1$	15	3	19	OPEN
V _{CC2}	16	4	20	GND

BURN - IN CONDITIONS:

V_{TT} = - 2.0 V MAX/ - 2.2 V MIN

V_{EE} = - 5.7 V MAX/ - 5.2 V MIN

Military 10H562

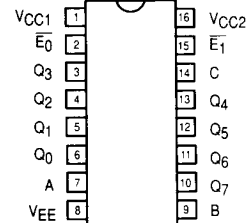


AVAILABLE AS

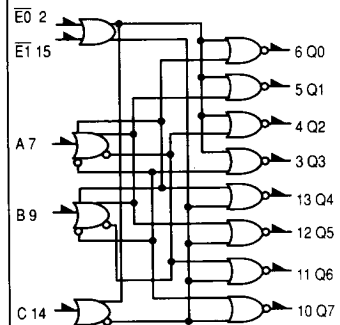
- 1) JAN: N/A
 - 2) SMD: N/A
 - 3) 883: 10H562/BXAJC
- X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before
the slash on LCC.



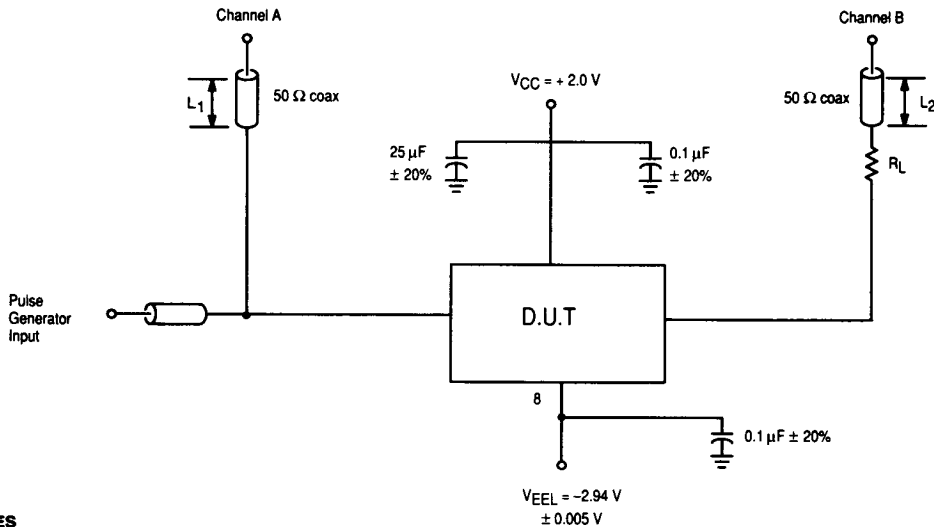
POSITIVE LOGIC DIAGRAM



10H562
TRUTH TABLE

Enable Inputs		Inputs			Outputs							
$\overline{E}_1$	$\overline{E}_0$	C	B	A	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	L	L	H	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	L	H	H	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H
H	Ø	Ø	Ø	Ø	L	L	L	L	L	L	L	L
Ø	H	Ø	Ø	Ø	L	L	L	L	L	L	L	L

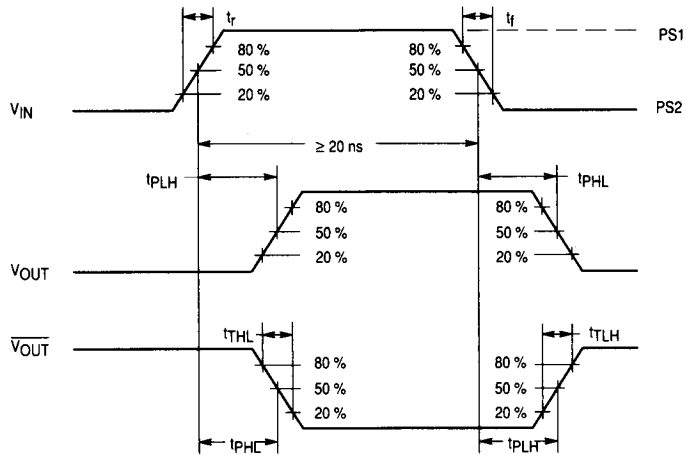
Ø = Don't Care



NOTES

1. All other outputs loaded 100 Ω to ground.
2. 2:1 divider may be used.
3. L₁ = L₂: Matched for equal time delay.
4. R_L = 50 Ω.

Figure 1. Switching Test Circuit

**NOTES**

V_{IN} has the following characteristics:

1. $P_W = 20$ ns.
2. $f_{IN} = 1.0$ MHz.
3. $t_r = t_f = 1.0$ ns ± 0.1 ns (20% - 80%).

Figure 2. Switching Test Circuit Waveforms

10H562 QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear is maintained. Outputs are terminated through a 100 Ω resistor to -2.0 volts.

Test Temperature	Test Voltage Values (Volts)									
	V _{IH}	V _{IL}	V _{IH1}	V _{IL1}	PS ₁	PS ₂	VEE ₁	VEE ₂	VEEL	
T _A = 25 °C	-0.780	-1.95	-1.10	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94	
T _A = 125 °C	-0.735	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94	
T _A = -55 °C	-0.840	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94	

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW									
		+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments VCC = 0 V, Output Load = 100 Ω to - 2.0 V									
		Subgroup 1		Subgroup 2		Subgroup 3												
		Min	Max	Min	Max	Min	Max		V _{IH}	V _{IL}	V _{IH1}	V _{IL1}	VEE2	VEE1	V _{CC}	P.U.T.		
V _{OH}	High Output Voltage	-1.01	-0.78	-0.86	-0.65	-1.06	-0.84	V	7, 9, 14					8	1, 16	3 - 6, 10 - 13		
V _{OL}	Low Output Voltage	-1.95	-1.58	-1.95	-1.363	-1.95	-1.61	V	2, 15					8	1, 16	3 - 6, 10 - 13		
V _{OH1}	High Output Voltage	-1.01	-0.78	-0.86	-0.65	-1.06	-0.84	V	7, 9, 14		2, 7, 9 14, 15	7, 9 14, 15	8	8	1, 16	3 - 6, 10 - 13		
V _{OL1}	Low Output Voltage	-1.95	-1.58	-1.95	-1.363	-1.95	-1.61	V	7, 9, 14		7, 9, 14	2, 7, 9 14, 15	8	8	1, 16	3 - 6, 10 - 13		
I _{EE}	Power Supply Current	-76		-84		-84		mA						8	1, 16	8		
I _{IH}	Input Current High		275		465		465	μA	2, 7, 9 14, 15					8	1, 16	2, 7, 9, 14, 15		
I _{IL}	Input Current Low	0.5		0.3		0.5		μA		2, 7, 9 14, 15			8		1, 16	2, 7, 9, 14, 15		

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Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments VCC = 2.0 V, Output Load = 100 Ω to GND							
		Subgroup 9		Subgroup 10		Subgroup 11										
		Min	Max	Min	Max	Min	Max									
t _{TLH}	Rise Time	0.6	1.9	0.6	2.0	0.6	1.8	ns	7, 9 14, 15	2, 7, 9, 14	3 - 6, 10 - 13	1, 16	8	7, 9 14, 15	3 - 6, 10 - 13	
t _{THL}	Fall Time	0.6	1.9	0.6	2.0	0.6	1.8	ns	7, 9 14, 15	2, 7, 9, 14	3 - 6, 10 - 13	1, 16	8	7, 9 14, 15	3 - 6, 10 - 13	
t _{PLH}	Propagation Delay	0.7	2.4	0.8	2.7	0.7	2.3	ns	7, 9 14, 15	2, 7, 9, 14	3 - 6, 10 - 13	1, 16	8	7, 9 14, 15	3 - 6, 10 - 13	
t _{PHL}	Propagation Delay	0.7	2.4	0.8	2.7	0.7	2.3	ns	7, 9 14, 15	2, 7, 9, 14	3 - 6, 10 - 13	1, 16	8	7, 9 14, 15	3 - 6, 10 - 13	