10/100BASE Dual Speed 8-Port Repeater with 4-Port Switch

Document No.: AX872-13 / V1.3 / Aug. 11 '99

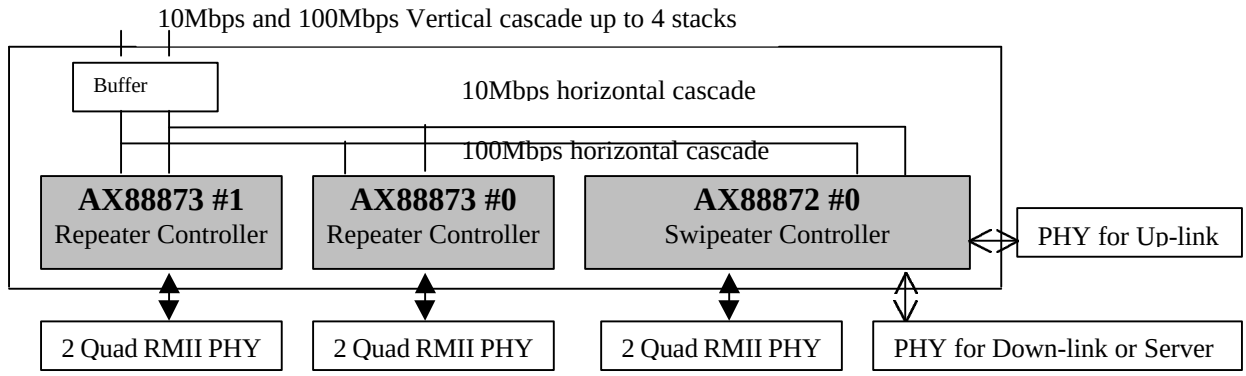
Features

- Support 8 10/100Mbps RMII I/F repeater ports and 2 10/100Mbps RMII/MII switch ports
- IEEE 802.3u repeater compatible
- Support virtual switch mode and Master/Slave mode for the cascade application
- Build in 4-ports 10/100Mbps Switch engine with following features
  - ✓ Low cost SSRAM interface to reduce system cost
  - ✓ One or two 64K*32bit SSRAM to buffer packets
  - ✓ 4/8 K MAC Address Entry Table is supported
  - ✓ Auto learning and filtering
  - ✓ Aging the MAC Address table is supported optionally
  - ✓ Three forwarding modes are supported : Store-and-Forward, Fragment-Free and Auto-Forward
  - ✓ Flow-control is supported optionally.
  - ✓ 802.3x flow control is supported in full duplex mode
  - ✓ Back-pressure base flow control is supported in half duplex mode
  - ✓ Ext. Buffer Memory auto testing
  - ✓ Routing and Learning at wire speed (148800 packets/sec at 100Mbps)
- Up-to 4 repeaters can be cascaded for vertical expansion
- Up-to 3 chips can be cascaded locally for horizontal expansion
- All ports can be separately isolated or partitioned in response to fault condition
- Separate jabber and partition state machines for each port
- Per-port LED display for Jabber, Partition, Activity. RAM test fail and collision, buffer utilization (%) and global traffic utilization (%) for 10/100Mbps presentation
- Power on LED diagnosis. All the LED display will follow the "ON-OFF-ON-OFF-Normal" operation procedure during/after power on reset
- 50MHz Operation, 3.3volt and 208-pin PQFP

Product description

The AX88872 10/100Mbps Dual Speed "**Swipeater"** Controller is **"a dual speed repeater with build in 4-ports switch function"** It is design for low cost dumb HUB application. The AX88872 directly supports up-to eight 10/100Mbps automatic links RMII interfaces. Maximum up-to 96 repeater ports can be constructed by stacking 1 AX88872 and 2 AX88873 chips horizontally and then cascading 4 horizontal boards vertically. About the build in 4-port switch: The switch port3 is fixed to 10Mbps speed and connects to 10Mbps repeater segment, The switch port2 is fixed to 100Mbps and connects to 100M repeater segment. The switch ports 0 and 1 are connected to external MII or RMII interfaces for various applications. For example, one port is used for down link and the other is used for up link to extend the network topology. The other case is one port for up link and the other port for server. The AX88872 is designed base on IEEE 802.3u clause 27 " Repeater for 100Mb/s base-band networks" It is fully compatible with IEEE 802.3u standard. Please refer Ax873-12.doc to get more information about AX88873.

System Block Diagram



Always contact ASIX for possible updates before starting a design.

ASIX ELECTRONICS CORPORATION **First Released Date : APR/09/1999**
2F, NO.13, Industry East Rd. II, Science-based Industrial Park, Hsin-Chu City, Taiwan, R.O.C.
TEL: 886-3-579-9500 **FAX: 886-3-579-9558** **http://www.asix.com.tw**

CONTENTS

FIGURES

1.0 AX88872 Overview

1.1 General Description

The AX88872 that built in a switch is not only a simple repeater but also it provide 2 repeater expansion buses for 10M and 100M respectively. So the cascade function of the AX88872 can be backward compatible with the AX88871A "Bripeater" in virtual switch mode. Also the AX88872 can support Master/Slave mode in stack application. That all the repeater stack system forms one 100Mbps segment and one 10Mbps segment in Master/Slave mode. The two segments are communication via the switch of the master chip.

In general, using RMII interface for 8 repeater ports can simplify the design and also provide a low cost solution with RMII Quad/Octet PHY and low cost 64Kx32 SSRAM as buffer memory. In additional, the AX88872 provides two 10/100M MII/RMII switch ports alternative for up-link and down-link function. AX88872 has counterpart AX88873 that is a simple dual-speed repeater controller without built-in switch.

The switch port3 is fixed to 10Mbps speed and connect to 10Mbps repeater segment, The switch port2 is fixed to 100Mbps and connect to 100M repeater segment. The other switch ports 0 and 1 are connected to external MII or RMII interfaces for various applications.

The built-in switch provides 4/8K look-up table that can learn, route and age with MAC address of each packet automatically for packet forwarding and filtering. That is, the AX88872 forwards and filters packets with DA (Destination Address) and the table. The performances of routing and learning fit wire speed (148800 packets/sec at 100Mbps). The switch provides three packet forwarding mode: Store-and-Forward, Fragment-Free (i.e., safe cut-through) and auto mode. Dynamically the switch selects optimum mode for packet forwarding based on network quality.

During transmission, the data is obtained from the buffer memory and routed to the destination port. For half-duplex operation, when collision occurs, the MAC controller will back off and retransmit in accordance to the IEEE802.3 specification. The switch also support flow-control mechanism. For full duplex operation mode, 802.3x flow control is supported. For half-duplex operation, an optional jamming based flow control is available to avoid loss of data. This is also well known as back-pressure. The flow control function is optional.

1.2 AX88872 Block Diagram:

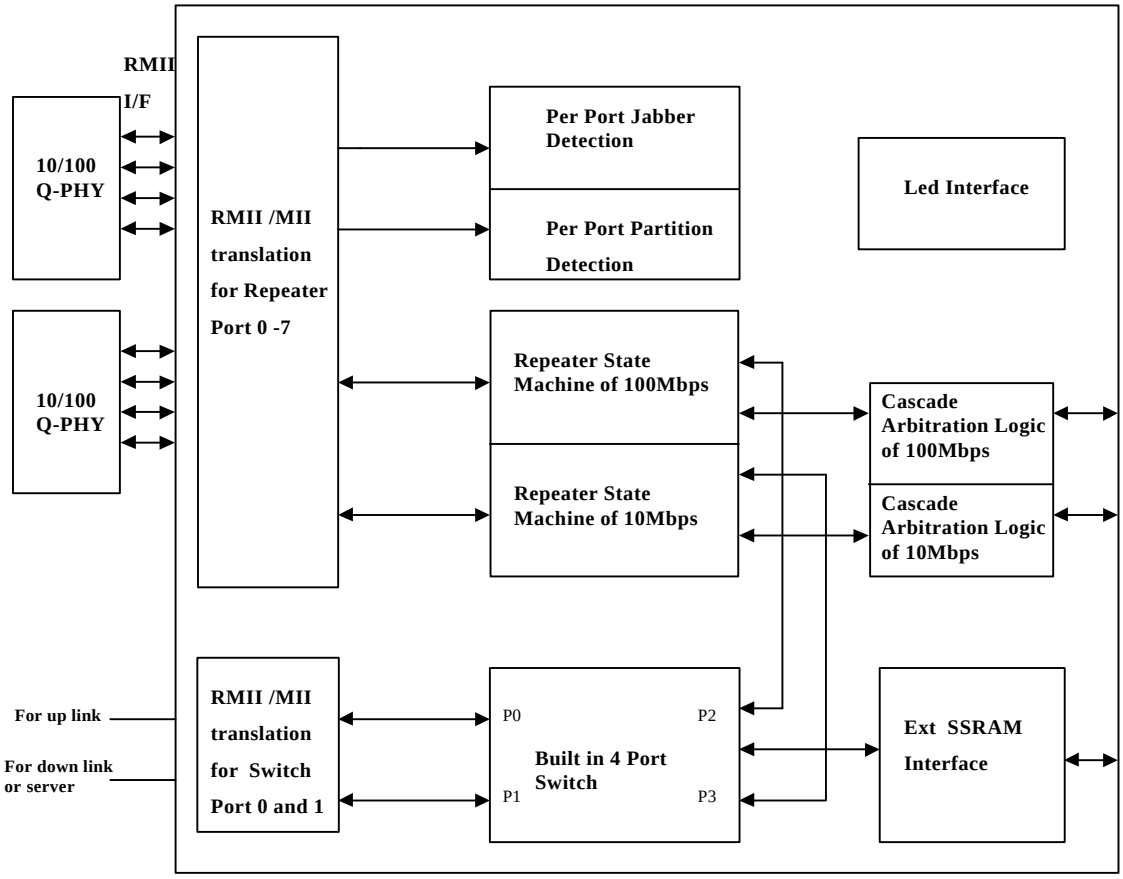


Fig - 1 AX88872 Block Diagram

1.3 Pin Connection Diagram

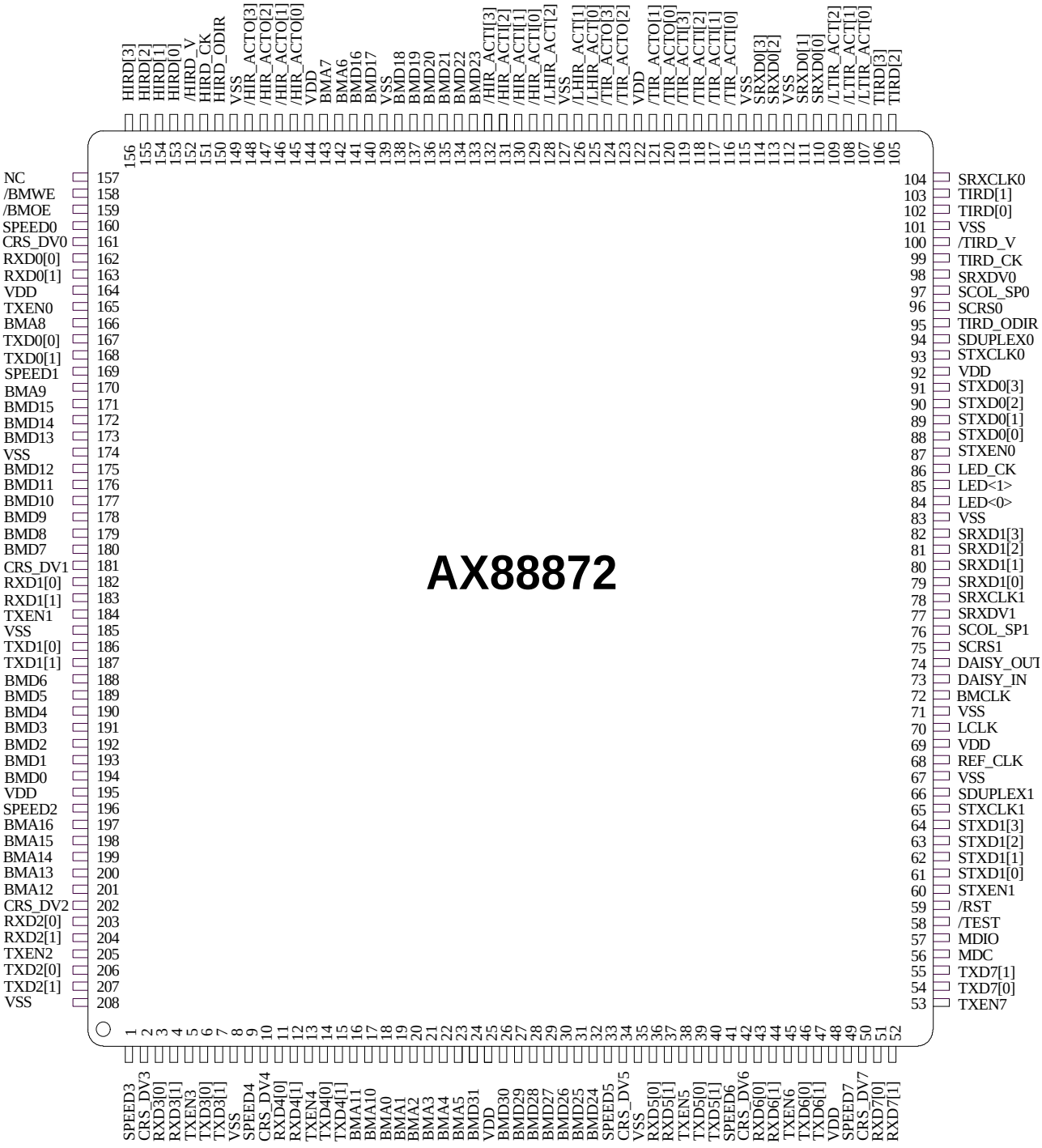


Fig - 2 Pin Connection Diagram

2.0 Pin Description

The following terms describe the AX88872 pin out:

All pin names with the "/" suffix are asserted low.

I	=	Input
O	=	Output
I/O	=	Input /Output

2.1 RMII interface for repeater ports

2.1.1 Repeater Port 0

Signal Name	Type	Pin No.	Description
SPEED0	I	160	**Speed Select :** SPEED0 is not standard RMII signal. This signal is source from PHY to inform repeater whether 10M or 100M speed is auto-negotiated. Active for 10Mbps speed is selected depending on power on configuration.
CRS_DV0	I	161	**Carrier Sense/Receive Data Valid :** CRS_DV is asserted asynchronously on detection of carrier. CRS_DV is asserted by the PHY when receive medium is non-idle. Loss of carrier shall result in the desertion of CRS_DV synchronous to the cycle of REF_CLK that presents the first DI-bits of a nibble on to RXD0[1:0].
RXD0[1:0]	I	163, 162	**Receive Data :** RXD0[1:0] is synchronous to REF_CLK RXD0[1:0] shall be "00" to indicate idle when CRS_DV is disserted. Value other than "00" are reserved for out-of-band signaling shall be ignored by MAC Upon assertion of CRS_DV, PHY shall ensure that RXD[1:0] = "00" until proper receive decoding takes place
TXEN0	O	165	**Transmit Enable :** TXEN0 is synchronous to REF_CLK. TXEN0 indicates that MAC is presenting DI-bits on TXD[1:0] for transmission. TXEN0 shall be negated prior to the 1st REF_CLK rising edge following the final DI-bit of a frame
TXD0[1:0]	O	168, 167	**Transmit Data :** TXD0[1:0] shall transition synchronously to REF_CLK. TXD0[1:0] shall be "00" to indicate idle when TX_EN is disserted. Value other than "00" are reserved for out-of-band signaling shall be ignored by PHY. When TX_EN is asserted, TXD[1:0] are accepted for transmission by PHY

2.1.2 Repeater Port 1

Signal Name	Type	Pin No.	Description
SPEED1	I	169	**Speed Select :** Please references section 2.1.1 PORT0 description.
CRS_DV1	I	181	**Carrier Sense/Receive Data Valid :** Please references section 2.1.1 PORT0 description.
RXD1[1:0]	I	183, 182	**Receive Data :** Please references section 2.1.1 PORT0 description.
TXEN1	O	184	**Transmit Enable :** Please references section 2.1.1 PORT0 description.
TXD1[1:0]	O	187, 186	**Transmit Data :** Please references section 2.1.1 PORT0 description.

2.1.3 Repeater Port 2

Signal Name	Type	Pin No.	Description
SPEED2	I	196	**Speed Select :** Please references section 2.1.1 PORT0 description.
CRS_DV2	I	202	**Carrier Sense/Receive Data Valid :** Please references section 2.1.1 PORT0 description.
RXD2[1:0]	I	204, 203	Receive Data : Please references section 2.1.1 PORT0 description.
TXEN2	O	205	**Transmit Enable :** Please references section 2.1.1 PORT0 description.
TXD2[1:0]	O	207,206	**Transmit Data :** Please references section 2.1.1 PORT0 description.

2.1.4 Repeater Port 3

Signal Name	Type	Pin No.	Description
SPEED3	I	1	**Speed Select :** Please references section 2.1.1 PORT0 description.
CRS_DV3	I	2	**Carrier Sense/Receive Data Valid :** Please references section 2.1.1 PORT0 description.
RXD3[1:0]	I	4, 3	**Receive Data :** Please references section 2.1.1 PORT0 description.
TXEN3	O	5	**Transmit Enable :** Please references section 2.1.1 PORT0 description.
TXD3[1:0]	O	7, 6	**Transmit Data :** Please references section 2.1.1 PORT0 description.

2.1.5 Repeater Port 4

Signal Name	Type	Pin No.	Description
SPEED4	I	9	**Speed Select :** Please references section 2.1.1 PORT0 description.
CRS_DV4	I	10	**Carrier Sense/Receive Data Valid :** Please references section 2.1.1 PORT0 description.
RXD4[1:0]	I	12, 11	**Receive Data :** Please references section 2.1.1 PORT0 description.
TXEN4	O	13	**Transmit Enable :** Please references section 2.1.1PORT0 description.
TXD4[1:0]	O	15, 14	**Transmit Data** : Please references section 2.1.1 PORT0 description.

2.1.6 Repeater Port 5

Signal Name	Type	Pin No.	Description
SPEED5	I	33	**Speed Select :** Please references section 2.1.1 PORT0 description.
CRS_DV5	I	34	**Carrier Sense/Receive Data Valid :** Please references section 2.1.1 PORT0 description.
RXD5[1:0]	I	37,36	**Receive Data :** Please references section 2.1.1 PORT0 description.
TXEN5	O	38	**Transmit Enable :** Please references section 2.1.1 PORT0 description.
TXD5[1:0]	O	40,39	**Transmit Data :** Please references section 2.1.1 PORT0 description.

2.1.7 Repeater Port 6

Signal Name	Type	Pin No.	Description
SPEED6	I	41	**Speed Select :** Please references section 2.1.1 PORT0 description.
CRS_DV6	I	42	**Carrier Sense/Receive Data Valid :** Please references section 2.1.1 PORT0 description.
RXD6[1:0]	I	44,43	**Receive Data :** Please references section 2.1.1 PORT0 description.
TXEN6	O	45	**Transmit Enable :** Please references section 2.1.1 PORT0 description.
TXD6[1:0]	O	47,46	**Transmit Data :** Please references section 2.1.1 PORT0 description.

2.1.8 Repeater Port 7

Signal Name	Type	Pin No.	Description
SPEED7	I	49	**Speed Select :** Please references section 2.1.1 PORT0 description.
CRS_DV7	I	50	**Carrier Sense/Receive Data Valid :** Please references section 2.1.1 PORT0 description.
RXD7[1:0]	I	52,51	**Receive Data :** Please references section 2.1.1 PORT0 description.
TXEN7	O	53	**Transmit Enable :** Please references section 2.1.1 PORT0 description.
TXD7[1:0]	O	55,54	**Transmit Data :** Please references section 2.1.1 PORT0 description.

2.2 MII/RMII interface for switch ports

2.2.1 Switch Port 0

Signal Name	Type	Pin No.	Description
STXEN0	O	87	**Transmit Enable :** STXEN0 is transition synchronously with respect to the rising edge of STXCLK0. STXEN0 indicates that the port is presenting nibbles on STXD0[3:0] for transmission. When RMII mode, TXEN is transition synchronously with respect to the rising edge of REF_CLK. STXEN0 indicates that the port is presenting nibbles on STXD0[1:0] for transmission.
STXD0[3:0]	O	91,90,89,88	**Transmit Data :** STXD0[3:0] is transition synchronously with respect to the rising edge of STXCLK0. For each STXCLK period in which STXEN is asserted, TXD[3:0] are accepted for transmission by the PHY. When RMII mode, STXD0[1:0] shall transition synchronously to REF_CLK. TXD0[1:0] shall be “00” to indicate idle when TX_EN is disserted. Value other than “00” are reserved for out-of-band signaling shall be ignored by PHY. When TX_EN is asserted, TXD[1:0] are accepted for transmission by PHY
STXCLK0	I	93	**Transmit Clock :** STXCLK0 is a continuous clock that provides the timing reference for the transfer of the STXEN0 and STXD0[3:0] signals from the MII port the switch to the PHY.
SDUPLEX0	I	94	**Duplex Select :** DUPLEX0 is not standard MII/RMII signal. This signal is source from PHY to inform switch whether 10M or 100M speed is auto-negotiated.
SCOL_SP0	I	97	**Collision :** SCOL_SP0 is input from PHY, when collision is detected.

			When RMII mode, the signal is stand for speed indicator. Active for 10Mbps speed is selected depending on power on configuration.
SCRS0 or SCRS_DV	I	96	**Carrier Sense :** Asynchronous signal SCRS0 is asserted by the PHY when receive medium is non-idle. When RMII mode, the signal is stand for CRS_DV (Carrier Sense/Receive Data Valid). CRS_DV is asserted asynchronously on detection of carrier. CRS_DV is asserted by the PHY when receive medium is non-idle. Loss of carrier shall result in the desertion of CRS_DV synchronous to the cycle of REF_CLK, which presents the first DI-bit of a nibble on to RXD0[1:0].
SRXDV0	I	98	**Receive Data Valid :** SRXDV0 is driven by the PHY synchronously with respect to SRXCLK0. Asserted high when valid data is present on SRXD0[3:0].
SRXCLK0	I	104	**Receive Clock :** SRXCLK0 is a continuous clock that provides the timing reference for the transfer of the SRXDV0 and SRXD0[3:0] signals from the PHY to the MII port of the repeater.
SRXD0[3:0]	I	114,113, 111,110	**Receive Data :** SRXD0[3:0] is driven by the PHY synchronously with respect to RXCLK. When RMII mode, SRXD0[1:0] shall transition synchronously to REF_CLK SRXD0[1:0] shall be “00” to indicate idle when CRS_DV is disserted. Value other than “00” are reserved for out-of-band signaling shall be ignored by MAC Upon assertion of CRS_DV, PHY shall ensure that RXD[1:0] = “00” until proper receive decoding takes place

2.2.2 Switch Port 1

Signal Name	Type	Pin No.	Description
STXEN1	O	60	**Transmit Enable :** Please references section 2.2.1 SWITCH PORT0 description.
STXD1[3:0]	O	64,63,62,61	**Transmit Data :** Please references section 2.2.1 SWITCH PORT0 description.
STXCLK1	I	65	**Transmit Clock :** Please references section 2.2.1 SWITCH PORT0 description.
SDUPLEX1	I	66	**Duplex Select :** Please references section 2.2.1 SWITCH PORT0 description.
SCOL_SP1	I	76	**Collision :** Please references section 2.2.1 SWITCH PORT0 description.
SCRS1 Or SCRS_DV1	I	75	**Carrier Sense :** Please references section 2.2.1 SWITCH PORT0 description.
SRXDV1	I	77	**Receive Data Valid :** Please references section 2.2.1 SWITCH PORT0 description.
SRXCLK1	I	78	**Receive Clock :** Please references section 2.2.1 SWITCH PORT0 description.
SRXD1[3:0]	I	82,81,80,79	**Receive Data :** Please references section 2.2.1 SWITCH PORT0 description.

2.3 Expansion Bus Interface for 100 Mbps

Signal Name	Type	Pin No.	Description
HIRD[3:0]	I/O/Z /PU	156, 155 154, 153	**INTER REPEATER DATA :** Nibble data input/output. Transfer data from the "active" AX88872/3 to all other "inactive" AX88872/3 chips. The bus-master of the IRD bus is determined by IR_ACT bus arbitration.
/HIRD_V	I/O/Z /PU	152	**INTER REPEATER DATA VALID :** This signal reflects the RX_DV status of the active port. Used to frame good packets.
HIRD_CK	I/O/Z /PU	151	**INTER REPEATER CLOCK VALID :** All inter repeater signals are synchronized to the rising edge of this clock.
HIRD_ODIR	O	150	**INTER REPEATER DATA IN/OUT DIRECTION :** This pin indicates the direction of IRD data . "High" = HIRD[3:0], /HIRD_V , HIRD_CK are Output. "Low" = HIRD[3:0], /HIRD_V , HIRD_CK are Input.
/LHIR_ACT[2:0]	I/O/OC	128, 126 125	**LOCAL REPEATER ACTIVITY IN/OUT :** the function is the same as /HIR_ACTO[3:0] but for local repeater activity only.
/HIR_ACTI[3:0]	I/PU	132, 131 130, 129	**INTER REPEATER ACTIVITY IN:** These pins perform the same function as /HIR_ACTO[3:0] when they serve as input function. Then the /HIR_ACTO[3:0] insert external buffers the input function must be replaced with /HIR_ACTI [3:0].
/HIR_ACTO[3:0]	I/O/OC	148, 147 146, 145	**INTER REPEATER ACTIVITY IN/OUT:** The local repeater activity appearance, the signal of the related RID (Repeater ID) will be asserted and as an output pin. All other pins serve as input pins but except the collision conditions. When collision occurs , the signal of related (RID-1) pins will also serve as outputs and will active during local collision period. The exception case is when RID = 0, then (RID-1) is replaced with (RID+1).

2.4 Expansion Bus Interface for 10 Mbps

Signal Name	Type	Pin No.	Description
TIRD[3:0]	I/O/Z /PU	106, 105 103, 102	**INTER REPEATER DATA :** Nibble data input/output. Transfer data from the "active" AX88872/3 to all other "inactive" AX88872/3 chips. The bus-master of the IRD bus is determined by IR_ACT bus arbitration.
/TIRD_V	I/O/Z /PU	100	**INTER REPEATER DATA VALID :** This signal reflects the RX_DV status of the active port. Used to frame good packets.
TIRD_CK	I/O/Z /PU	99	**INTER REPEATER CLOCK VALID :** All inter repeater signals are synchronized to the rising edge of this clock.
TIRD_ODIR	O	95	**INTER REPEATER DATA IN/OUT DIRECTION :** This pin indicates the direction of data for external transceiver. "High" = TIRD[3:0], /TIRD_V , TIRD_CK are Output. "Low" = TIRD[3:0], /TIRD_V , TIRD_CK are Input.
/LTIR_ACT[2:0]	I/O/OC	109, 108 107	**LOCAL REPEATER ACTIVITY IN/OUT :** the function is the same as /TIR_ACTO[3:0] but for local repeater activity only.
/TIR_ACTI[3:0]	I/PU	119, 118 117, 116	**INTER REPEATER ACTIVITY IN:** These pins perform the same function as /HIR_ACTO[3:0] when they serve as input function. Then the /HIR_ACTO[3:0] insert external buffers the input function must be replaced with /HIR_ACTI [3:0].
/TIR_ACTO[3:0]	I/O/OC	124, 123 121,120	**INTER REPEATER ACTIVITY IN/OUT:** The local repeater activity appearance, the signal of the related RID (Repeater ID) will be asserted and as an output pin. All other pins serve as input pins but except the collision conditions. When collision occurs , the signal of related (RID-1) pins will also serve as outputs and will active during local collision period. The exception case is when RID = 0, then (RID-1) is replaced with (RID+1).

2.5 LED Display

<table>
<tr><th>Signal Name</th><th>Type</th><th>Pin No.</th><th>Description</th></tr>
<tr><td>LED[1:0]</td><td>O</td><td>85, 84</td><td>Those signals indicate each port‘s statuses (such as activity, jabber and partition) and global information(such as Collision , Repeater ID, Utilization) in sequence. For detail , see the LED timing specification
The utilization of 100M segment and 10M segment are using the same scale.
The Utilization % display define as following : (See also Note 1)
1: Led off
0: Led on
<table>
<tr><th>Utilization %</th><th>UTI0</th><th>UTI1</th><th>UTI2</th><th>UTI3</th><th>UTI4</th><th>UTI5</th></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>5</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>10</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>15</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>30</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>60</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table>
The buffer utilization of internal switch uses the following definition:
1: Led off
0: Led on
<table>
<tr><th>Utilization %</th><th>UTI0</th><th>UTI1</th><th>UTI2</th><th>UTI3</th><th>UTI4</th><th>UTI5</th></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>10</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>20</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>40</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>60</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>80</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>95</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table>
LED[0] : This signal also indicates SRAM chip 0 fail (continue active low) and 100M repeater collision (Blinking) during the interval of sequence shift data.

LED[1] : This signal also indicates SRAM chip 1 fail (continue active low) and 10 M repeater collision (Blinking) during the interval of sequence shift data.</td></tr>
<tr><td>LED_CK</td><td>O</td><td>86</td><td>LED Clock : The signal is a discontinue clock for LED signals serial shift out. The clock period width is 400nS and last 32 cycle with every 52.4ms repeated.</td></tr>
</table>

2.6 Buffer memory pins group

Signal Name	Type	Pin No.	Description
BMA[16:0]	O	197-201 16,17 170,166 143,142 23-18	**SSRAM Address Bus**
BMD[31:24] BMD[23:16] BMD[15:8] BMD[7:0]	I/O	24, 26-32 133-138 140, 141 171-173 175-179 180, 188-194	**SSRAM Data Bus**
/BMWE	O	158	**SSRAM Write Strobe**
/BMOE	O	159	**SSRAM Read Strobe**
BMCLK	O	72	**SSRAM CLOCK**

2.7 Miscellaneous

Signal Name	Type	Pin No.	Description
LCLK	I	70	**Local Clock :** 50-66Mhz. Used for system operation synchronous.
/RST	I	59	**Reset :** Active Low The chip is reset when this signal is asserted Low
REF_CLK	I	68	**Reference clock :** The input is a continuous clock at 50Mhz for timing reference with RMII interface.
DAISY_IN	I/PU	73	**Repeater Identification Number Daisy-Chain In :** When MODE="1" , This pin is a daisy chain serial input for Repeater ID. The State machines always monitors the input if a correct data (RID) present at the pin, the (RID+1) will be written to RID register and override the power on setup RID for the chip.
DAISY_OUT	O/ML	74	**Repeater Identification Number Daisy-Chain Out :** When MODE="1" , This pin is periodically shift out the RID of itself to the next chained chip to inform that this ID has already been occupied. The RID is shift out periodically every about 200us.
MDIO	I/O	57	**Station Management Data In/Out :** For setup PHY auto-negotiation registers. A burst write commands are issue to setup PHY register after reset. The PHY address 4h, 5h, 6h, 7h, 8h, 9h,Ah and Bh will be written as register 4h to value 00A1h (Advertise register set to 10/100 half-duplex mode)and register 0h to value 1000h(Enable auto-negotiation). See also Appendix for more information.
MDC	O	56	**Station Management Data Clock Out :** For MDIO reference clock.
/TEST	I/PU	58	**Test Pin :** Active LOW The pin is just for test mode setting purpose only. Must be pull high when normal operation.
NC	O	157	**NC :** Keep no connection
VDD	I	25, 48 69, 92 122, 144 107, 120	**POWER :** +3.3V +/-5%
VSS	I	8, 35 67, 71 83, 101 112,115 127, 139 149, 174 185, 208	**POWER:** 0V

2.8 Power on configuration setup signals cross reference table

Signal Name	Share with	Description
/Hash_En	BMA[16]	**Hash Algorithm Enable :** 0 : Enable look-up table addressing use hashing algorithm. 1 : Disable look-up table addressing use linear addressing
Aging_S[2:0]	BMA[15:13]	**Aging Timer Selection :** **Aging_S2 Aging_S1 Aging_S0 Aging Time (Min)** 1 1 1 no aging (disable) 1 1 0 5 1 0 1 10 1 0 0 20 0 1 1 40 0 1 0 160 0 0 1 640 0 0 0 1
RxFC_En	BMA[12]	**PAUSE Identification Enable :** 0 : Disable 802.3x receives flow control function in full duplex. 1 : Enable 802.3x receives flow control function in full duplex.
MII_S1	BMA[11]	**MII/RMII Interface Selection for Switch Port 1:** 0 : Switch port 1 “RMII” mode is selected 1 : Switch port 1 “MII” mode is selected
MII_S0	BMA[10]	**MII/RMII Interface Selection for Switch Port 0:** 0 : Switch port 0 “RMII” mode is selected 1 : Switch port 0 “MII” mode is selected
/Part_En	BMA[9]	**TX Partition Enable :** 0 : Enable partition function of transmission. 1 : Disable partition function of transmission.
RAM_S	BMA[5]	**RAM Size Selection :** External packet buffer RAM size select **RAM_S RAM SIZE** 1 64K * 32 SSRAM 0 128K * 32 SSRAM
NetQlty_S	BMA[4]	**Network Quality Selection:** Auto forwarding mode is based on packet error percentage to select Store-and-Forward or Fragment Free mode. **NetQlty_S Error Packet Ratio** 1 20% 0 40%
FwTyp_S1 FwTyp_S0	BMA[3] BMA[2]	**Forward Type Selection :** **FwTyp _S1 FwTyp _S0 Forward Mode** 1 1 Store & Forward 1 0 Store & Forward 0 1 Fragment Free 0 0 Auto
HiBndy_S1 HiBndy_S0	BMA[1] BMA[0]	**Threshold Selection for Flow Control :** Flow control will be active when buffer memory is below the threshold: **HiBndy_S1 HiBndy_S0 Buffers Left** 1 1 64 packets 1 0 32 packets 0 1 16 packets 0 0 96 packets
/ FlowCtl _En3	STXD0[3]	**P3 Flow Control Enable :** Enable flow control function of switch port 3 (Link to 10Mbps repeater port), back pressure for half duplex. 0 : Enable flow control function.

		1 : Disable flow control function.
/ FlowCtl _En2	STXD0[2]	**P2 Flow Control Enable :** Enable flow control function of switch port 2 (Link to 100Mbps repeater port), back pressure for half duplex. 0 : Enable flow control function. 1 : Disable flow control function.
/ FlowCtl _En1	STXD0[1]	**P1 Flow Control Enable :** Enable flow control functions of switch port 1, 802.3x for full duplex, back pressure for half duplex. 0 : Enable flow control function. 1 : Disable flow control function.
/FlowCtl_En0	STXD0[0]	**P0 Flow Control Enable :** Enable flow control function of switch port 0, 802.3x for full duplex, back pressure for half duplex. 0 : Enable flow control function. 1 : Disable flow control function.
Speed_S2	TXD7[1]	**Speed Setting for Repeater Port 0 to Port 7 :** 0 : SPEED0~7 pin is Low for 10M,high for 100M 1 : SPEED0~7 pin is Low for 100M,high for 10M
Speed_S1	STXD1[2]	**Speed Setting for Switch Port 1 :** It is useful for switch port 1 in RMII mode Don't care the setting when switch port 1 is in MII mode. 0 : SCOL_SP1 pin is Low for 10M,high for 100M 1 : SCOL_SP1 pin is Low for 100M,high for 10M
Speed_S0	STXD1[1]	**Speed Setting for Switch Port 0 :** It is useful for switch port 0 in RMII mode Don't care the setting when switch port 0 is in MII mode. 0 : SCOL_SP0 pin is Low for 10M,high for 100M 1 : SCOL_SP0 pin is Low for 100M,high for 10M
FdpxHi_S1	STXD1[0]	**Duplex Setting for Switch Port 1 :** Switch Port 1 "SDUPLEX1" pin function select 0 : SDUPLEX1 pin is low for half duplex,high for full duplex 1 : SDUPLEX1 pin is low for full duplex,high for half duplex
FdpxHi_S0	STXEN1	**Duplex Setting for Switch Port 0 :** Switch Port 0 "SDUPLEX0" pin function selection 0 : SDUPLEX0 pin is low for half duplex,high for full duplex 1 : SDUPLEX0 pin is low for full duplex,high for half duplex
LRID_S1 LRID_S0	TXD5[1] TXD5[0]	**Local Repeater ID Selection :** **LRID_S1 LRID_S0 LRID No.** 1 1 0 1 0 1 0 1 2 0 0 reserved
/871_En	TXEN6	**AX88871A Compatible Enable :** 0 : Enable AX88871A compatible mode 1 : Disable AX88871A compatible mode
/RdPhy_En	TXD6[0]	**MDIO read PHY Register 05h Information** 0 : Enable 1 : Disable
WrPhyNo_S	TXD4[1]	**MDIO Write PHY Number Selection** 1 : MDIO Write 8 PHY address 0 : MDIO Write 6 PHY address (for 6R+2S application)
WrPhyRegNo_S	TXD4[0]	**MDIO Write PHY Register Number Selection** 0 : MDIO Write 2 Registers (04h, 00h) 1 : MDIO Write 3 Registers (10h, 04h, 00h)
WrPhyStrAddr	TXD3[1]	**MDIO Write PHY Starting Address** 0 : MDIO Write PHY from address 18h (18h to 1Fh) 1 : MDIO Write PHY from address 04h (04h to 0Bh)
PktLenOpt	TXD3[0]	**Maximun Packet Length Selection** 0 : 1522 Byte

		1 : 1518 Byte

All of the above signals are pull-up for default values.

Note 1 :

The calculation formulae of Traffic Utilization between ASIX and NetCom is difference, so you will get different results when using SmartBit (SB) testing this item.

We found the SmartBit calculate the Utilization without include 96 Bit time inter frame gap (IFG). So the utilization value can be 100%. As well as we found SB used min packet size (64 byte) and min IFG (96 bit-time) as 100% utilization. In theory, when max packet size (1518 byte) and min IFG the utilization will be more than 100%, but SB also treat it as 100%.

In our AX88872 design, we use real cable bandwidth as calculation base. We calculate the bit counts of carrier within a unit time. Because of the existence of inter frame gap, In our calculation 100% utilization is impossible. So the above two cases (64 byte packet size and 1518 byte packet size with min. IFG), we will count as 85.7% and 99.2%.

If using SB test result to indicate utilization LED the value must be modified. See the following reference table.

ASIX's Utilization%	1	5	10	15	30	60
SmartBit's Utilization%	2	7	12	17	34	68

3.0 Functional Description

3.1 Repeater State Machine

The repeater state machine is in idle state when there is no carrier presented on any ports **.** When there is only one port has receive activity, the repeater state machine will enter data -forwarding state to ensure correct data forwarding to other connected ports. If collision happens anytime, The repeater state machine detects collision then send jam pattern to all ports until collision ceases.

3.2 RXE /TXE Control

Idle state

CRS_DV(ALL) = 0, the repeater sends no data to any port.

RXE(ALL) = 0.
TXE(ALL) = 0.

Data Forwarding state

If CRS_DV(ALL) = 1, N is the only one port that has incoming packet.

RXE(N) = 1, RXE(ALLXN) = 0.
TXE(N) = 0, TXE(ALLXN) = 1.

Collision state

If CRS_DV(ALL) > 1, the repeater sends jam pattern to all ports.

RXE(ALL) = 0.
TXE(ALL) = 1.

One Port Left state

When all packets are back off except only one port still has activity, that is CRS_DV(ALL) = 1 again . N is the only one left port that has incoming packet. The repeater sends jam pattern to all other port except for the still activity ports.

RXE(ALL) = 0.
TXE(ALLXN) = 1.

3.3 Jabber State Machine

To prevent an illegally long reception of data from reaching the repeater unit, each port has its own jabber timer. If a reception exceeds this duration (64K bit times for AX88872), the jabber condition will be detected. In this condition, repeater unit will disable receive and transmit packets for the jabbered port and the other ports remain the normal operation.

When the carrier is no longer detected for the jabbered port or reset the repeater, the jabber state will be existed and the port will receive and transmit packets normally.

3.4 Partition State Machine

The partition state machine is used to protect network from being upset when a port suffer continuous

collision, each port uses a partition state machine to detect and prevent this condition. When a port suffers from continuous 64 times of collision events, then it goes to Partition State. The partitioned port will be not released until a packet without collision be transmitted(more than 512 bit times for AX88872) or reset the repeater.

3.5 Operation of the Built-In Switch

In general, the basic operation of the switch is very simple. The switch receives incoming packets from one of its ports, searches in the Look-Up Table for the Destination MAC Address and then forwards the packet to the destination ports, if appropriate. If the destination MAC address is not found in the Look-Up Table, the switch treats the incoming packet as a broadcast packet and forwards it to all ports except itself. Basically the switch automatically learns the port number of attached network devices by examining the Source MAC Address of all incoming packets. The device is updated the table with the Source MAC Address if the Source MAC Address does not exist the table.

3.5.1 Packet Filtering and Forwarding Process

During the receiving process, the switch will monitor the length of the received packet. Legal Ethernet packets should have a length of no less 64 bytes and nor more than 1528 bytes. The switch discards any packet with illegal length.

After a packet is received, its Source MAC Address and Destination MAC Address are received. The Source MAC Address is used to update the Look-Up Table and the Destination MAC Address is used to determine the destination port of the packet. Once a MAC Address has been learned, and the packet is buffered, it must be forwarded, That is, the packet forwarding mechanism for the switch is handled automatically based on the destination MAC Address.

Under the following conditions, received packets are filtered:

- The switch will check all received packets for errors, e.g., FCS error, runt packet, long packet, etc.
- Any packet handing to its own source port will be filtered. That is, its destination port is its source port.
- The incoming packet will be discarded if the switch's buffer memory is full.

The switch supports three forwarding modes: Store-and-Forward, Fragment-Free and Auto.

- Store-and-Forward Mode: An entry packet is received, checked and stored in the buffer memory before it is forwarded. That is, each forwarded packet is correct.
- Fragment-Free Mode: It is a simple improvement on Cut-Through method. The switch will forward a packet whose packet length is more than 64 bytes. All runt packets will be filtered in Fragment-Free mode.
- Auto Mode: In Auto mode, the switch select dynamically its optimized forwarding mode based on the current network quality of each port.

3.5.2 MAC Address Learning and Aging Process

The switch can learn up to 8K unique MAC addresses with a hashing algorithm. Addresses are stored in the Look-Up Table located in external SSRAM, then each packet updates the table.

The table lookup engine provides the switching information required routing the data packets. The address table is set up through auto address learning dynamically. After the switch receives a packet, the Source MAC Address and Destination MAC Address are received. The Source Address retrieved from the received packet is automatically stored in a SA buffer. The switch will check for error and perform a SA search. The switch will update the Look-Up Table with the Source MAC Address if there is no error.

The Look-Up Table is cleared on power-on, or hardware reset. When the aging option is enabled, the dynamically Learned SA will be cleared if it is not refreshed in less than configured time (2 or 5 min).

3.5.3 Flow Control Process

The switch can operate at two different modes: half-duplex and full-duplex. Each port can be configured to have flow control enabled or not. The switch supports 802.3X for full-duplex operation and uses back pressure for half-duplex.

In full-duplex mode, the switch will receive and transmit the packet in accordance to 802.3X. The transmission channel and the receiving channel operate independently. If the occupancy of the buffer memory is above the FlowControlActive

threshold, the MAC of port will send out a PAUSE frame with maximum delay. The switch will send out a PAUSE frame with zero delay after below FlowControlActive threshold.

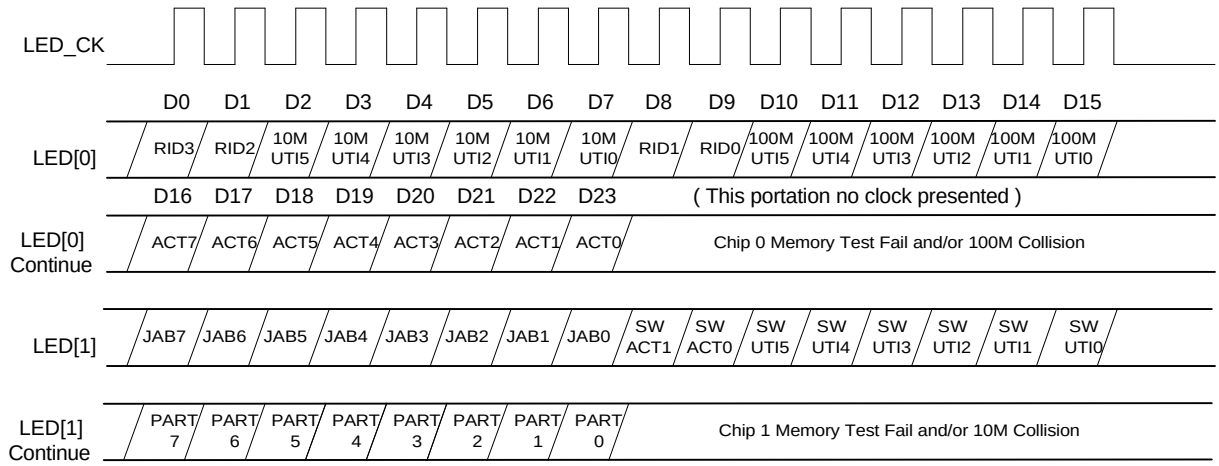
For the receiving channel, the switch will not transmit the next packet whenever received a PAUSE frame with non-zero delay. The switch will resume packet transmission either after the pause timer expired or a PAUSE frames with zero delay received.

In half-duplex mode, the switch will receive and transmit the packet in accordance to 802.3 CSMA/CD. If the occupancy of the buffer memory is above the FlowControlActive threshold, the MAC of port will send out JAM pattern .

3.6 LED Display Interface

AX88872 provides per-port LED status indication for partition, jabber, activity and support rate - based LED for 10 and 100Mbps segments utilization (%) and switch buffer utilization (%) . All LED[1:0] perform active low.

LED[1:0] Status Driver Wave-form as follows :



Notes:

a. PART7~0indicates partition status for each port
b. JAB7~0 indicates jabber status for each port
c. ACT7~0 indicates activity status for each port
d. RID3~0 is the ID of repeater chip
e. 10M UTI5~0 indicate global utilization rate of 10Mbps for each 104.8ms sampling period.
f. 100M UTI5~0 indicate global utilization rate of 100Mbps for each 104.8ms sampling period.
g. SW UTI5~0 indicate global utilization rate of Switch packet buffers for each 104.8ms sampling period.
h. RAM FAIL : Switch RAM test fail.

It has to use external shift register to decode data on LED[1:0]. The application shows as follows:

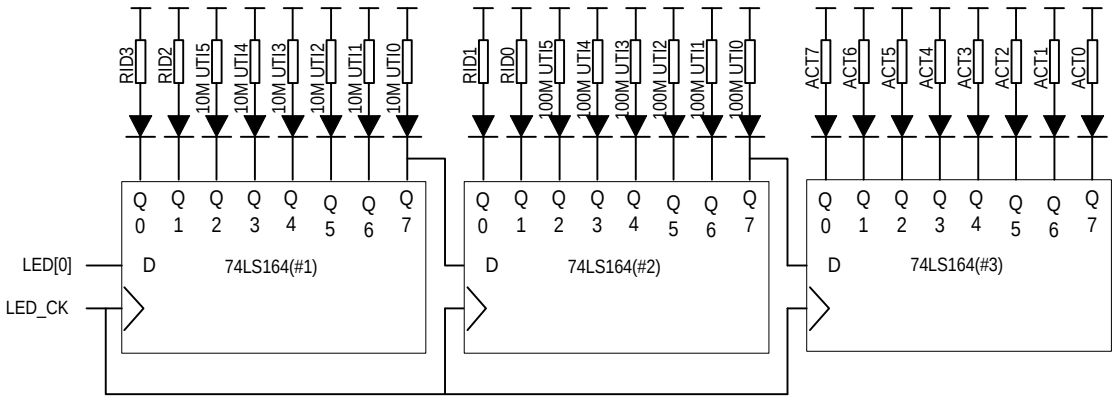


Fig - 3 Application for LED display

If the user don‘t want to show jabber status, take away the latter 74LS164(#2). The application is the same for LED[1].

4.0 INTERNAL REGISTERS

(This page keep blank)

5.0 ELECTRICAL SPECIFICATION AND TIMING

5.1 Absolute Maximum Ratings

Description	SYM	Min	Max	Units
Operating Temperature	Ta	0	+70	°C
Storage Temperature	Ts	-55	+150	°C
Supply Voltage	Vcc	-0.3	+4	V
Input Voltage	Vin	-0.3	Vdd+0.5	V
Output Voltage	Vout	-0.3	Vdd+0.5	V
Lead Temperature (soldering 10 seconds maximum)	Tl	-55	+220	°C

Note : Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to Absolute Maximum Ratings conditions for extended period, adversely affect device life and reliability

5.2 General Operation Conditions

Description	SYM	Min	Max	Units
Operating Temperature	Ta	0	+70	°C
Supply Voltage	Vdd	+3.0	+3.6	V

5.3 DC Characteristics

(Vdd=3.0V to 3.6V, Vss=0V, Ta=0°C to 70°C)

Description	SYM	Min	Max	Units
Low Input Voltage	Vil	Vss-0.3	0.8	V
High Input Voltage	Vih	2	Vdd+0.5	V
Low Output Voltage	Vol		0.4	V
High Output Voltage	Voh	2.4		V
Input Leakage Current 1 (Note 1)	Iil1		10	uA
Input Leakage Current 2 (Note 2)	Iil1		500	uA
Output Leakage Current	Iol		10	uA

Description	SYM	Min	Typ	Max	Units
Power Consumption	Pc		TBD		mA

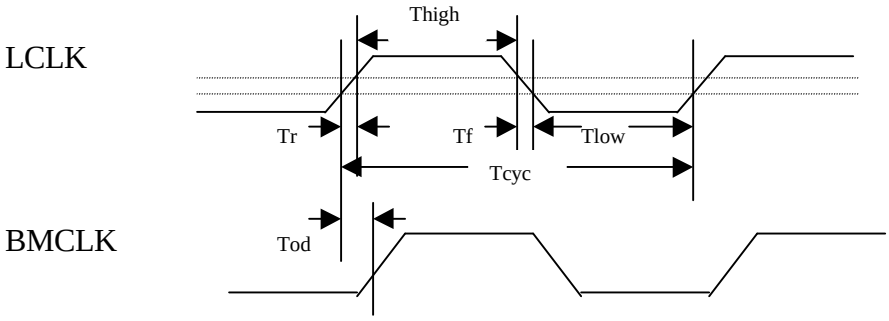
Note :

a. All the input pins without pull low or pull high.

b. Those pins had been pull low or pull high.

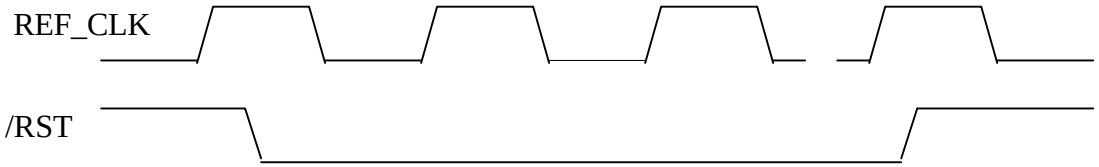
5.4 AC specifications

5.4.1 LCLK



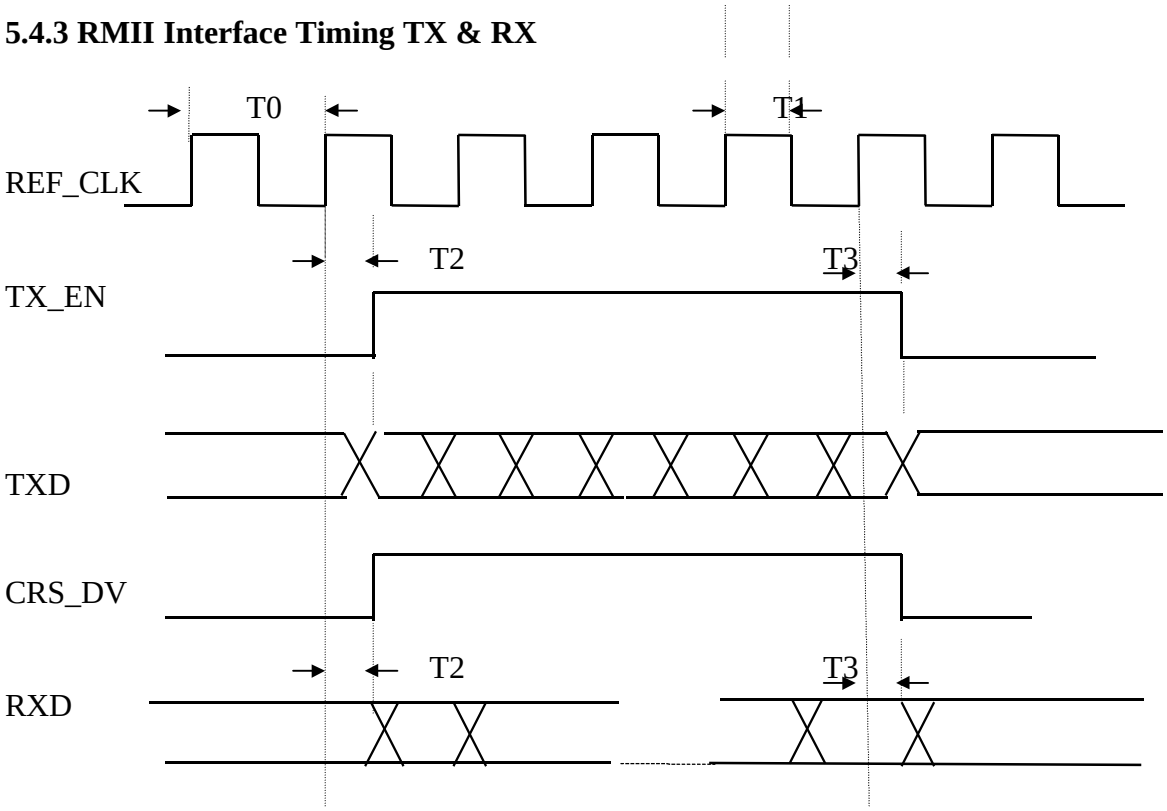
Symbol	Description	Min	Typ.	Max	Units
Tcyc	CYCLE TIME		20		ns
Thigh	CLK HIGH TIME	8	10	12	ns
Tlow	CLK LOW TIME	8	10	12	ns
Tr/Tf	CLK SLEW RATE	1	-	4	ns
Tod	LCLK TO BMCLK OUT DELAY		2		ns

5.4.2 Reset Timing



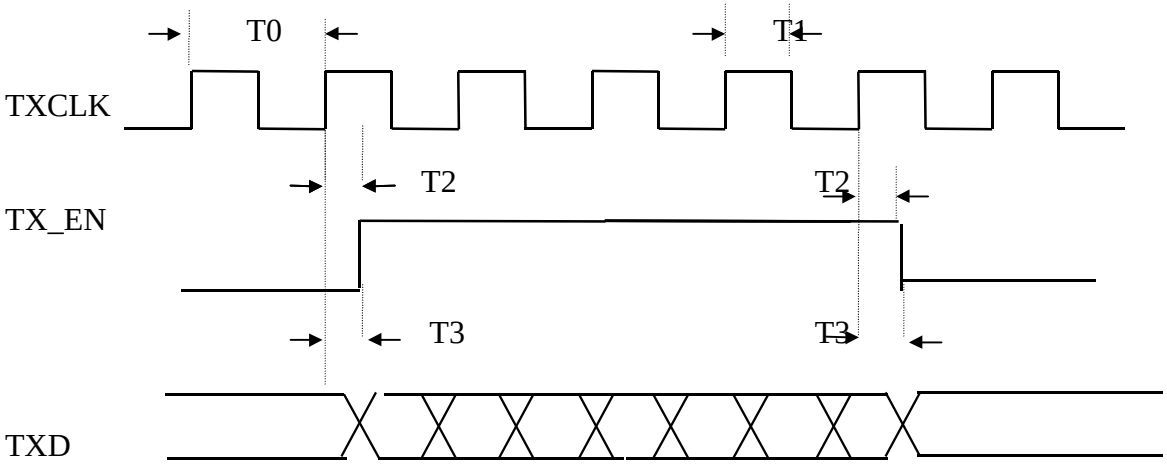
Symbol	Description	Min	Typ.	Max	Units
Trst	Reset pulse width	10	-	-	REF_Clk

5.4.3 RMII Interface Timing TX & RX

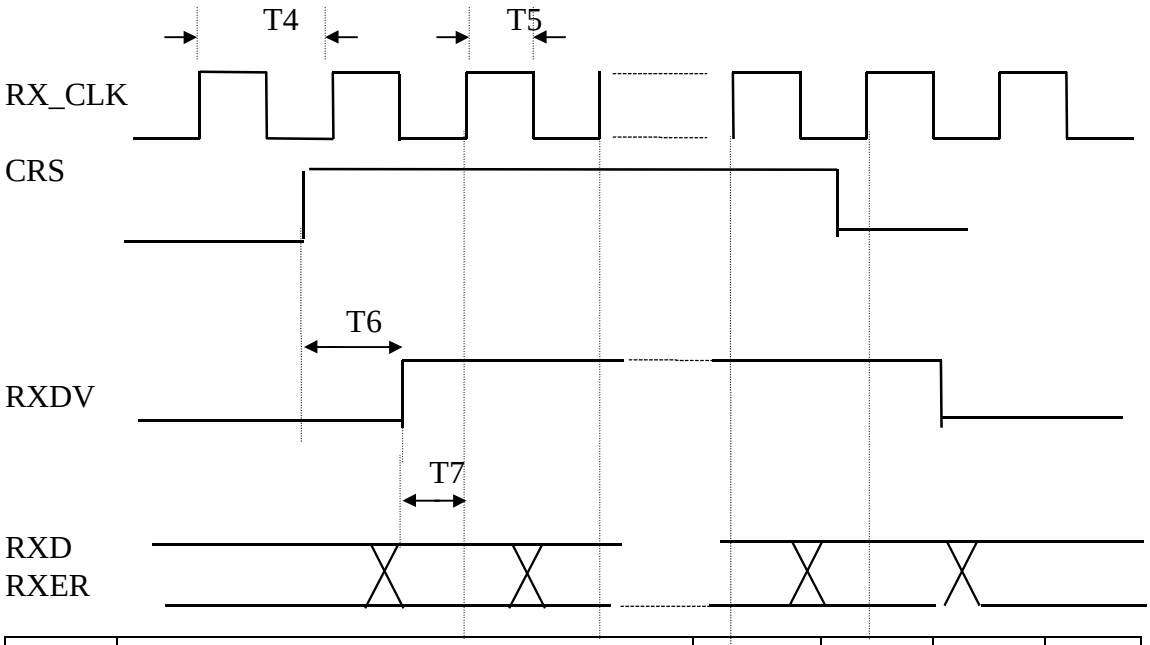


Symbol	Description	Min	Typ.	Max	Units
T0	REF_CLK Clock Cycle Time	19.998	20	20.002	ns
T1	REF_CLK Clock High Time	7	10	13	ns
T2	CRS_DV, RXD, TXEN and TXD data setup to REF_CLK rising edge	4			ns
T3	CRS_DV, RXD, TXEN and TXD data hold from REF_CLK rising edge	2			ns

5.4.4 MII Interface Timing TX & RX



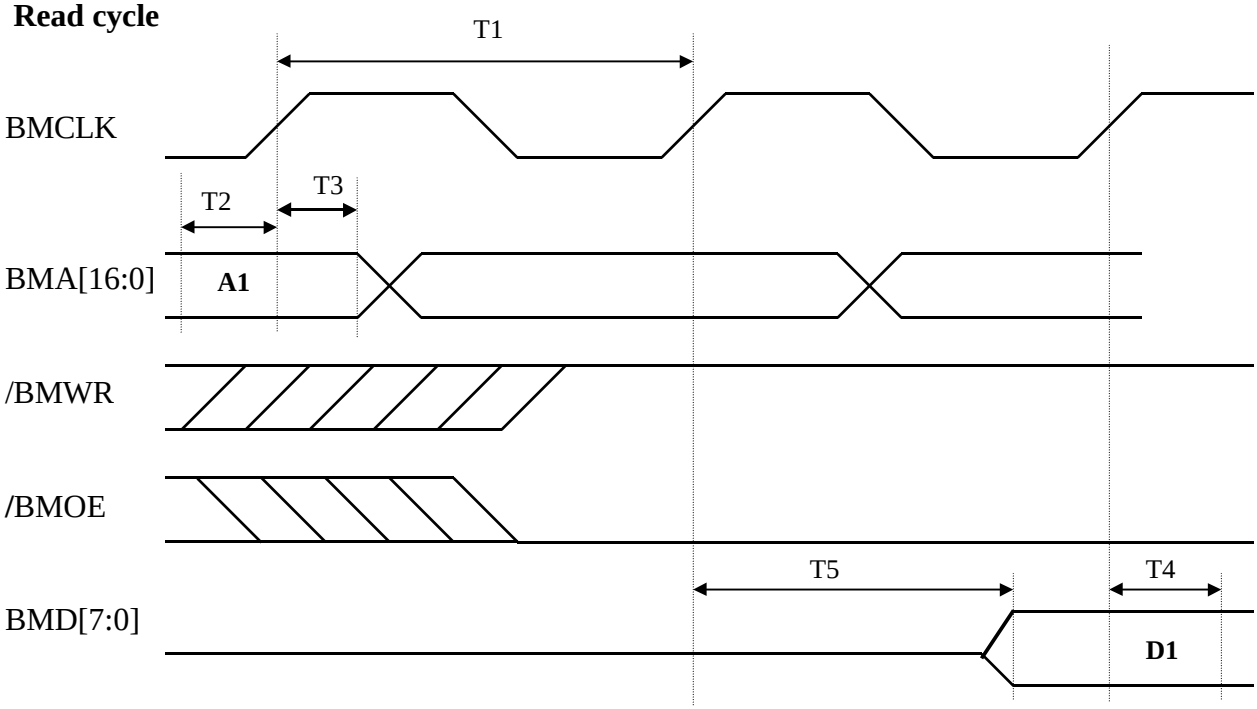
Symbol	Description	Min	Typ.	Max	Units
T0	TXCLK Cycle Time	39.996	40	40.004	ns
T1	TXCLK High Time	14	20	26	ns
T2	TX_EN Delay from TXCLK High	7.440		21.760	ns
T3	TXD Delay from TXCLK High	3.410		13.320	ns



Symbol	Description	Min	Typ.	Max	Units
T4	RX_CLK Clock Cycle Time	39.996	40	40.004	ns
T5	RX_CLK Clock High Time	14	20	26	ns
T6	CRS to RXDV Delay Requirement	40		160	ns
T7	RXD or RXDV setup to RX_CLK rise time	10		-	ns

5.4.5 SRAM read cycle

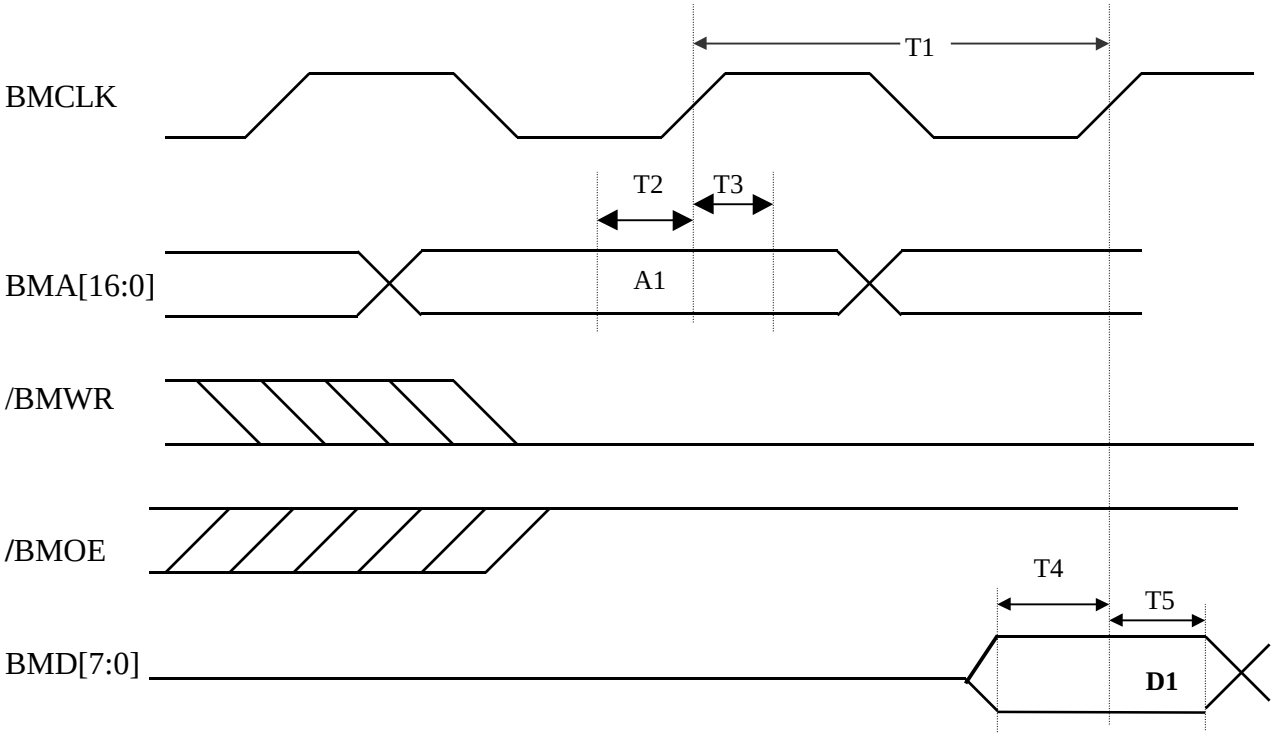
Read cycle



Symbol	Description	Min	Max	Units
T1	Clock Cycle Time	15	-	ns
T2	Address Bus Setup Time	2.5	-	ns
T3	Address Bus Hold Time	0.5	-	ns
T4	Clock to Output Invalid	2	-	ns
T5	Clock to Output Valid	-	6	ns

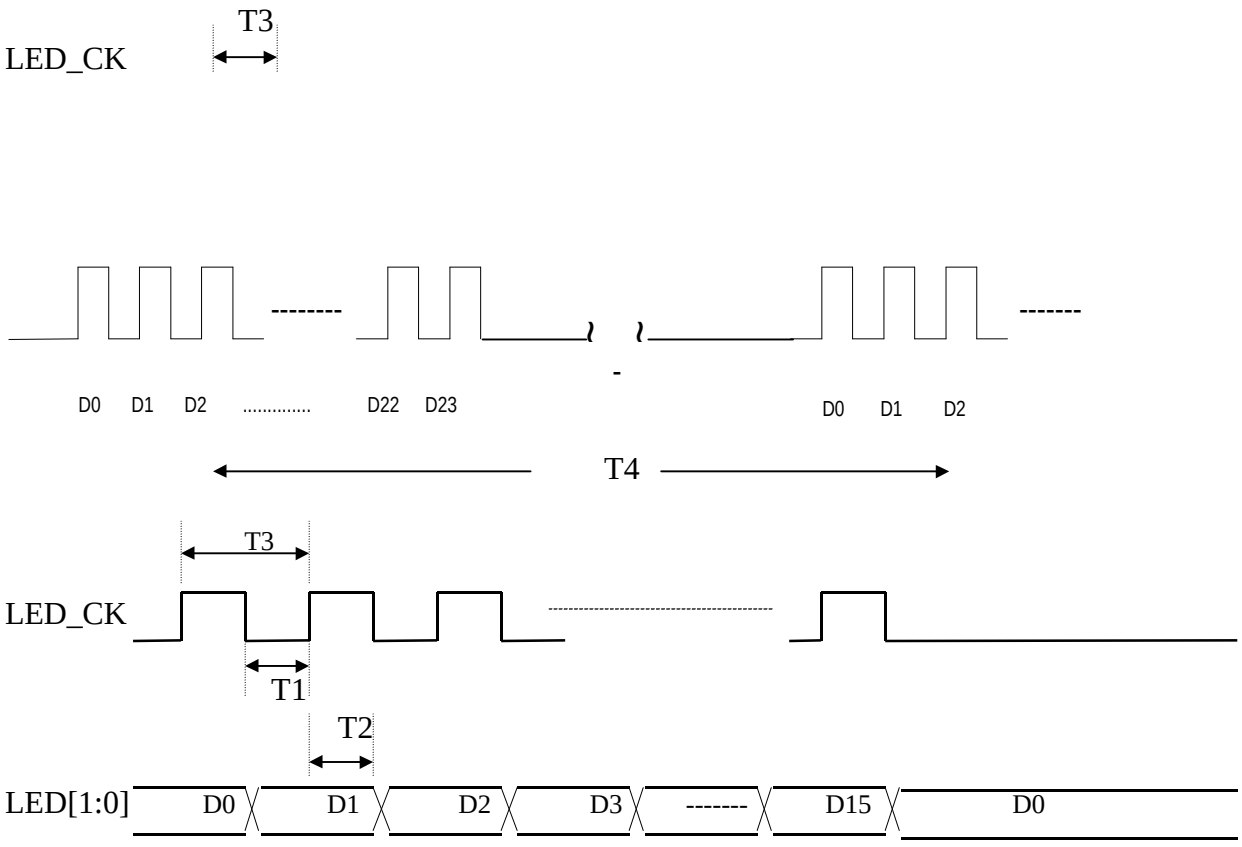
5.4.6 SRAM write cycle

T1



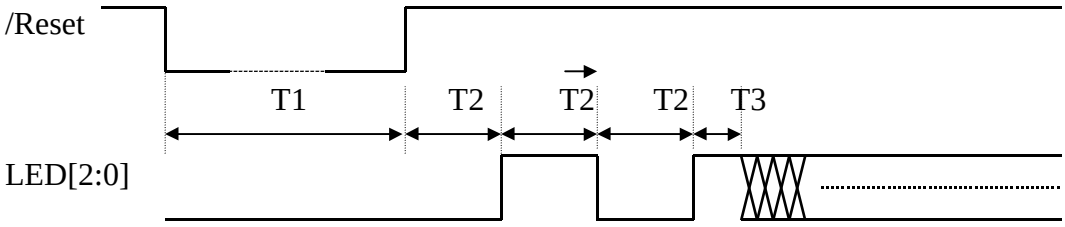
Symbol	Description	Min	Max	Units
T1	Clock Cycle Time	15	-	ns
T2	Address Bus Setup Time	2.5	-	ns
T3	Address Bus Hold Time	0.5	-	ns
T4	Write Data Setup Time	2.5	-	ns
T7	Write Data Hold Time	0.5	-	ns

5.4.7 LED DISPLAY



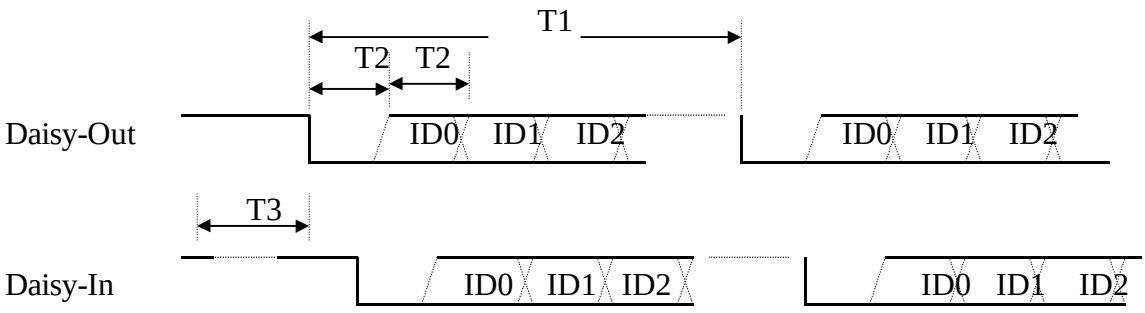
Symbol	Description	Min	Typ.	Max	Units
T1	LED setup to LED_CK High	190		200	ns
T2	LED hold from LED_CK High	200		210	ns
T3	LED_CK Period Width		400		ns
T4	LED_CK Cycle burst out period		52.4		ms

5.4.8 LED Display after Reset



Symbol	Description	Min	Typ.	Max	Units
T1	Repeater reset time	1000			ns
T2	LED Blink Time After Reset		838.4		ms
T3	LED Dark Time Before Normal Display		419.2		ms

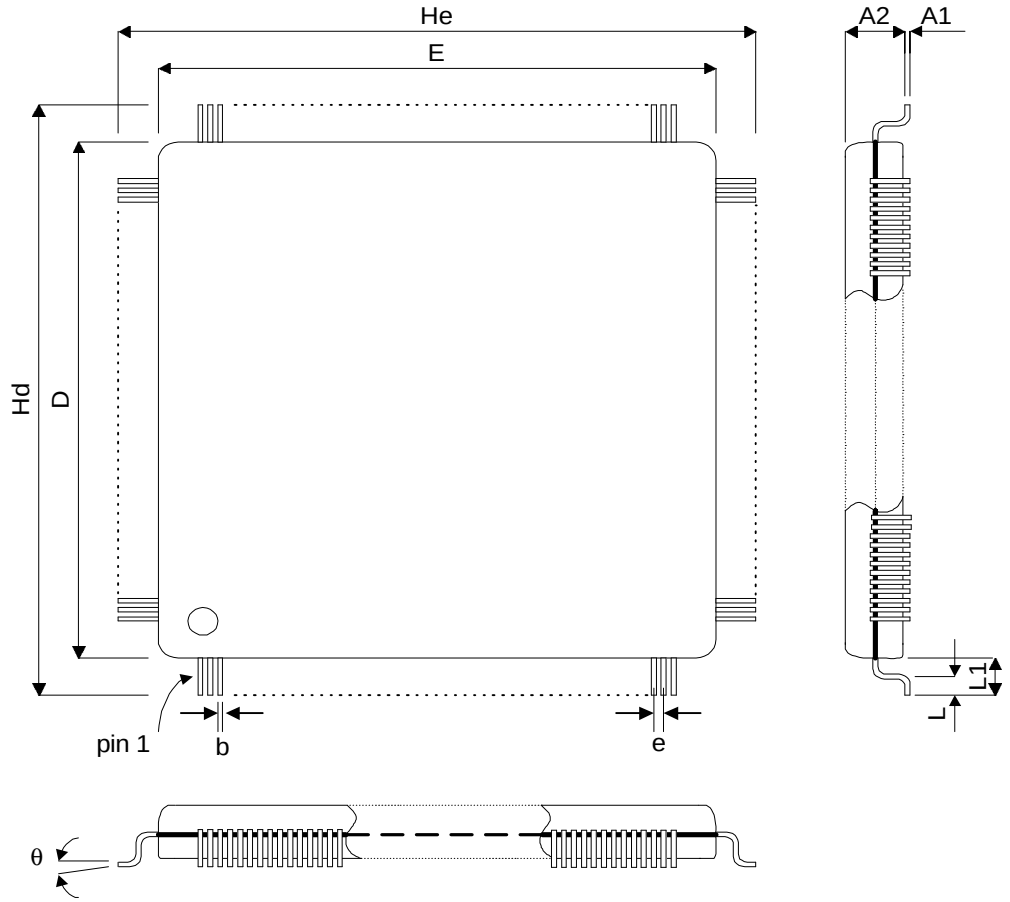
5.4.9 Repeater ID Daisy Chain



Symbol	Description	Min	Typ.	Max	Units
T1	Daisy Chain One Burst period		204.8		us
T2	Start Bit Period or Data Width		12.8		us
T3	Time-out occur when no data present on Daisy_in *		3.8		s

Note : Daisy-Chain Data-In Time-out stands for no input data (always high level) for the specific time.

6.0 PACKAGE INFORMATION

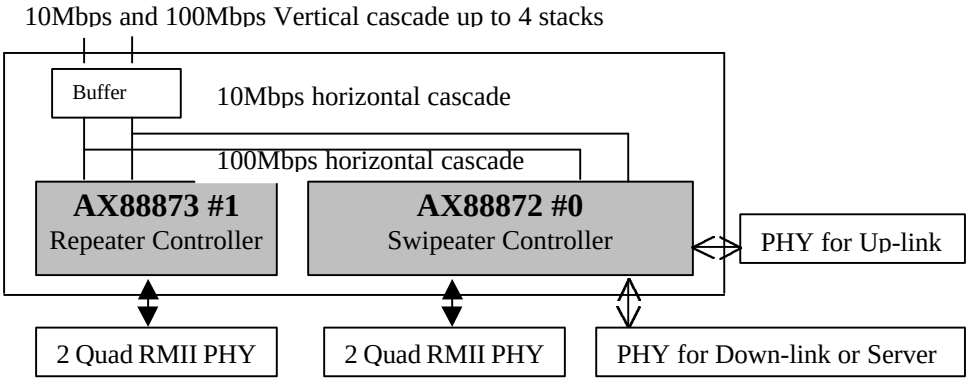


SYMBOL	MILIMETER		
	MIN.	NOM	MAX
A1	0.05	0.25	0.5
A2	3.17	3.32	3.47
b	0.10	0.20	0.30
D	27.90	28.00	28.10
E	27.90	28.00	28.10
e		0.50	
Hd	30.35	30.60	30.85
He	30.35	30.60	30.85
L	0.45	0.60	0.75
L1		1.30	
θ	0		10

Appendix A: System Applications

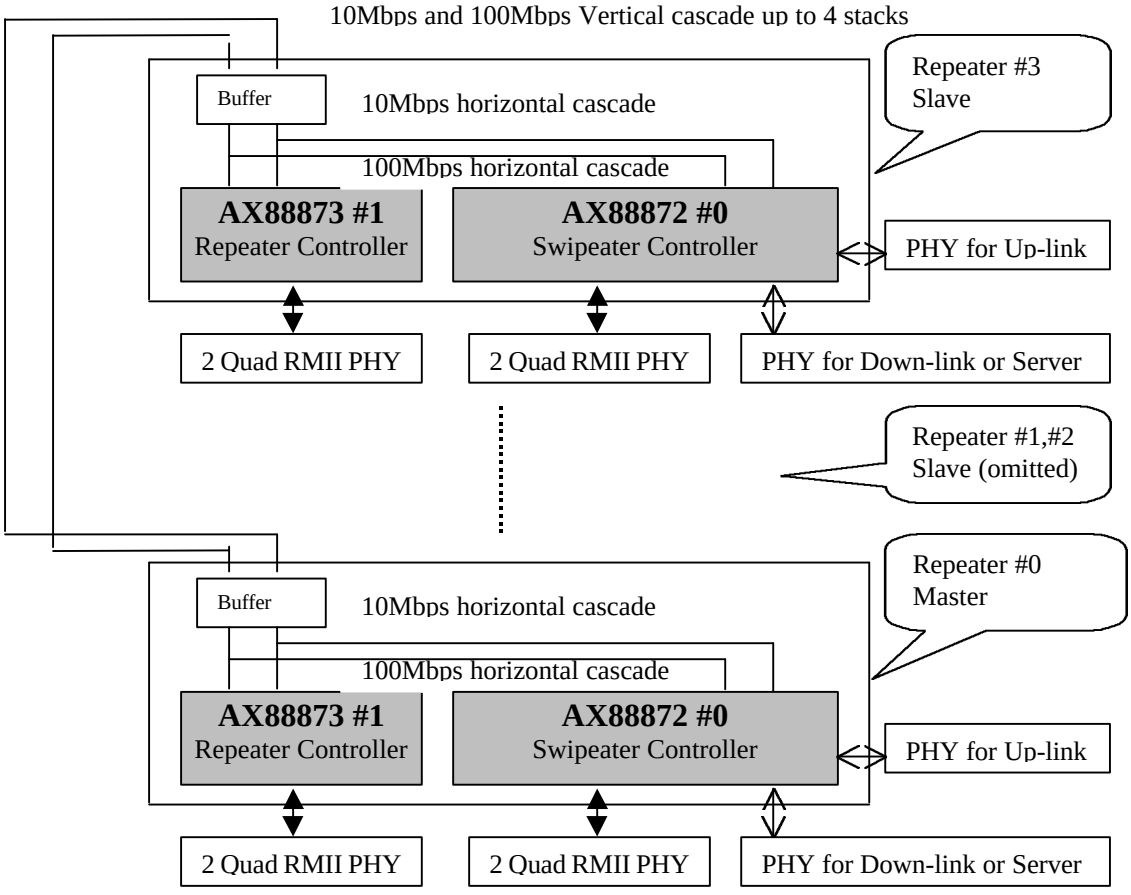
Some typical applications for AX88872 are illustrated bellow.

A.1 16-port (24-port) repeater with 2-port switch

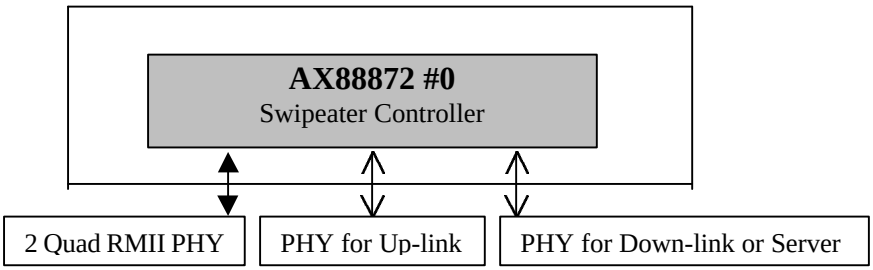


Note : Add additional AX88873 to build a 24-port repeater

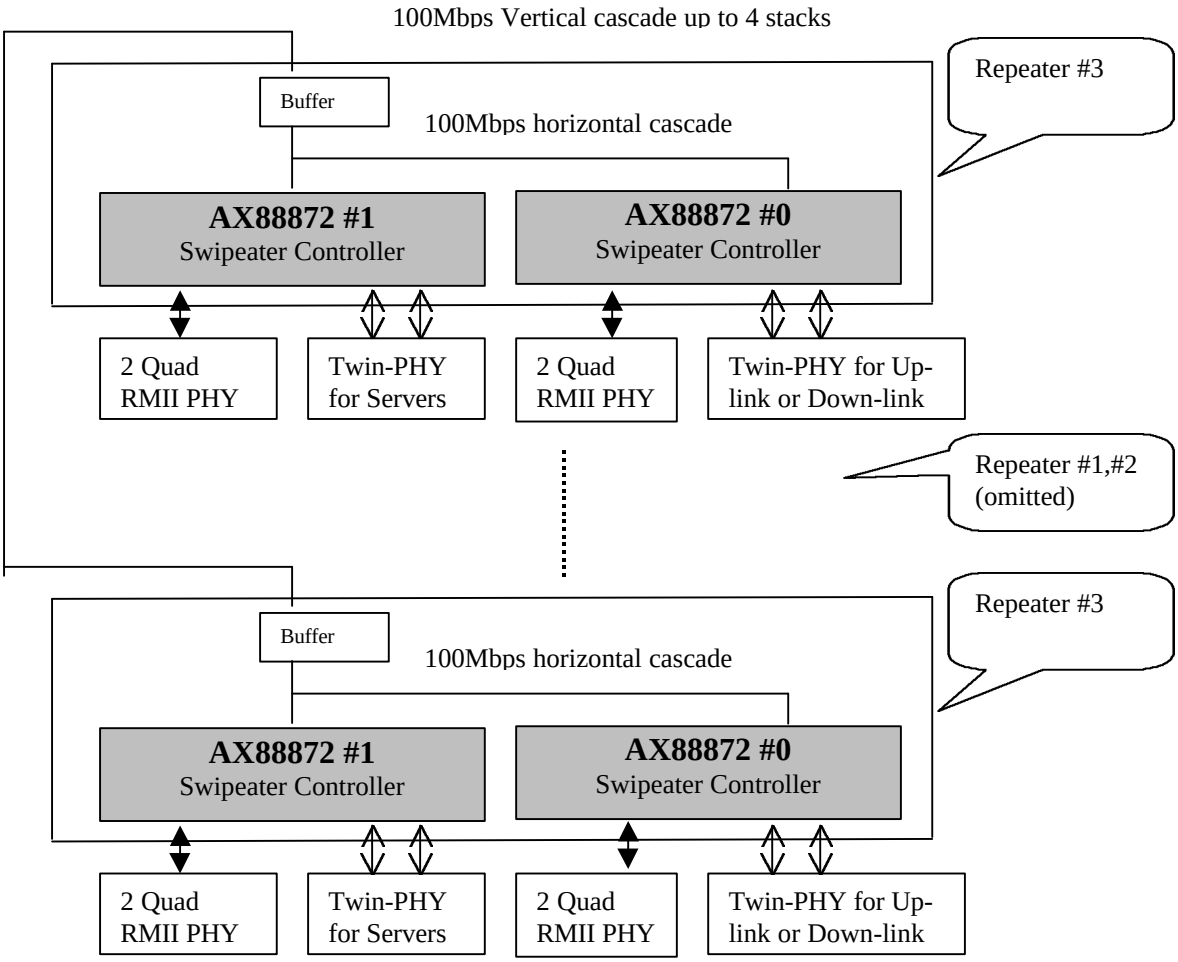
A.2 16-port repeater with up to 4 stacks



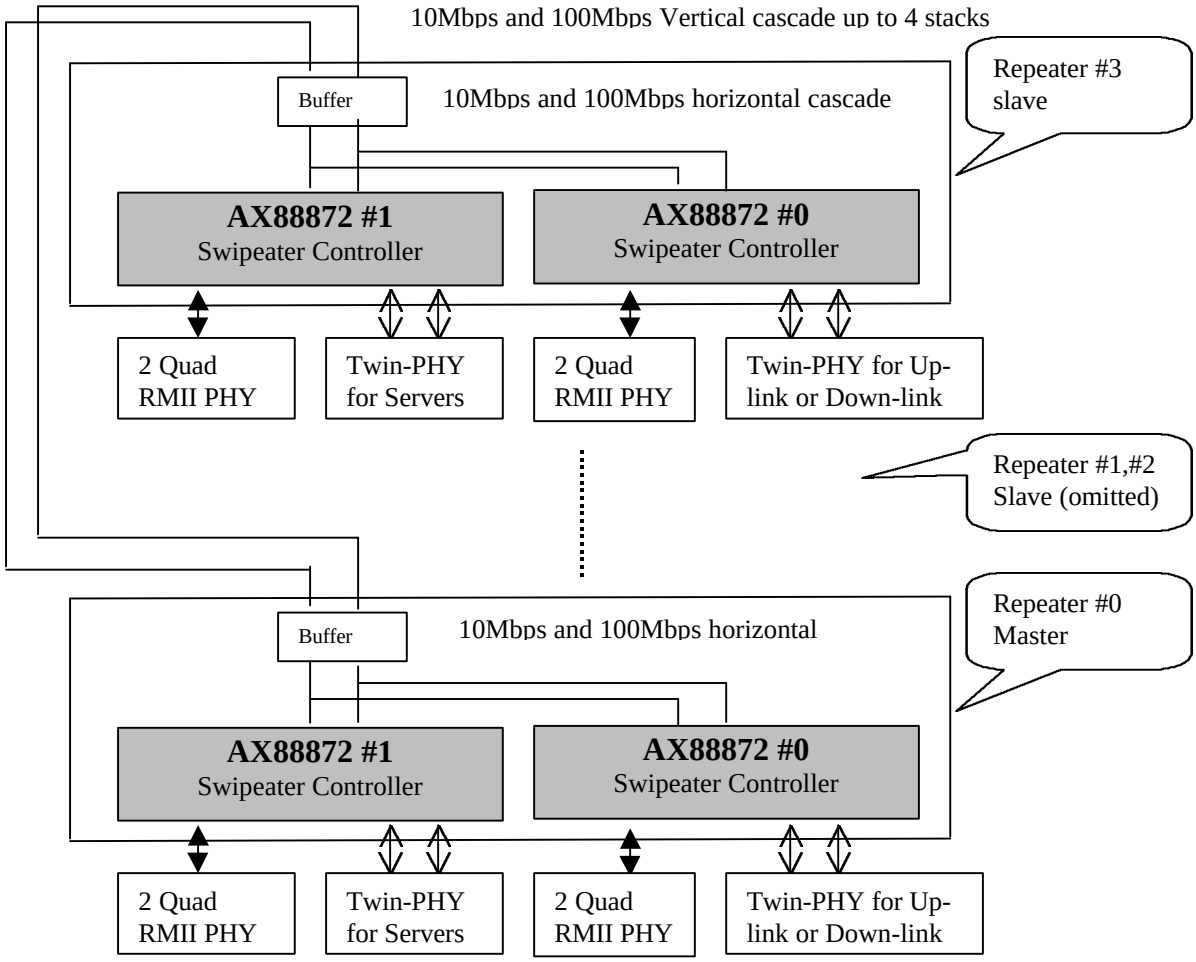
A.3 8-port standalone repeater with 2-port switch



A.4 16-port repeater with up to 4 stacks of AX88871A compatible mode



A.5 16-port repeater with up to 4 stacks and more switch ports



Note : Only the switch ports between 10M and 100M segment of Repeater #0/AX88872 #0 are enable

Appendix B: Design Note

B.1 Using Station Management (STA) Connection

There are two methods to get two switch port speed and duplex information in AX88872 . One way is by hardware pins such as SPEED0, SDUPLEX0, SPEED1, SDUPLEX1. AX88872 also provides 2 pins (MDC and MDIO, STA – Station Management connection) to read PHY Auto Negotiation Remote Capability register to get current speed and duplex status. For the PHY connected to repeater ports must be configured by STA write function. In a word, AX88872 use STA read function to get PHY register status for switch port and use STA write function to program PHY register for hub port. The address setting of PHY must be fixed as follows:

Application 1: 8 hub ports + 2 switch ports application

RP : repeater port SP : switch port

RP0	RP1	RP2	RP3	RP4	RP5	RP6	RP7	SP0	SP1
04h	05h	06h	07h	08h	09h	0ah	0bh	0fh	10h

The corresponding option setting
/RdPhy_En = 0, WrPhyNo_S = 1, WrPhyStrAddr = 1

Application 2: 6 hub ports + 2 switch ports application

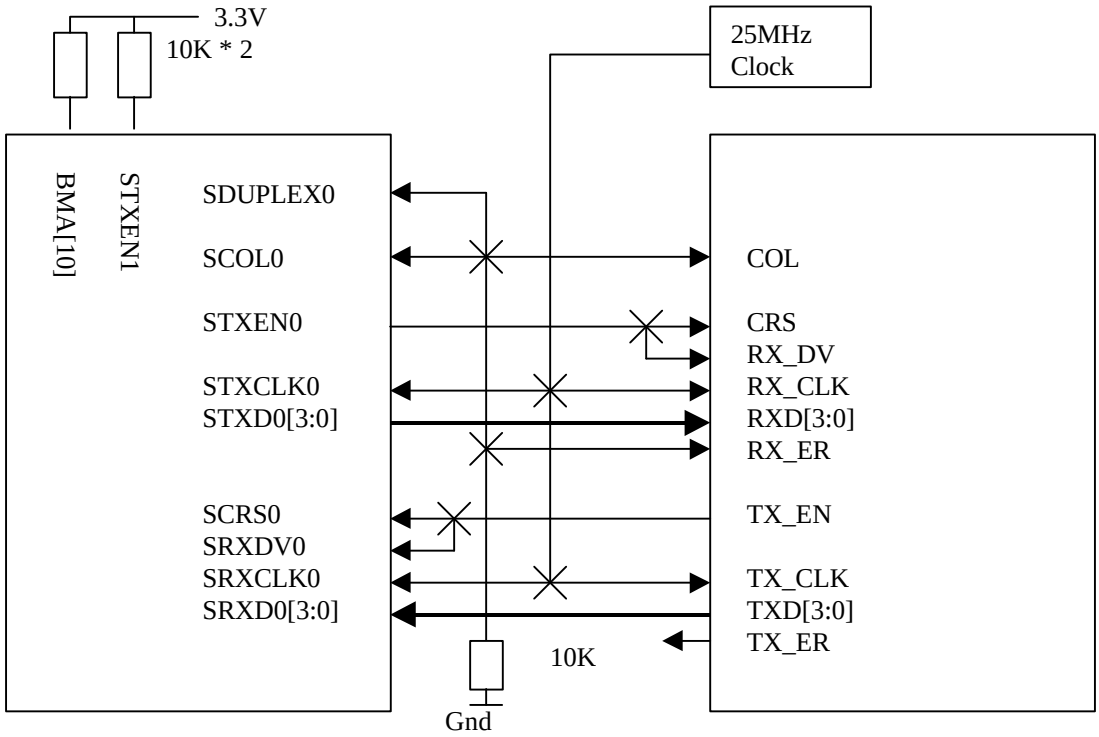
RP : repeater port SP : switch port

RP0	RP1	RP2	RP3	RP4	RP5	SP0	SP1
18h	19h	1ah	1bh	1ch	1dh	1eh	1fh

The corresponding option setting
/RdPhy_En = 0, WrPhyNo_S = 0, WrPhyStrAddr = 0

B.2 Using MII I/F connects to MAC

There are two ports of AX88872 can connect to MAC type MII interface. For example, Switch Port 0 is illustrated bellow.



Note : 1. The MAC needs to run at fullduplex mode.
2. Care must be taken that the receive side has enough setup and/or hold time
3. Some kind of CPU with embbeded MAC can also refer to this example