Integrated Device Technology, Inc.

128K x 8 SRAM WITH LATCHED/ BUFFERED ADDRESS LINES, REGISTERED $DATA_{IN}$ LINES AND LATCHED/BUFFERED $DATA_{OUT}$ LINES

IDT7M822

FEATURES:

- Latched and buffered address lines
- Registered input data lines
- Latched and buffered output data lines
- Separate I/O
- High-speed access time:
  - Military temperature range: 55ns (max.)
  - Commercial temperature range: 45ns (max.)
- 20MHz read/write cycle time

DESCRIPTION:

The IDT7M822 is a 128K x 8 RAM with latched address, registered $DATA_{IN}$ and latched $DATA_{OUT}$ lines. The address and $DATA_{IN}$ latches have independent latch enables (LE) allowing the latch to be used as a buffer by connecting its Latch Enable LE to V_{CC}.

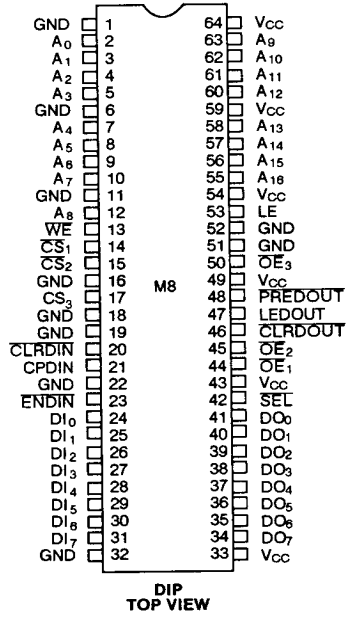
Address, Write Enable ($\overline{WE}$) and the three Chip Select ($\overline{CS}$) lines are controlled by LE. When LE is high, the address latches and decoder are transparent or in the buffer mode. All address, $\overline{CS}$ and $\overline{WE}$ data that meets the specified set-up time will be latched when LE goes low.

$DATA_{IN}$ is controlled by its own clock, CPDIN. When ENDIN (clock enable) is asserted, all $DATA_{IN}$ data that meets the specified set-up time requirements will be registered on the rising edge of CPDIN. $\overline{CLRDIN}$ is an asynchronous control that can be used to clear the $DATA_{IN}$ register.

$DATA_{OUT}$ is controlled by its own enable, LEDOUT. With this line in the high state, the latch is in the transparent or buffer mode. Data out of the RAM array that meets the set-up time requirements will be latched when LEDOUT goes low. $\overline{PREDOUT}$ and $\overline{CLRDOUT}$ are asynchronous controls that can be used to preset or clear the $DATA_{OUT}$ latch. The preset function overrides the clear so that, with both asserted, the latch will be preset. There are three active low output enables for $DATA_{OUT}$. Unless all three of these lines are asserted, the output will be in the high impedance state.

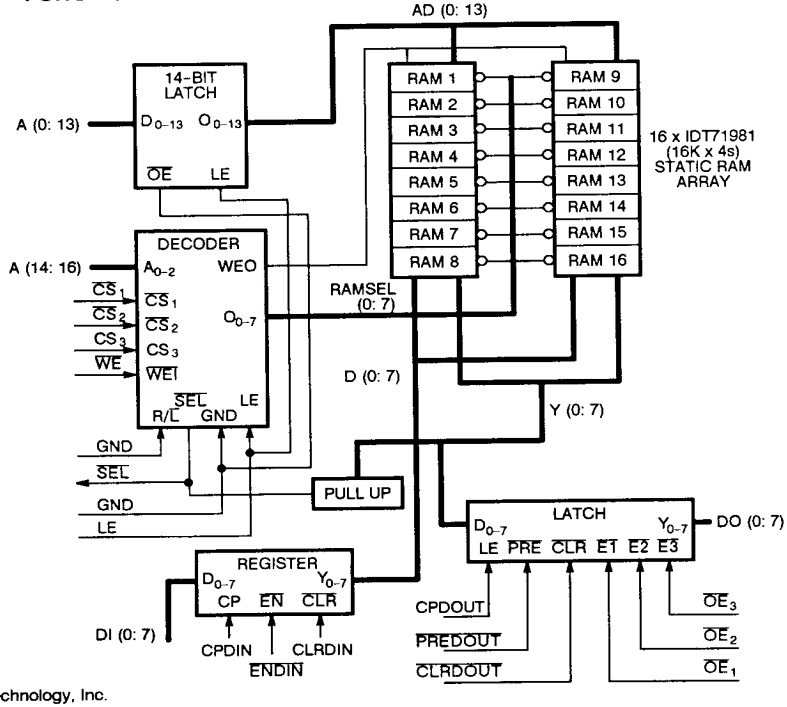
The $\overline{SEL}$ signal is an output that can be used to monitor the state of the internal RAM array output bus.

PIN CONFIGURATION



DIP
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



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AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

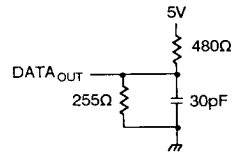

Figure 1. Output Load

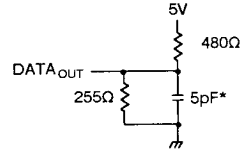

Figure 2. Output Load (for t_{OHZ})

* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, T_A = 0°C to +70°C and -55°C to +125°C)

SYMBOL	PARAMETER	IDT7M822S45 (COM'L. ONLY) MIN.	IDT7M822S45 (COM'L. ONLY) MAX.	IDT7M822S55 MIN.	IDT7M822S55 MAX.	IDT7M822S70 MIN.	IDT7M822S70 MAX.	UNIT
READ CYCLE(1)								
t_{AA}	Address, $\overline{CS}$ Access Time	–	45	–	55	–	70	ns
t_{ADS}	Address, $\overline{CS}$ to LE Set-up Time	2	–	2	–	2	–	ns
t_{ADH}	Address, $\overline{CS}$ from LE Hold Time	2	–	2	–	3	–	ns
t_{LEDO}(2)	$DATA_{OUT}$ Latch from Address, $\overline{CS}$	–	36	–	40	–	55	ns
t_{OE}	$\overline{OE}$ to Data Valid	–	8	–	9	–	15	ns
t_{OHZ}(3)	$\overline{OE}$ to High Z	–	7	–	9	–	15	ns
WRITE CYCLE								
t_{AW}	Address, $\overline{CS}$ to End of Write	31	–	45	–	55	–	ns
t_{WP}	Write Pulse Width	27	–	35	–	45	–	ns
t_{ADS}	Address, $\overline{CS}$ to LE Set-up Time	2	–	2	–	2	–	ns
t_{ADH}	Address, $\overline{CS}$ from LE Hold Time	2	–	2	–	3	–	ns
t_{EDS}	$DATA_{IN}$ Clock Enable to Clock Set-up Time	3	–	3	–	3	–	ns
t_{EDH}	$DATA_{IN}$ Clock Enable from Clock Hold Time	0	–	0	–	2	–	ns
t_{DS}	$DATA_{IN}$ to $DATA_{IN}$ Clock Set-up Time	3	–	3	–	5	–	ns
t_{DH}	$DATA_{IN}$ from $DATA_{IN}$ Clock Hold Time	2	–	2	–	3	–	ns
t_{CDW}	$DATA_{IN}$ Clock to End of Write Cycle	27	–	31	–	40	–	ns

NOTES:
1. $\overline{WE}$ Must be high for read cycles.
2. Latch Enable signal arriving after this maximum will delay overall access time (t_{AA}).
3. Transition is measured -200mV from steady state voltage with specified loading in Figure 2.

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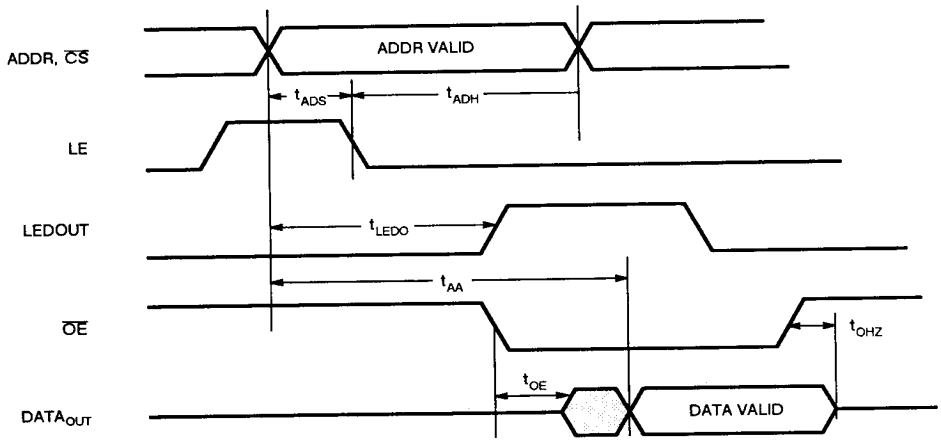
TIMING WAVEFORM OF READ CYCLE



TIMING WAVEFORM OF WRITE CYCLE