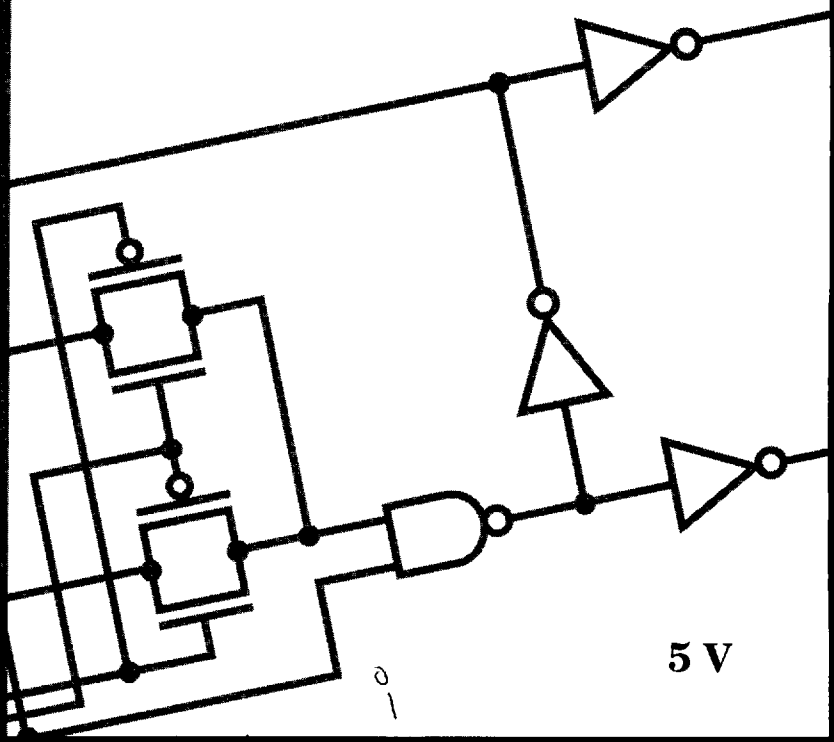
LSI LOGIC

LCA300K Gate Array 5 Volt Series Products Databook

October 1993



5 V

Preface

The LCA300K Gate Array Product Series Databook is written for logic and system designers who wish to use LSI Logic's 0.6-micron gate array products to create high-performance designs. It is assumed that users of this manual are familiar with LSI Logic's MDE®/C-MDE™ design sequences from having attended LDS® Core, Design Methodology, and Compacted Array™ design classes at one of LSI Logic's design resource centers.

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Chapter 1
LCA300K Gate Array Product

1.1 Introduction

This databook contains design information for the 0.6-micron gate array products. These products are designed using the LCA300K/LCA310K Gate Array series product family libraries. This databook also contains performance information for each of the libraries' internal macrocells (Chapter 2). The timing data given on the macrocell's data page are calculated using LSI Logic's modeling enhancement software tool called CHARMS (CHARacterization and Modeling System), which calculates delay values that closely match actual silicon performance.

The remaining chapters of this databook provide information on the following system building blocks: '

- 5 V and 3.3 V I/O Macrocells (Chapter 3)
- Logic Functions (Block Synthesis) and Memories (Memory Compiler) (Chapter 4)
- Macrofunctions (Chapter 5)
- System Building Blocks (Megafunctions) and CoreWare™ Microprocessors (Chapter 6)

1.2 Features of the 0.6-Micron Array-Based Products

The 0.6-micron array-based products have the following features:

- a 0.6-micron drawn gate length (0.45-micron effective channel length) HCMOS process technology
- functional equivalence to LSI Logic's 1.0- and 0.7-micron array-based products
- compatibility with LEA300K Embedded Array® ASICs product family library and LCB300K Cell-Based ASICs product family library
- masterslices that offer from 10,000 to 500,000 usable gates complexity and user-defined memory capable of up to 96 Kbits of SRAM and 348 Kbits of ROM
- 2- or 3-layer metal interconnect options

In addition, the product family libraries used in the 0.6-micron array-based products provide architectural solutions for system designs by including complex industry-standard megafunctions. The integration of these functions raises reliability by reducing system component count and increases performance by reducing the use of PC board and package interconnect.

The product family libraries offer I/O pad counts of up to 888 (depending on the number of required power pins). Unidirectional, bidirectional, and 3-state output buffers are available with design-specific options for pull-up or pull-down resistors, variable drive strengths, and slew rate control. Pseudo ECL I/O buffers furnish an ECL-level interface without the cost and power penalties of ECL, and NTL (NMOS transceiver logic) I/O buffers reduce noise while switching at data rates of up to 175 MHz. Both 5 V and 3.3 V I/O buffers are available to enable flexibility in designing low-power systems.

1.3 Product Family Library Description

This section describes the LCA300K/LCA310K Gate Array Series. LCA300K has 2-layer metal interconnect; LCA310K has 3-layer metal interconnect.

These product families use LSI Logic's Gate Array architecture, which is an array core filled with potentially active transistors connected through either 2- or 3-layers of metal interconnect.

LCA300K Gate Array Series, 2-Layer Metal

The LCA300K Gate Array Series with 2-layer metal interconnect offers I/O pad counts of up to 668 in standard packages and up to 888 with TAB (Tape Automated Bonding) in COT (Chip-On-Tape) packages. The 2-layer metal series is ideal for applications that are limited by the number of required I/O buffers but are not pushing the limits of gate capacity.

Table 1.1 shows the products available in the LCA300K 2-layer metal series.

Table 1.1
LCA300K 2-Layer
Metal Products

Device Name	*Die Code*	*Total Gates*	*Usable Gates/% Utilization*				*I/0 Pad Count (by pitch, in mil)*			
			Nominal		*High*		*3.3*	*4.1*	*4.4*	*4.9*
LC300 023	3A02	22,518	7,900	35%	10,800	48%	168	136	128	120
LC300 030	3A03	30,268	10,600	35%	14,500	48%	192	160	152	136
LC300 036	3A04	35,904	12,600	35%	16,900	47%	208	168	160	144
LC300 053	3A05	52,824	18,500	35%	24,300	46%	240	200	192	168
LC300 069	3A07	69,012	24,200	35%	31,100	45%	280	232	216	192
LC300 097	3A10	96,768	33,900	35%	42,600	44%	328	264	248	224
LC300 123	3A12	122,850	43,000	35%	52,800	43%	368	296	280	248
LC300 153	3A15	152,764	53,500	35%	64,200	42%	408	328	312	280
LC300 185	3A19	185,136	64,800	35%	75,900	41%	448	360	344	304
LC300 236	3A24	235,800	82,500	35%	96,700	41%	496	400	376	336
LC300 317	3A32	317,376	111,100	35%	130,100	41%	576	464	440	392
LC300 415	3A41	414,816	145,200	35%	165,900	40%	656	528	496	440
LC300 563	3A56	562,950	197,000	35%	225,200	40%	760	616	576	512
LC300 784	3A78	783,920	274,400	35%	313,600	40%	896	720	680	600

LCA310K Gate Array Series, 3-Layer Metal

The LCA310K Gate Array Series with 3-layer metal interconnect offers the same pad counts and buffer options as LCA300K designs, but LCA310K has a higher gate capacity.

Table 1.2 shows the products available in the LCA310K 3-layer metal series.

Table 1.2
LCA310K 3-Layer
Metal Products

Device Name	Die Code	Total Gates	Usable Gates/% Utilization Nominal		High		I/0 Pad Count (by pitch, in mil) 3.3	4.1	4.4	4.9
LC310 023	3A02	22,518	10,800	48%	15,800	70%	168	136	128	120
LC310 030	3A03	30,268	14,500	48%	20,900	69%	192	160	152	136
LC310 036	3A04	35,904	17,200	48%	24,100	67%	208	168	160	144
LC310 053	3A05	52,824	25,400	48%	34,900	66%	240	200	192	168
LC310 069	3A07	69,012	33,100	48%	44,900	65%	280	232	216	192
LC310 097	3A10	96,768	46,400	48%	61,900	64%	328	264	248	224
LC310 123	3A12	122,850	59,000	48%	77,400	63%	368	296	280	248
LC310 153	3A15	152,764	73,300	48%	94,700	62%	408	328	312	280
LC310 185	3A19	185,136	88,900	48%	112,900	61%	448	360	344	304
LC310 236	3A24	235,800	113,200	48%	141,500	60%	496	400	376	336
LC310 317	3A32	317,376	152,300	48%	187,300	59%	576	464	440	392
LC310 415	3A41	414,816	199,100	48%	244,700	59%	656	528	496	440
LC310 563	3A56	562,950	270,200	48%	326,500	58%	760	616	576	512
LC310 784	3A78	783,920	376,300	48%	454,700	58%	896	720	680	600

1.4 Overview of LSI Logic Library Options

LSI Logic has developed libraries to meet a wide range of design needs:

- Standard Library
- 5 V, 3.3 V, and Mixed-Voltage Applications
- C-MDE and Third-Party Design Environments

Standard Library

The macrocells contained in this book comprise the LCA300K standard library. The majority of these macrocells are characterized up to 64 standard loads; however, this library also contains cells characterized up to 16 and 256 standard loads. Because these cells are characterized using CHARMS (which is described in Section 1.7 below), LSI Logic is able to calculate delay values that more accurately match silicon performance at both chip and system levels.

5 V, 3.3 V, and Mixed-Voltage Applications

The standard library's macrocells and I/O buffers are available for 5 V and 3.3 V power supply levels in the IO300K library. The 3.3 V option offers lower power dissipation, interface compatibility with 3.3 V buses and components, fewer design constraints on the number of simultaneously switching output buffers, and less ground-bounce noise. (3.3 V I/Os are not TTL-compatible.) Refer to Chapter 3 for more information about 3.3 V design.

C-MDE and Third-Party Design Environments

LSI Logic offers its libraries for use with its C-MDE design system. In addition it offers reconfigured versions of the standard library that are compatible with third-party design tools. Contact your applications engineer for information on available libraries.

1.5 Designing for Test

LSI Logic provides the design engineer with the following test tools:

- Test Builder for internal scan testing (fully compliant with IEEE 1149.1 methodology)

  Test Builder is an advanced scan design environment that reduces time-to-market for ASIC-based systems. Scan Chain Synthesis achieves predictable test results by automatically inserting the most optimized scan path. Scan ATPG improves the quality of test vectors by achieving over 99 percent stuck-at-fault coverage. High fault coverage will raise the end user's confidence in IC quality and minimize the expenses of field failures. Test Builder supports edge-sensitive and level-sensitive scan methodologies, including testing of RAMs, ROMs, and megafunctions.

- Automatic JTAG Builder for inserting test access port and boundary-scan architecture (IEEE 1149.1 standard)

  Automatic JTAG Builder inserts and interconnects JTAG logic to system logic. It also automatically generates the BSDL description of the boundary scan circuit, as well as a full set of test vectors for boundary scan logic. High fault coverage at the system level using boundary scan will raise the end user's confidence in product quality and minimize the expenses of field failures.

Automatic JTAG Builder supports mandatory instructions (such as BYPASS, SAMPLE/PRELOAD, and EXTEST) as well as optional instructions (such as RUNBIST, INTEST, CLAMP, HIGHZ, and other user-defined instructions). This tool supports LSI Logic's boundary scan cells or user-defined cells, and I/O buffers with built-in multiplexer for reducing delays due to boundary scan cells.

- Accelerated fault simulation

  Accelerated fault simulation is fully integrated into the C-MDE simulation environment using the XP family of Zycad hardware accelerators at LSI Logic's design centers. This family can simulate a design of 1,000,000 gates, allowing a user to concurrently run thousands of faults per pass, thus performing fault simulation in days rather than months using a serial algorithm. LSI Logic provides statistical as well as deterministic fault simulation for end users.

Contact your applications engineer for more information about test methodology and tools.

1.6 Propagation Delays

Propagation delays are primarily determined by cell drive capability and loading, which consists of cell input capacitances and wiring. However, for a reliable operation of a chip in a system environment, a designer should also take into account the following three critical variables that affect the delays in an integrated circuit: 1) process variation, 2) supply voltage, and 3) on-chip junction temperature, where junction temperature is calculated using chip power dissipation and thermal resistance to the ambient temperature of the package being used.

Process variation is introduced because of the limitations of manufacturing equipment and processes. Hence this variation could change the physical dimensions of some critical parameters—such as gate oxide, gate length, etc.— which consequently affect the electrical characteristics of devices, either increasing or slowing performance as compared to that for a nominal condition.

Voltage and temperature variables are introduced because of the system environment. Increase in voltage reduces the propagation delay, whereas increase in temperature increases the propagation delay. Three environments are accepted as standard in the industry: commercial, industrial, and military.

Because of the unknown process variation and a need for designing chips in a wide range of voltage and temperature environments, designers must simulate their designs under all three conditions: nominal, worst-case, and best-case.

The following sections discuss these factors and give equations for computing best- and worst-case propagation delays.

Table 1.3 defines the symbols used in propagation delay calculations.

Table 1.3 Propagation Delay Symbols

Symbol	*Definition*
K_{pmin}	Minimum processing factor
K_{pmax}	Maximum processing factor
K_{Twc}	Worst-case temperature factor
K_{Tbc}	Best-case temperature factor
K_{Vbc}	Best-case voltage factor
K_{Vwc}	Worst-case voltage factor
K_{bc}	Best-case factor
K_{wc}	Worst-case factor
T_j	Junction temperature
t_{max}	Maximum time
t_{min}	Minimum time
t_{nom}	Nominal time
t_pLH	Propagation delay from low to high
t_pHL	Propagation delay from high to low
VDD	Supply voltage

Table 1.4 shows the delay derating factors for process (K_p), voltage (K_V), and temperature (K_T).

Table 1.4 K_p, K_V and K_T Derating Factors

Environment	*Commercial*			*Industrial*			*Military*		
	K_p	K_V	K_T	K_p	K_V	K_T	K_p	K_V	K_T
Best-Case	0.70	0.94	0.94	0.7	0.94	0.83	0.7	0.87	0.79
Nominal	1	1	1	1	1	1	1	1	1
Worst-Case	1.4	1.07	1.12	1.4	1.07	1.15	1.4	1.13	1.26

Interconnect Routing

The wire lengths used between different-sized blocks of logic affect propagation delay. The matrixes in Table 1.5 and Table 1.6 show the equivalent standard load values for different sizes of block areas using 2-layer and 3-layer metal interconnect, respectively. Wire loading for 3-layer metal is generally lower than for 2-layer metal (for a given fanout and block size) because of shorter statistical wirelengths as well as lower average unit capacitance. These values are based on relative capacitive loading and are used in wire length estimates.

In these tables, the following parameters are used:

- The Size column (at left) shows the dimensions of the physical block in mm.
- The fanout values (F.O.) (at the top of the matrix) represent fanout (the number of pins on a net minus 1).
- The numbers in the Slope column (at right) represent the linear ratio of the standard load value over the value of F.O.
- The intercept value, which is the intrinsic standard load of the cell (the loading without considering the loading that would be added by wire) is always 0. It equals the y-axis intercept of the fanout curve vs. the standard load.
- The values in the body of the matrix, for each block size and F.O. value, are the number of equivalent standard loads of the wire length used within the given block size.

Table 1.5
Equivalent Standard Load Matrix for
2-Layer Metal Interconnect

Size of die (mm)	Fanouts (F.O.—number of equivalent standard loads)										Intercept=0	
	1	2	3	4	5	6	7	8	16	32	64	Slope
0.5x0.5	0.78	1.55	2.33	3.10	3.88	4.65	5.43	6.20	12.40	24.81	49.61	0.775
1.0x1.0	0.82	1.63	2.45	3.26	4.08	4.89	5.71	6.52	13.04	26.08	52.17	0.815
2.0x2.0	0.89	1.79	2.68	3.58	4.47	5.37	6.26	7.16	14.32	28.64	57.27	0.895
3.0x3.0	0.97	1.95	2.92	3.90	4.87	5.85	6.82	7.80	15.59	31.19	62.38	0.975
4.0x4.0	1.05	2.11	3.16	4.22	5.27	6.33	7.38	8.44	16.87	33.74	67.48	1.054
5.0x5.0	1.13	2.27	3.40	4.54	5.67	6.81	7.94	9.07	18.15	36.29	72.59	1.134
6.0x6.0	1.21	2.43	3.64	4.86	6.07	7.28	8.50	9.71	19.42	38.85	77.70	1.214
7.0x7.0	1.29	2.59	3.88	5.18	6.47	7.76	9.06	10.35	20.70	41.40	82.80	1.294
8.0x8.0	1.37	2.75	4.12	5.49	6.87	8.24	9.61	10.99	21.98	43.95	87.91	1.374
9.0x9.0	1.45	2.91	4.36	5.81	7.27	8.72	10.17	11.63	23.25	46.51	93.01	1.453
10.0x10.0	1.53	3.07	4.60	6.13	7.67	9.20	10.73	12.26	24.53	49.06	98.12	1.533
11.0x11.0	1.61	3.23	4.84	6.45	8.06	9.68	11.29	12.90	25.81	51.61	103.22	1.613
12.0x12.0	1.69	3.39	5.08	6.77	8.46	10.16	11.85	13.54	27.08	54.16	108.33	1.693
13.0x13.0	1.77	3.54	5.32	7.09	8.86	10.63	12.41	14.18	28.36	56.72	113.44	1.772
14.0x14.0	1.85	3.70	5.56	7.41	9.26	11.11	12.97	14.82	29.64	59.27	118.54	1.852
15.0x15.0	1.93	3.86	5.80	7.73	9.66	11.59	13.52	15.46	30.91	61.82	123.65	1.932

Table 1.6
Equivalent Standard Load Matrix for
3-Layer Metal Interconnect

Size of die (mm)	Fanouts (F.O.—number of equivalent standard loads)										Intercept=0	
	1	2	3	4	5	6	7	8	16	32	64	Slope
0.5x0.5	0.75	1.50	2.25	3.00	3.76	4.51	5.26	6.01	12.02	24.04	48.08	0.751
1.0x1.0	0.79	1.58	2.37	3.16	3.95	4.74	5.53	6.32	12.64	25.28	50.55	0.790
2.0x2.0	0.87	1.73	2.60	3.47	4.34	5.20	6.07	6.94	13.87	27.75	55.50	0.867
3.0x3.0	0.94	1.89	2.83	3.78	4.72	5.67	6.61	7.56	15.11	30.22	60.45	0.944
4.0x4.0	1.02	2.04	3.07	4.09	5.11	6.13	7.15	8.17	16.35	32.70	65.39	1.022
5.0x5.0	1.10	2.20	3.30	4.40	5.50	6.59	7.69	8.79	17.59	35.17	70.34	1.099
6.0x6.0	1.18	2.35	3.53	4.71	5.88	7.06	8.23	9.41	18.82	37.64	75.29	1.176
7.0x7.0	1.25	2.51	3.76	5.01	6.27	7.52	8.78	10.03	20.06	40.12	80.24	1.254
8.0x8.0	1.33	2.66	3.99	5.32	6.65	7.99	9.32	10.65	21.30	42.59	85.18	1.331
9.0x9.0	1.41	2.82	4.22	5.63	7.04	8.45	9.86	11.27	22.53	45.07	90.13	1.408
10.0x10.0	1.49	2.97	4.46	5.94	7.43	8.91	10.40	11.88	23.77	47.54	95.08	1.486
11.0x11.0	1.56	3.13	4.69	6.25	7.81	9.38	10.94	12.50	25.01	50.01	100.03	1.563
12.0x12.0	1.64	3.28	4.92	6.56	8.20	9.84	11.48	13.12	26.24	52.49	104.97	1.640
13.0x13.0	1.72	3.44	5.15	6.87	8.59	10.31	12.02	13.74	27.48	54.96	109.92	1.718
14.0x14.0	1.79	3.59	5.38	7.18	8.97	10.77	12.56	14.36	28.72	57.43	114.87	1.795
15.0x15.0	1.87	3.74	5.62	7.49	9.36	11.23	13.10	14.98	29.95	59.91	119.82	1.872

Use the following equation to interpolate for load conditions other than those provided in the matrixes:

```
number of                          number of
equivalent standard loads = fanouts    x slope + intercept
```

Supply Voltage and Junction Temperature

Figure 1.1 shows propagation delay variation in two ways:

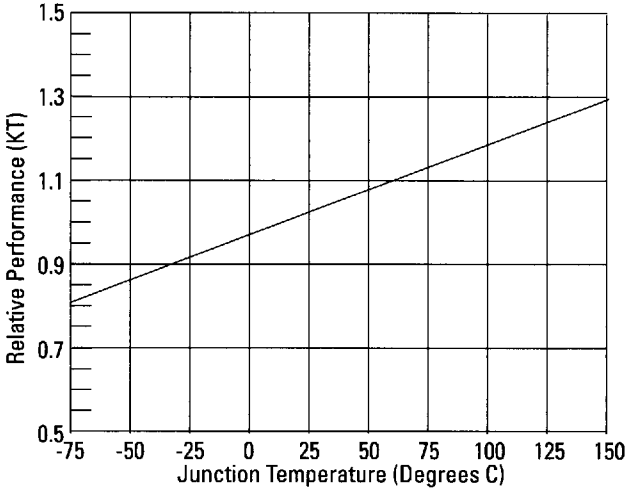
- K_T, which shows the delay variation as a function of on-chip junction temperature (T_j)

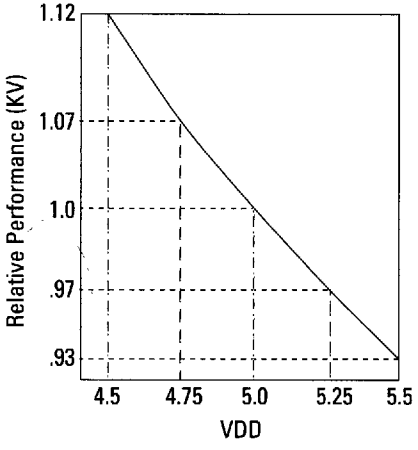
  Junction temperature (the temperature of the die inside the package) is calculated using chip power dissipation and the thermal resistance to the ambient temperature (θ_{ja}) of the package being used. Contact your LSI Logic applications engineer for more information on package thermal performance.

- K_V, which shows the delay variation as a function of supply voltage (V_{DD})

LSI Logic allows for a +40% and -30% variance attributed to all factors, including process ($K_{pmin} = 0.7$, $K_{pmax} = 1.4$).

Figure 1.1
Propagation Delays as a Function of Junction Temperature and Supply Voltage





Propagation Delay

Worst-case propagation delay can be calculated as follows:

$$t_{max} = K_{pmax} \times K_{Twc} \times K_{Vwc} \times t_{nom} = K_{wc} \times t_{nom}$$

where:

$$K_{pmax} = 1.4$$

Best-case propagation delay can be calculated as follows:

$$t_{min} = K_{pmin} \times K_{Tbc} \times K_{Vbc} \times t_{nom} = K_{bc} \times t_{nom}$$

where:

$$K_{pmin} = 0.7$$

1.7 CHARMS Overview

LSI Logic is dedicated to achieving a closer coupling between predicted system timing delay parameters and actual silicon performance. Therefore the cells in the 300K libraries have been modeled using a new engineering software tool that brings circuit simulation accuracy to the delay prediction environment.

This tool, called CHARMS (CHARacterization and Modeling System), provides the following functions:

- extraction of circuit simulator timing information from key parameters (output loading and input ramp time)
- recognition of the effects of switching threshold on timing information
- characterization of cell delays with output loading, input ramp time, and switching-threshold information

Key benefits of CHARMS include 1) the availability of independent characterization variables to account for variation in output loading and input ramp time, and 2) the ability to account for the effect of switching threshold on cell-to-cell delay. Because of these benefits, LSI Logic is able to calculate delay values that more accurately match silicon performance at both chip and system levels.

For more information, refer to the application note "Designing with a CHARMS-Enhanced Library," or contact your applications engineer.

1.8 Clocking and Skew Control

Clocking is one of the most important considerations for the high-speed digital design system. The clock frequency determines the maximum rate of data processing and data transmission. Maximum clock frequency is limited by clock skew, flip-flop setup time, flip-flop delay time, and the delay time of the logic block between any two flip-flop elements.

In advanced integrated circuit designs, clock skew is caused by different interconnection delays due to local buffers and unequal lengths of local interconnect wire. To minimize clock skew in ASICs, LSI Logic has introduced the use of the Phase-Locked Loop circuit (discussed below) and the Balanced Clock-Tree Compiler.

The Balanced Clock-Tree Compiler is based on a multi-level clock distribution scheme that improves ASIC performance by minimizing the clock skew, reducing total clock delay, improving rise and fall times, and reducing silicon area usage by the clock circuitry. For more information about the use of Balanced Clock-Tree Compiler, see the application note "Clock Distribution Schemes for 300K Technologies" and contact your applications engineer.

1.9 Phase-Locked Loop Circuit

A Phase-Locked Loop (PLL) consists of a phase detector, loop filter, and voltage-controlled oscillator (VCO). The PLL synchronizes the on-chip clock with the system clock in both frequency and phase. LSI Logic can, upon request, put its PLL circuitry into a design. The advantages of adding PLL circuitry are

- the minimizing of the effect of clocking skew at system level caused by variations in the process temperature, power supply, interconnects, and routing
- frequency synthesis, which uses the system clock as a base frequency to generate higher frequencies for the internal logic

Contact your applications engineer for more information about phase-locked loop circuits.

1.10 Output Buffer Slew Rate Control

LSI Logic offers the option of slew rate control on output buffers. Using slew rate control allows longer interconnections on a PC board.

The fast rise and fall times of CMOS output buffers can cause system noise and signal overshoot. When a buffer is driving an unterminated line, the maximum allowable length of the line can be determined from the rise or fall time of the output buffer and the round-trip delay of the line. Long transmission lines degrade system performance because of reflections and ringing.

The user can slow down the output edge rate, thereby allowing the use of a longer line, by controlling slew rate. Two slew rates are provided for each type of output buffer (except `b1` and `b2`). Moderate slew rate is designated by the suffix `rp` in the buffer's name; minimum slew rate is designated by the suffix `r`. The selected slew rate depends on design requirements.

A `b4` unidirect output buffer (with a 4 mA output drive strength) has a typical delay of 1.3 ns when loaded with 15 pF. A `b4r` unidirect output buffer (with minimum slew rate) has a typical delay of 2.5 ns. For a typical line delay of 0.055 ns/cm, the maximum allowable length of the signal trace is 11.8 cm for the `b4` and 22.7 cm for the `b4r`.

Table 1.7 shows the minimum rise/fall time in nanoseconds and the maximum interconnection lengths in centimeters for unidirect output buffers with varying slew rates. Longer interconnections will degrade system performance.

Table 1.7 Minimum Rise/Fall Time and Maximum Interconnection Lengths for Output Buffers

Output Buffers	*Min Rise/Fall Time t(ns)*[1]	*Maximum Interconnection Lengths (cm) = t(ns) / 0.055 (ns/cm) / 2*
b1	3.80	34.5
b2	2.60	23.6
b4	1.30	11.8
b4rp	1.60	14.5
b4r	2.50	22.7
b6	1.00	9.1
b6rp	1.20	10.9
b6r	2.00	18.2
b8	0.92	8.4

(Sheet 1 of 2)

Table 1.7 (Cont.) Minimum Rise/Fall Time and Maximum Interconnection Lengths for Output Buffers

Output Buffers	*Min Rise/Fall Time t(ns)*[1]	*Maximum Interconnection Lengths (cm) = t(ns) / 0.055 (ns/cm) / 2*
b8rp	1.10	10.0
b8r	1.40	12.7
b12	0.88	8.0
b12rp	1.10	10.0
b12r	1.20	10.9
b24a	0.88	8.0
b24rpa	1.10	10.0
b24ra	1.20	10.9

(Sheet 2 of 2)

1. 15 pF loading under nominal conditions.

1.11 Custom Buffers

The standard library's buffers may not provide the flexibility necessary to handle the design problems associated with high-performance system designs. To aid in the design process, LSI Logic has developed the following types of custom buffers:

- Delay-Compensated Output Buffers
- NMOS Transceiver Logic (NTL)
- Pseudo ECL (PECL)
- Differential Input Buffer

Contact your applications engineer for information on obtaining these buffers.

Delay-Compensated Output Buffers

System performance can be improved if the buffer delay variance that results from changes in process, temperature, and supply voltage is reduced. The standard 300K output buffer is designed to accommodate delay compensation. Delay compensation is achieved by actively adjusting the output transistor's drive based on process strength and environmental conditions. When this procedure is used, total delay derating for outputs is reduced from 0.64 ns best-case commercial and 1.67 ns worst-case commercial to 0.70 ns best-case commercial and 1.30 ns worst-case commercial.

Control circuitry is used to activate the delay compensated outputs. Approximately 300 standard core logic gates are used to implement the

control circuit. A counter, which is customized for each system clock frequency, is also used. The system clock represents a known "standard" value, which is then compared against an internal delay circuit. The delay value of the internal circuit is dependent upon supply voltage, temperature, and process. The output buffer drive is adjusted based on the outcome of this comparison.

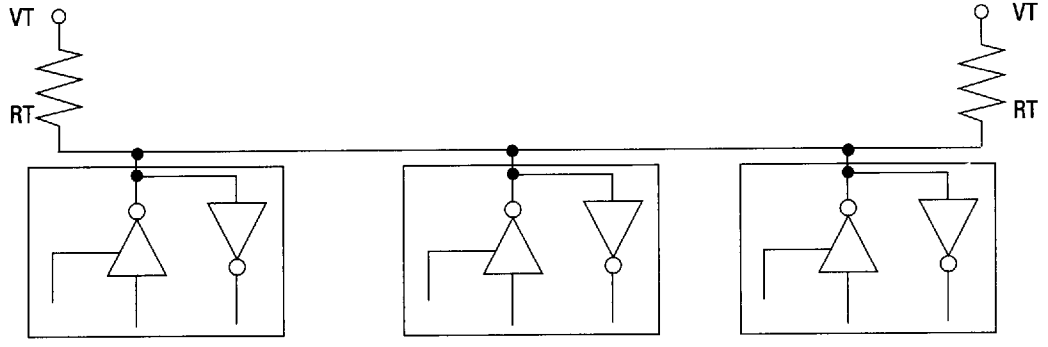
NMOS Transceiver Logic (NTL)

In typical high-performance system designs, conventional CMOS interfaces suffer from overshoot and ringing. CMOS I/Os above 40-50 MHz require careful design and simulation.

NTL is a user-definable, low-voltage swing interface that employs a matched impedance transmission line environment similar to that of ECL. NTL enables high-speed and low-power chip-to-chip communication in excess of 175 Mbits per second. NTL also allows for direct driving of back planes from the ASIC.

NTL uses an open drain output configuration for line driving. In single-driver applications, the transmission line is terminated at the receiver. When multiple drivers are tied to the same transmission line, the line is terminated at both ends to prevent reflections, as shown in Figure 1.2. NTL can be configured for single-end or differential operations.

Figure 1.2
Multi-Driver NTL Backplane Operation

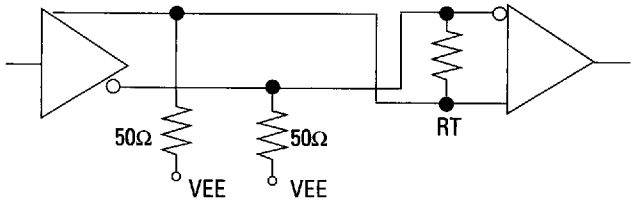


NTL provides an option for GTL—which is co-developed by Xerox, Sun Microsystems, and LSI Logic and is a specific implementation of NTL. GTL typically uses a 1.2 V termination voltage and provides an approximate 800 mV output swing. Vol_{max} is specified at 0.4 V and Voh_{min} is specified at VT or 1.2 V.

Pseudo ECL (PECL)

PECL interfaces are used with high-speed chip-to-chip communication and for backplane transceiver applications. In addition, PECL is used to interface with ECL logic and memory. PECL outputs are externally terminated to VDD minus 2 V. The output swing is centered around VDD minus 1.3 V. PECL can also be configured for differential applications, as shown in Figure 1.3. The PECL output buffer is designed for high-performance applications supporting clock rates in excess of 175 MHz.

Figure 1.3 Differential PECL Operation



Differential Input Buffer

LSI Logic's differential input buffer is used to accept signals from a variety of high-performance interface technologies, including PECL and NTL. When provided with a reference voltage, the input buffer operates in the single-end mode. The buffer is capable of accepting signal swings down to Vref +/- 50 mV.

1.12 Packaging Overview

LSI Logic offers the following industry-standard and custom plastic and ceramic packages for the LCA300K product family library: Dual In-Line Packages, Leaded and Leadless Chip Carriers, Pin Grid Arrays, Plastic Ball Grid Arrays, Quad Flat Packs, Chip-On-Tape, Metal Quad Flat Packs, and Thin Quad Flat Packs.

Refer to LSI Logic's *Package Selector Guide* for a complete description of package data and characteristics. The guide provides electrical and thermal information, mechanical drawings and dimensions of the package, and external pin to internal die cavity pad mapping for each available package. To aid in board layout, detailed drawings of specific packages are available upon request.

1.13 Factors Affecting Power and Ground

This section describes the rules that govern the use of power and ground buses for the LCA300K product.

Types of power and ground buses are listed below:

- Primary power and ground buses
  - VDD, a power bus for output/bidirectional drivers and clock buffers
  - VSS, a ground bus for output/bidirectional drivers and clock buffers
  - VDD4, a power bus for I/O cells whose supply voltage is other than that of the core logic
- Internal logic ground, and input receiver power and ground buses
  - VDD2, a power bus for internal logic and input receivers
  - VSS2, a ground bus for internal logic and input receivers

Each design must be evaluated to determine the required number and location of power and ground pads. The total number of power and ground pads a design requires (VSS/VDD and VSS2/VDD2) is a function of:

- for VSS/VDD
  - the number, types, and locations of output/bidirectional drivers and clock drivers
  - package inductance (Single-layer packages require more pad pairs.)
  - the total load capacitance
  - the number of simultaneously switching outputs (SSO) in the design

➤ ***Note:*** The design engineer should consult LSI Logic's application support for how to implement the full set of rules for VSS/VDD pad requirements for a particular design.

- for VSS2/VDD2
  - gate utilization, percentage of simultaneously switching internal gates, and operating frequency
  - number and location of differential input buffers (see below)
  - memories

General Requirements for Differential Input Receivers

Differential input receivers draw static current. Each 36 differential input receivers require one pair of VDD2/VSS2 pads.

Guidelines for Internal Power and Ground Bus (VDD2/VSS2)

VDD2/VSS2 provide a power/ground bus for the design's internal logic. The size and operating characteristics of the internal logic array determines VDD2/VSS2 pad requirements.

Unlike other VDD/VSS pad pairs, VDD2/VSS2 pad requirements must be calculated for each side of the die.

Follow these guidelines for calculating the required total number of VDD2/VSS2 pads for the die:

- The total number of VDD2/VSS2 pads required in any design is determined by the quantity and speed of internal switching gates. Use the following equation to calculate the required number of VDD2/VSS2 pads for each side:

$$\text{number of VDD2/VSS2 pads/side} = \frac{G_U \times P_{GS} \times S_P \times 1.6e^{-5}}{4}$$

where:

G_U is the number of used gates.

P_{GS} is the percent of gates switched.

S_P is the operating frequency in MHz.

➤ ***Note:*** At least one VSS2/VDD2 pad pair must be used; however, it is recommended that each design use at least one VSS2/VDD2 pad pair per side.

Rounding Off for VSS2/VDD2 Calculations

Use the following rule to round off calculations for the required number of VSS2/VDD2 pad pairs. If a power or ground calculation results in a number that is not an integer, then round off according to the following rules:

- If the calculated fraction is < 0.1, round off to the nearest integer. For example, if n = 3.1, use 3 pads.
- If the calculated fraction is > 0.1, round off to the next higher integer. For example, if n = 3.2, use 4 pads.

1.14 Estimating Switching Power Consumption

Before selecting a package, it is important to estimate the switching power consumption of the die accurately. For example, an inverter switches from output 0 to output 1, but before the switching occurs, the NMOS transistor is on and the PMOS transistor is off. When the input switches from 1 to 0, a short period of time exists when both transistors are turned on—which means that the dc current path from power to ground is not included in the switching power estimation. The switching power occurs when the NMOS transistor is turned off, the PMOS transistor is turned on, and the current from the PMOS transistor charges up the external capacitive load. This switching power is described by the following equation:

$$P = \left(\frac{1}{2}\right) \times C \times V^2 \times \mathrm{f}$$

where:

P is the ac switching power.

C is the capacitive load.

V is the voltage change of the capacitive load.

f is the operating frequency.

When calculating capacitive load, you must take into account the input capacitive load and the wiring capacitive load. In submicron technologies, wire capacitance makes up a significant percentage of the total load.

Use the form on the following page to estimate switching power consumption of the die. The form assumes the following:

- Most gates inside the die switch one gate every three to five clock cycles. A gate, in this case, is defined as a two-input NAND gate with four transistors.
- The average driver inside a macrocell drives 1.5 standard loads.
- The value for average pins per net is 3.2.
- The average wire length is 0.5 mm.
- The average flip-flop of a macrocell has ten gates. The equation to calculate a flip-flop's power uses three types of drivers: clock, datapath, and output.
- Macrocells that are not flip-flops are assumed to have one output cell.

Estimating Switching Power Consumption Form

Basic Switching Power Equation: $P = fCV^2(1/2)$

Data Needed:

G = Total Number of Gates _____

A = Total Number of Macrocells _____

P = Total Number of Flip-Flops _____

S = Percentage of Flip-Flops on System Clock _____%

f = System Frequency (MHz) _____

B = Total Number of Outputs & Bidirects _____

L = Average Chip Output Capacitive Load (pF) _____

H = Height of Clock Trunk (cm) (@size of die) _____

Data Given:

For 0.6m: Cin = 0.042pF, Cout = 0.030pF, Cwire = 0.13pF/mm

Clock Trunk Cap. = Q × Flip-Flops × die width in cm

Q = 0.04pF/cm/FF for over 500 F/F, Q = 0.08pF/cm/FF for 500 or fewer F/F

Assumptions:

Average gate inside macrocell drives 1.5 loads

Average input load is 1.5; non-F/F macrocells have one output each

Average pins/net is 3.2,
3.2 - 1driver = 2.2 fanout × 1.5 loads = 3.3 loads/output

Average wire = .5mm

Average gate switches on 30% of cycles

Average flip-flop = 10 gates (including passive transmission gates),
internal F/F clock = 2 gates w/FO = 2, switching twice/cycle,
average flip-flop datapath = 5.5 gates,
20% of flip-flops use both Q and QN

Calculations:

M = Total Random Output Stages = (A - P) × 1 _____

N = Total Random Internal Stages = G - M - 10P _____

J = System Clocked Flip-Flops = P × 5% _____

K = Other Flip-Flops = P - J _____

Mp = .3M[Vdd2(Cout + 3.3Cin + .5Cwire)f/2] _____

Np = .3N[Vdd2(Cout + 1.5Cin)f/2] _____

Hp = 2[Vdd2(Cout + JCin + HJQ)f/2] _____

Jp = 4J[Vdd2(Cout + 2Cin)f/2]
+ 1.7J[Vdd2(Cout + 1.5Cin)f/2]
+ .36J[Vdd2(Cout + 3.3Cin + .5Cwire)f/2] _____

Kp = 1.2K[Vdd2(Cout + 2Cin)f/2]
+ 1.7K[Vdd2(Cout + 1.5Cin)f/2]
+ .36K[Vdd2(Cout + 3.3Cin + .5Cwire)f/2] _____

Bp = .3B[Vdd2(L)f/2] _____

Ptot = Total Dynamic Pwr = Mp + Np + Hp + Jp + Kp + Bp _____

1.15 DC Characteristics

Table 1.8 lists DC characteristics for the 0.6-micron gate array product. The data are specified at VDD = 5V ± 10% (VDD = 3.3 V ± 10% for low voltage option) for junction temperature over the specified temperature range.[1]

Table 1.8
DC Characteristics

Symbol	*Parameter*	*Condition*	*Min*	*Typ*	*Max*	*Unit*
VIL	Voltage input LOW TTL inputs CMOS levels				 0.8 0.2 VDD	V
VIH	Voltage input HIGH TTL inputs (Com/Ind/ Mil temp range) TTL Schmitt trigger inputs (Ind/Mil temp range) CMOS levels		 2.0 2.25 0.7 VDD			 V V V
VT	Switching threshold	TTL CMOS		1.5 2.5		V V
VT+	Schmitt trigger, positive-going threshold	CMOS TTL		1.77 2.0	2.0 2.25	V V
VT-	Schmitt trigger, negative-going threshold	CMOS (5 V) CMOS (3.3 V) TTL	1.0 0.8 0.8	1.5 1.04 1.04		V V V
	Hysteresis, Schmitt trigger	CMOS VIL to VIH TTL VIL to VIH	1.0 0.4	1.5 0.8		V
IIN	Input current, CMOS, TTL Inputs Inputs with pulldown resistors (5 V) Inputs with pulldown resistors (3.3 V) TTL inputs and inputs with pullup resistors (5 V) TTL inputs and inputs with pullup resistors (3.3 V)	VIN = VDD or VSS VIN = VDD VIN = VDD VIN = VSS VIN = VSS	-10 35 35 -35 -35	±1 115 -115 -115 -115	10 222 138 -214 -131	µA µA µA µA µA

Table 1.8 (Cont.)
DC Characteristics

Symbol	*Parameter*	*Condition*	*Min*	*Typ*	*Max*	*Unit*
VOH	Voltage output HIGH	Commercial and Military				
	Type B1	IOH = -1 mA	2.4			V
	Type B2	IOH = -2 mA	2.4			V
	Type B4	IOH = -4 mA	2.4			V
	Type B6	IOH = -6 mA	2.4			V
	Type B8	IOH = -8 mA	2.4			V
	Type B12[2]	IOH = -12 mA	2.4			V
VOL	Voltage output LOW	Commercial and Military				
	Type B1	IOL = 1 mA		0.2	0.4	V
	Type B2	IOL = 2 mA		0.2	0.4	V
	Type B4	IOL = 4 mA		0.2	0.4	V
	Type B6	IOL = 6 mA		0.2	0.4	V
	Type B8	IOL = 8 mA		0.2	0.4	V
	Type B12[2]	IOL = 12 mA		0.2	0.4	V
IOZ	3-State output leakage current	VOH = VSS or VDD	-10	±1	10	µA
IOS	Output short circuit current[3]	VDD = 5.25 V, VO = VDD	37	90	140	mA
		VDD = 5.25 V, VO = VSS	-117	-75	-40	mA
		VDD = 3.45 V, VO = VDD	50	110	182	mA
		VDD = 3.45 V, VO = VSS	-99	-60	-31	mA
IDD	Quiescent supply current	VIN = VDD or VSS	User-Design Dependent			
CIN	Input capacitance	Any Input and Bidirectional Buffers	2.5			pF
COUT	Output capacitance	Any Output Buffer[4]	2.0			pF

1. Military junction temperature range is -55 °C to +150 °C, ±10% power supply (ceramic packages only); industrial junction temperature range is -40 °C to +125 °C, ±5% power supply; commercial junction temperature range is 0 °C to +115 °C, ±5% power supply.
2. Requires two output pads.
3. Type B4 output. Output short circuit current for other outputs will scale.
4. Output using single buffer structure (excluding package).

1.16 How to Read a Data Page

When reading a data page, you need to understand:

- the naming conventions that identify available options. Cell naming conventions are explained at the introduction to each new group of cells (for example, flip-flops or input buffers).

- the timing tables that contain information for each "version" of the cell

  Versions are indicated by the suffix appended to the cell name. These suffixes apply to available options. For example, the data page for `an2` (see Figure 1.4) shows two versions: `an2` and `an2p`. The `p` is the naming convention used to denote the high output drive strength option.

Figure 1.4 shows the `an2` data page. Circled numerals are keyed to the explanations below:

1. The macrocell's name and description are at the top of the page.
2. The coding syntax shows the following:

   Instance name (output list) = cell name* (input list);

   where * represents the available options and/or drive strengths with the same coding syntax.
3. The logic symbol is shown.
4. The schematic is shown.
5. The truth table is shown.
6. The Loading Characteristics table, which gives input loading values in standard loads for each version of the cell, is provided.

   A standard load is a normalized unit of input capacitance, based on the input capacitance of an inverter. One standard load equals 0.041 pF for LCA300K.
7. The AC Characteristics table—which gives gate count, delay paths output transition, propagation delays for various standard loads, and slope and intercept values for each version of the cell—is provided.

   "t_{pLH}" is the propagation delay from low to high.

   "t_{pHL}" is the propagation delay from high to low.

   To calculate propagation delays, use the equations:

   t_{pLH} = number of standard loads × slope value + incpt value

   t_{pHL} = number of standard loads × slope value + incpt value

For flip-flops and latches, a Timing Constraints table—which gives setup time, hold time, and minimum clock pulse width—is provided.

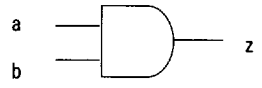
Figure 1.4
Data Page for an2, a
2-Input AND

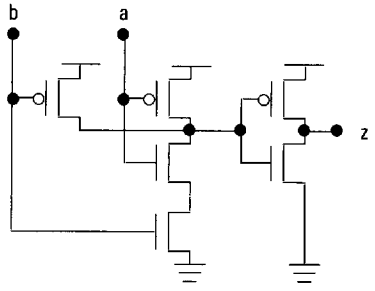
an2
2-Input AND

Name: an2 (1) Description: 2-Input AND

Coding Syntax: z=an2*(a,b) (2)

Logic Symbol: (3) Schematics: (4)





Truth Table: (5)

a	*b*	*z*
0	0	0
0	1	0
1	0	0
1	1	1

Loading Characteristics: (6)

Values stated in standard loads.

Version	*a*	*b*
an2	1.0	1.0
an2p	1.0	1.0

AC Characteristics: (7)

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
an2	2	in_to_z	tpLH	0.30	0.38	0.54	0.71	0.87
			tpHL	0.24	0.29	0.37	0.45	0.53
an2p	2	in_to_z	tpLH	0.29	0.32	0.41	0.49	0.57
			tpHL	0.25	0.27	0.33	0.37	0.41

Chapter 2
LCA300K Internal Macrocells

This chapter contains data pages for gates, internal buffers, flip-flops, and latches. These macrocells are used in LCA300K designs.

The Naming Conventions section at the beginning of each macrocell type describes how to differentiate the different output drive strengths.

Flip-flops and latches also have buffered inputs and buffered outputs.

2.1 Gates

This section contains the data pages for LCA300K gates.

Naming Conventions

A gates root name is given at the top of each data page. High output drive strength is indicated by the suffix `p`. Gate names with no suffix have a standard output drive strength.

For example:

`an2p` has high output drive strength.

`an2` has standard output drive strength.

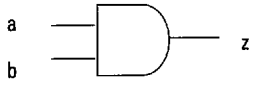
➤ ***Note:*** For the coding syntax, an asterisk following the cell name (for example, `an2*`) is a wildcard symbol for the `p` option, indicating that the data page applies to both high output and standard drive strength configurations.

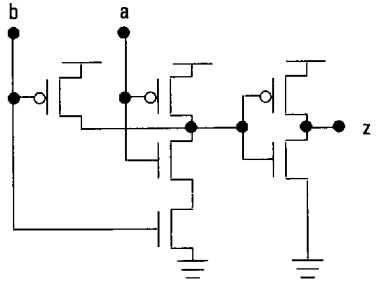
2-Input AND

Name: an2 Description: 2-Input AND

Coding Syntax: z=an2*(a,b)

Logic Symbol: Schematics:





Truth Table:

a	*b*	*z*
0	0	0
0	1	0
1	0	0
1	1	1

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*b*
an2	1.0	1.0
an2p	1.0	1.0

AC Characteristics:

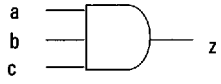
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

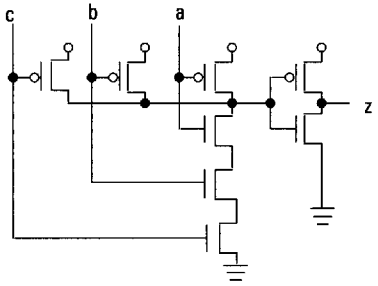
Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
an2	2	in_to_z	tpLH	0.30	0.38	0.54	0.71	0.87
			tpHL	0.24	0.29	0.37	0.45	0.53
an2p	2	in_to_z	tpLH	0.29	0.32	0.41	0.49	0.57
			tpHL	0.25	0.27	0.33	0.37	0.41

Name: an3 Description: 3-Input AND

Coding Syntax: z=an3*(a,b,c)

Logic Symbol: Schematics:





Truth Table:

a	*b*	*c*	*z*
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*b*	*c*
an3	1.0	1.0	1.0
an3p	1.0	1.0	1.0

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

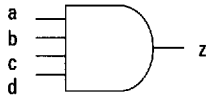
Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
an3	2	in_to_z	tpLH	0.38	0.47	0.64	0.81	0.98
			tpHL	0.28	0.33	0.42	0.50	0.58
an3p	3	in_to_z	tpLH	0.38	0.43	0.52	0.60	0.69
			tpHL	0.28	0.31	0.37	0.41	0.46

an4
4-Input AND

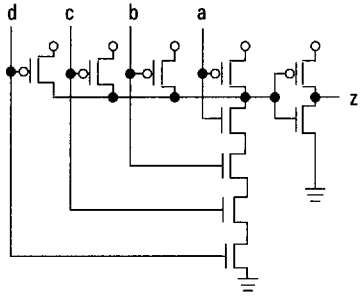
Name: an4 Description: 4-Input AND

Coding Syntax: z=an4*(a,b,c,d)

Logic Symbol:



Schematics:



Truth Table:

a	*b*	*c*	*d*	*z*
0	x	x	x	0
x	0	x	x	0
x	x	0	x	0
x	x	x	0	0
1	1	1	1	1

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*b*	*c*	*d*
an4	1.0	1.0	1.0	1.0
an4p	1.0	1.0	1.0	1.0

AC Characteristics:

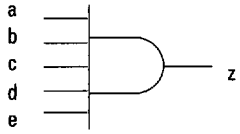
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

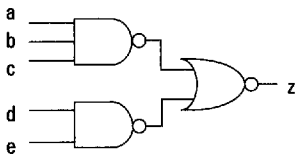
Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
an4	3	in_to_z	tpLH	0.49	0.59	0.76	0.94	1.11
			tpHL	0.31	0.37	0.46	0.55	0.62
an4p	3	in_to_z	tpLH	0.49	0.55	0.65	0.74	0.82
			tpHL	0.31	0.35	0.40	0.46	0.50

Name: an5 Description: 5-Input AND

Coding Syntax: z=an5*(a,b,c,d,e)

Logic Symbol: Schematics:





Truth Table:

a	*b*	*c*	*d*	*e*	*z*
0	x	x	x	x	0
x	0	x	x	x	0
x	x	0	x	x	0
x	x	x	0	x	0
x	x	x	x	0	0
1	1	1	1	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*b*	*c*	*d*	*e*
an5	1.0	1.0	1.0	1.0	1.0
an5p	1.0	1.0	1.0	1.0	1.0

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

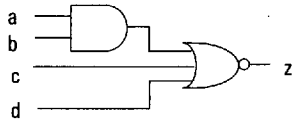
Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
an5	4	in_to_z	tpLH	0.44	0.60	0.91	1.23	1.57
			tpHL	0.27	0.31	0.40	0.48	0.56
an5p	5	in_to_z	tpLH	0.41	0.49	0.65	0.80	0.96
			tpHL	0.29	0.32	0.36	0.41	0.45

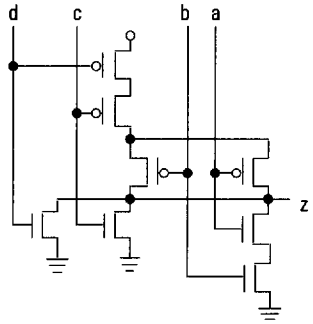
ao1
2-AND into 3-NOR

Name: ao1 Description: 2-AND into 3-NOR

Coding Syntax: z=ao1*(a,b,c,d)

Logic Symbol: Schematics:





Truth Table:

a	*b*	*c*	*d*	*z*
1	1	x	x	0
x	x	1	x	0
x	x	x	1	0
x	0	0	0	1
0	x	0	0	1

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*b*	*c*	*d*
ao1	0.9	0.9	1.0	1.0
ao1p	1.9	1.9	1.9	2.0

AC Characteristics:

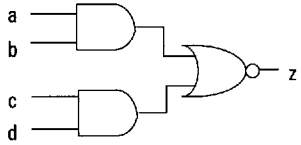
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

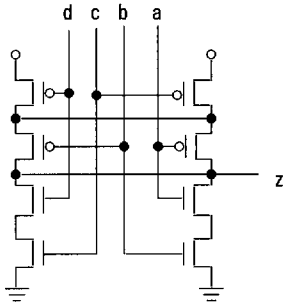
Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
ao1	2	in_to_z	tpLH	0.47	0.70	1.20	1.66	2.14
			tpHL	0.20	0.25	0.36	0.46	0.56
ao1p	4	in_to_z	tpLH	0.36	0.47	0.72	0.95	1.20
			tpHL	0.17	0.20	0.25	0.30	0.36

Name: ao2 Description: 2 2-ANDs into 2-NOR

Coding Syntax: z=ao2*(a,b,c,d)

Logic Symbol: Schematics:





Truth Table:

a	*b*	*c*	*d*	*z*
1	1	x	x	0
x	x	1	1	0
0	x	0	x	1
0	x	x	0	1
x	0	x	0	1
x	0	0	x	1

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*b*	*c*	*d*
ao2	1.0	1.0	1.0	1.0
ao2p	2.0	2.0	2.0	2.0

AC Characteristics:

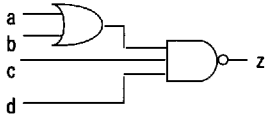
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

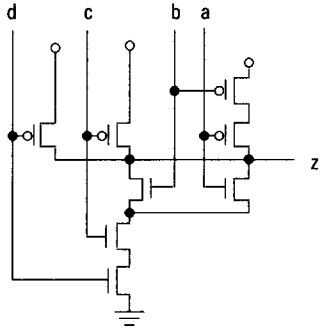
Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
ao2	2	in_to_z	tpLH	0.38	0.53	0.87	1.18	1.52
			tpHL	0.23	0.29	0.43	0.56	0.70
ao2p	4	in_to_z	tpLH	0.30	0.38	0.54	0.70	0.87
			tpHL	0.19	0.23	0.29	0.36	0.43

Name: ao3 Description: 2-OR into 3-NAND

Coding Syntax: z=ao3*(a,b,c,d)

Logic Symbol: Schematics:





Truth Table:

a	*b*	*c*	*d*	*z*
1	x	1	1	0
x	1	1	1	0
0	0	x	x	1
x	x	0	x	1
x	x	x	0	1

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*b*	*c*	*d*
ao3	1.0	1.0	1.0	1.0
ao3p	2.0	2.0	2.0	2.0

AC Characteristics:

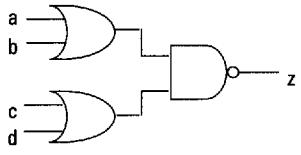
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
ao3	2	in_to_z	tpLH	0.26	0.38	0.63	0.88	1.14
			tpHL	0.28	0.37	0.55	0.74	0.94
ao3p	4	in_to_z	tpLH	0.21	0.26	0.39	0.51	0.63
			tpHL	0.23	0.28	0.37	0.46	0.54

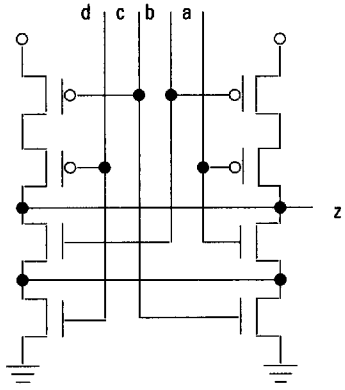
Name: ao4 Description: 2 2-ORs into 2-NAND

Coding Syntax: z=ao4*(a,b,c,d)

Logic Symbol:



Schematics:



Truth Table:

a	*b*	*c*	*d*	*z*
0	0	x	x	1
x	x	0	0	1
1	x	1	x	0
x	1	1	x	0
1	x	x	1	0
x	1	x	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*b*	*c*	*d*
ao4	1.0	1.0	1.0	1.0
ao4p	2.0	2.0	2.0	1.9

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

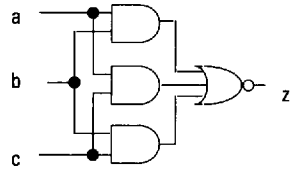
Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
ao4	2	in_to_z	tpLH	0.35	0.51	0.85	1.18	1.50
			tpHL	0.25	0.31	0.45	0.57	0.72
ao4p	4	in_to_z	tpLH	0.27	0.35	0.51	0.67	0.84
			tpHL	0.21	0.25	0.32	0.38	0.45

ao5
Inverting 2-of-3 Majority

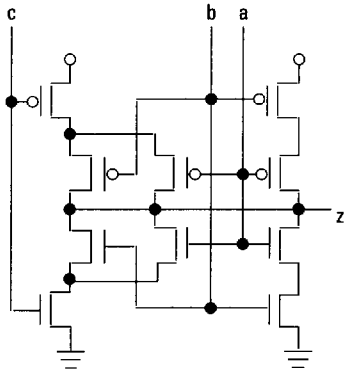
Name: ao5 Description: Inverting 2-of-3 Majority

Coding Syntax: z=ao5*(a,b,c)

Logic Symbol:



Schematics:



Truth Table:

a	*b*	*c*	*z*
1	1	x	0
1	x	1	0
x	1	1	0
0	0	x	1
0	x	0	1
x	0	0	1

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*b*	*c*
ao5	1.9	1.9	1.0
ao5p	3.9	3.9	2.1

AC Characteristics:

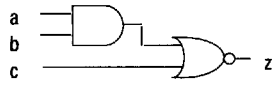
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

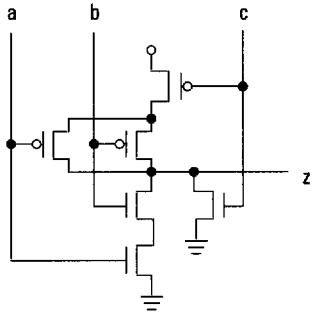
Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
ao5	3	in_to_z	tpLH	0.42	0.58	0.92	1.24	1.57
			tpHL	0.29	0.36	0.49	0.63	0.77
ao5p	5	in_to_z	tpLH	0.34	0.42	0.58	0.75	0.90
			tpHL	0.25	0.29	0.36	0.42	0.49

Name: ao6 Description: 2-AND into 2-NOR

Coding Syntax: z=ao6*(a,b,c)

Logic Symbol: Schematics:





Truth Table:

a	*b*	*c*	*z*
x	x	1	0
0	x	0	1
x	0	0	1
1	1	x	0

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*b*	*c*
ao6	1.0	1.0	1.0
ao6p	2.0	2.0	2.0

AC Characteristics:

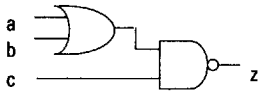
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

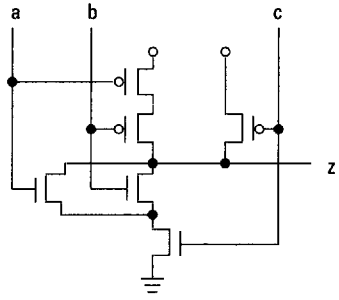
Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
ao6	2	in_to_z	tpLH	0.31	0.46	0.79	1.12	1.46
			tpHL	0.19	0.24	0.36	0.48	0.58
ao6p	3	in_to_z	tpLH	0.24	0.31	0.47	0.63	0.79
			tpHL	0.16	0.19	0.24	0.30	0.36

Name: ao7 Description: 2-OR into 2-NAND

Coding Syntax: z=ao7*(a,b,c)

Logic Symbol: Schematics:





Truth Table:

a	*b*	*c*	*z*
x	x	0	1
1	x	1	0
x	1	1	0
0	0	x	1

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*b*	*c*
ao7	1.0	1.0	1.0
ao7p	2.0	2.0	2.0

AC Characteristics:

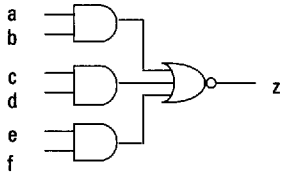
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

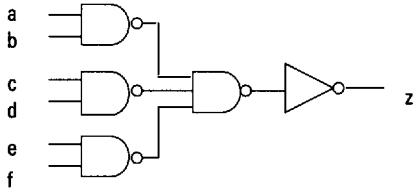
Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
ao7	2	in_to_z	tpLH	0.26	0.39	0.67	0.95	1.22
			tpHL	0.21	0.28	0.41	0.54	0.67
ao7p	3	in_to_z	tpLH	0.19	0.26	0.39	0.52	0.66
			tpHL	0.18	0.21	0.28	0.34	0.41

Name: ao11 Description: 3 2-ANDs into 3-NOR

Coding Syntax: z=ao11*(a,b,c,d,e,f)

Logic Symbol: Schematics:





Truth Table:

a	*b*	*c*	*d*	*e*	*f*	*z*
1	1	x	x	x	x	0
x	x	1	1	x	x	0
x	x	x	x	1	1	0
other states						1

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*b*	*c*	*d*	*e*	*f*
ao11	1.0	1.0	1.0	1.0	1.0	1.0
ao11p	1.0	1.0	1.0	1.0	1.0	1.0

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

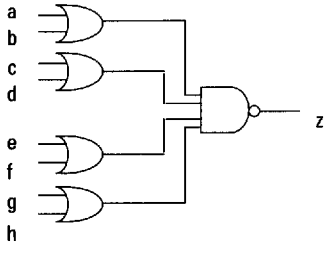
Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
ao11	5	in_to_z	tpLH	0.48	0.57	0.74	0.91	1.08
			tpHL	0.42	0.47	0.55	0.64	0.72
ao11p	6	in_to_z	tpLH	0.47	0.53	0.61	0.70	0.79
			tpHL	0.42	0.45	0.51	0.55	0.60

Name: ao12

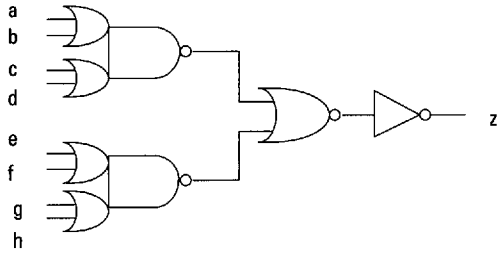
Description: 4 2-ORs into 4-NAND

Coding Syntax: z=ao12*(a,b,c,d,e,f,g,h)

Logic Symbol:



Schematics:



Truth Table:

a	*b*	*c*	*d*	*e*	*f*	*g*	*h*	*z*
0	0	x	x	x	x	x	x	1
x	x	0	0	x	x	x	x	1
x	x	x	x	0	0	x	x	1
x	x	x	x	x	x	0	0	1
other states								0

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*b*	*c*	*d*	*e*	*f*	*g*	*h*
ao12	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
ao12p	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0

AC Characteristics:

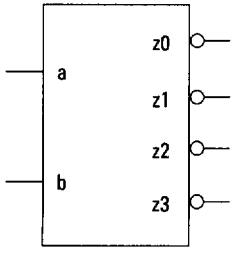
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
ao12	6	in_to_z	tpLH	0.54	0.62	0.78	0.95	1.13
			tpHL	0.54	0.58	0.68	0.76	0.85
ao12p	6	in_to_z	tpLH	0.53	0.57	0.65	0.73	0.81
			tpHL	0.56	0.59	0.66	0.72	0.75

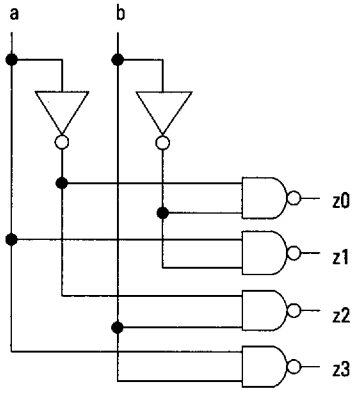
Name: d24l Description: 2-to-4 Decoder

Coding Syntax: u(z0,z1,z2,z3)=d24l*(a,b)

Logic Symbol:



Schematics:



Truth Table:

a	*b*	*z0*	*z1*	*z2*	*z3*
0	0	0	1	1	1
1	0	1	0	1	1
0	1	1	1	0	1
1	1	1	1	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*b*
d24l	2.8	3.0
d24lp	4.5	5.0

AC Characteristics:

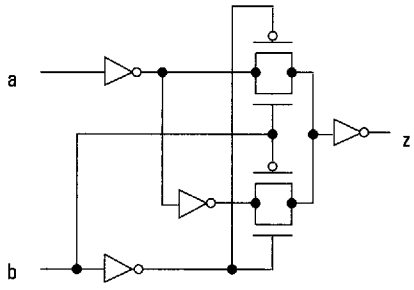
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
d24l	5	a_to_z0	tpLH	0.52	0.61	0.77	0.95	1.13
			tpHL	0.57	0.64	0.77	0.91	1.05
		b_to_z0	tpLH	0.57	0.65	0.81	0.99	1.18
			tpHL	0.55	0.62	0.75	0.89	1.03
		a_to_z1	tpLH	0.70	0.78	0.94	1.11	1.30
			tpHL	0.99	1.06	1.20	1.34	1.47
		b_to_z1	tpLH	0.53	0.61	0.77	0.94	1.13
			tpHL	0.57	0.64	0.78	0.92	1.05
		a_to_z2	tpLH	0.51	0.60	0.77	0.94	1.14
			tpHL	0.54	0.62	0.76	0.90	1.04
		b_to_z2	tpLH	0.60	0.69	0.86	1.03	1.23
			tpHL	0.71	0.79	0.93	1.07	1.21
		a_to_z3	tpLH	0.50	0.64	0.88	1.09	1.29
			tpHL	0.59	0.73	0.95	1.15	1.32
		b_to_z3	tpLH	0.39	0.53	0.77	0.99	1.19
			tpHL	0.41	0.54	0.77	0.96	1.14
d24lp	9	a_to_z0	tpLH	0.61	0.65	0.74	0.82	0.91
			tpHL	0.66	0.70	0.78	0.84	0.91
		b_to_z0	tpLH	0.67	0.72	0.80	0.88	0.97
			tpHL	0.66	0.70	0.77	0.84	0.91
		a_to_z1	tpLH	0.36	0.40	0.57	0.71	0.84
			tpHL	0.67	0.72	0.80	0.87	0.94
		b_to_z1	tpLH	0.64	0.68	0.85	0.99	1.13
			tpHL	0.67	0.72	0.80	0.87	0.94
		a_to_z2	tpLH	0.60	0.64	0.73	0.82	0.90
			tpHL	0.64	0.68	0.77	0.84	0.91
		b_to_z2	tpLH	0.56	0.61	0.70	0.78	0.87
			tpHL	0.54	0.58	0.67	0.74	0.81
		a_to_z3	tpLH	0.40	0.47	0.61	0.73	0.84
			tpHL	0.44	0.52	0.65	0.77	0.88
		b_to_z3	tpLH	0.32	0.39	0.53	0.66	0.77
			tpHL	0.33	0.41	0.54	0.66	0.77

Name: en Description: 2-Input Exclusive NOR

Coding Syntax: z=en*(a,b)

Logic Symbol: Schematics:



Truth Table:

a	*b*	*z*
0	0	1
0	1	0
1	0	0
1	1	1

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*b*
en	1.1	2.0
enp	1.1	2.0

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
en	3	a_to_z	tpLH	0.47	0.56	0.73	0.89	1.08
			tpHL	0.45	0.52	0.61	0.70	0.79
		b_to_z	tpLH	0.27	0.35	0.51	0.68	0.87
			tpHL	0.25	0.31	0.40	0.49	0.57
enp	4	a_to_z	tpLH	0.46	0.51	0.59	0.67	0.76
			tpHL	0.45	0.49	0.56	0.61	0.67
		b_to_z	tpLH	0.26	0.30	0.39	0.46	0.55
			tpHL	0.26	0.29	0.35	0.40	0.46

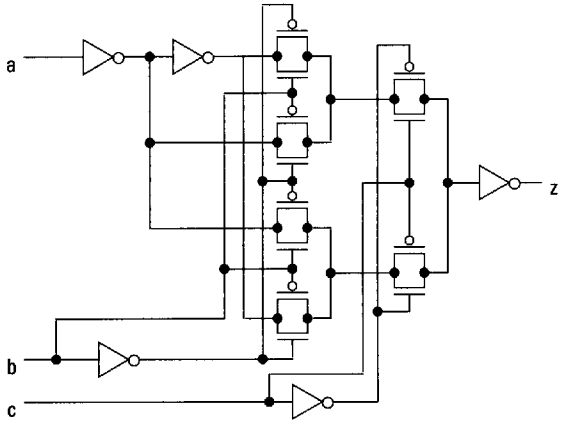
en3
3-Input Exclusive NOR

Name: en3 Description: 3-Input Exclusive NOR

Coding Syntax: z=en3*(a,b,c)

Logic Symbol:

Schematics:



Truth Table:

a	*b*	*c*	*z*
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*b*	*c*
en3	1.1	2.3	1.3
en3p	1.1	2.3	1.3

AC Characteristics:

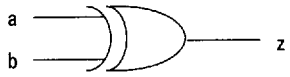
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

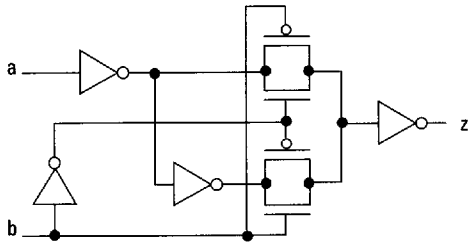
Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
en3	6	a_to_z	tpLH	0.78	0.87	1.04	1.21	1.39
			tpHL	0.81	0.88	0.99	1.11	1.19
		b_to_z	tpLH	0.46	0.55	0.72	0.89	1.07
			tpHL	0.49	0.56	0.67	0.79	0.88
		c_to_z	tpLH	0.35	0.44	0.61	0.78	0.96
			tpHL	0.38	0.45	0.56	0.68	0.76
en3p	6	a_to_z	tpLH	0.76	0.81	0.91	1.00	1.08
			tpHL	0.82	0.87	0.95	1.01	1.07
		b_to_z	tpLH	0.44	0.50	0.59	0.68	0.76
			tpHL	0.50	0.55	0.63	0.69	0.75
		c_to_z	tpLH	0.33	0.38	0.47	0.56	0.65
			tpHL	0.39	0.43	0.51	0.58	0.64

Name: eo Description: 2-Input Exclusive OR

Coding Syntax: z=eo*(a,b)

Logic Symbol: Schematics:





Truth Table:

a	*b*	*z*
0	0	0
0	1	1
1	0	1
1	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*b*
eo	1.1	2.0
eop	1.1	2.0

AC Characteristics:

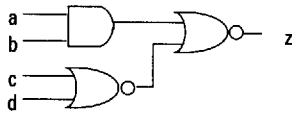
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

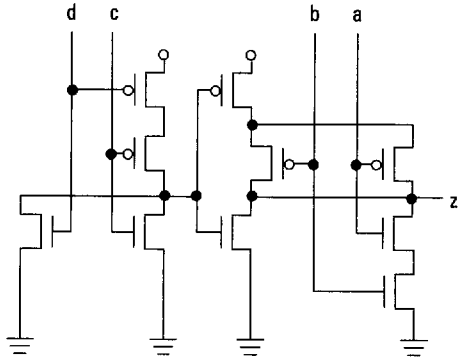
Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
eo	3	a_to_z	tpLH	0.47	0.56	0.73	0.90	1.08
			tpHL	0.46	0.52	0.62	0.71	0.79
		b_to_z	tpLH	0.27	0.35	0.51	0.68	0.86
			tpHL	0.25	0.30	0.40	0.49	0.57
eop	4	a_to_z	tpLH	0.46	0.51	0.59	0.68	0.76
			tpHL	0.45	0.50	0.56	0.62	0.67
		b_to_z	tpLH	0.26	0.30	0.38	0.46	0.55
			tpHL	0.25	0.29	0.35	0.40	0.45

Name: eo1 Description: 2-AND, 2-NOR into 2-NOR

Coding Syntax: z=eo1*(a,b,c,d)

Logic Symbol: Schematics:





Truth Table:

a	*b*	*c*	*d*	*z*
1	1	x	x	0
0	x	1	x	1
0	x	x	1	1
x	0	1	x	1
x	0	x	1	1
x	x	0	0	0

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*b*	*c*	*d*
eo1	1.0	1.0	1.0	1.0
eo1p	1.9	1.9	1.0	1.0

eo1
2-AND, 2-NOR into 2-NOR

AC Characteristics:

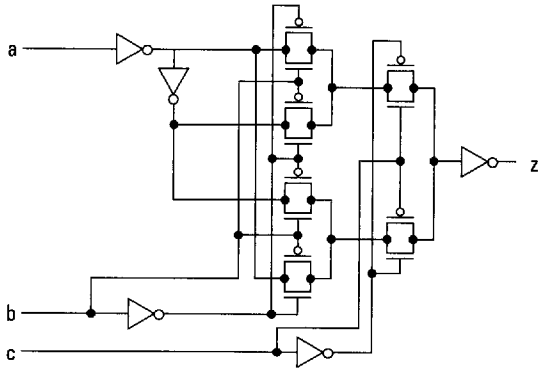
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
eo1	3	c_to_z	tpLH	0.54	0.69	1.02	1.34	1.66
			tpHL	0.38	0.44	0.53	0.63	0.73
		d_to_z	tpLH	0.53	0.68	1.00	1.33	1.65
			tpHL	0.34	0.39	0.49	0.58	0.68
		a_to_z	tpLH	0.35	0.50	0.83	1.15	1.47
			tpHL	0.23	0.29	0.42	0.56	0.70
		b_to_z	tpLH	0.27	0.42	0.75	1.08	1.40
			tpHL	0.20	0.27	0.40	0.53	0.67
eo1p	4	c_to_z	tpLH	0.49	0.56	0.72	0.88	1.05
			tpHL	0.43	0.46	0.52	0.57	0.62
		d_to_z	tpLH	0.48	0.55	0.71	0.87	1.04
			tpHL	0.39	0.42	0.47	0.53	0.58
		a_to_z	tpLH	0.27	0.35	0.50	0.66	0.83
			tpHL	0.20	0.23	0.29	0.36	0.42
		b_to_z	tpLH	0.20	0.27	0.42	0.58	0.75
			tpHL	0.17	0.20	0.27	0.33	0.40

Name: eo3 Description: 3-Input Exclusive OR

Coding Syntax: z=eo3*(a,b,c)

Logic Symbol: Schematics:



Truth Table:

a	*b*	*c*	*z*
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*b*	*c*
eo3	1.1	2.3	2.1
eo3p	1.1	2.3	2.1

eo3
3-Input Exclusive OR

AC Characteristics:

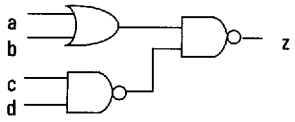
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

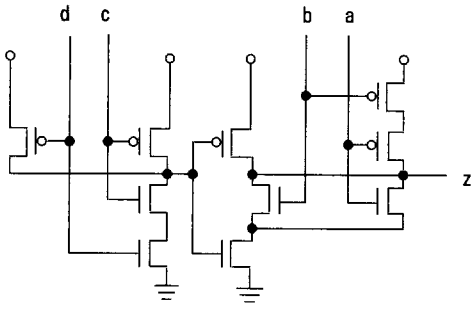
Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
eo3	6	a_to_z	tpLH	0.78	0.87	1.06	1.21	1.39
			tpHL	0.75	0.82	0.94	1.05	1.15
		b_to_z	tpLH	0.47	0.56	0.73	0.90	1.08
			tpHL	0.44	0.50	0.61	0.74	0.84
		c_to_z	tpLH	0.31	0.39	0.56	0.74	0.92
			tpHL	0.28	0.34	0.44	0.58	0.68
eo3p	6	a_to_z	tpLH	0.77	0.82	0.92	1.01	1.08
			tpHL	0.75	0.79	0.86	0.94	1.00
		b_to_z	tpLH	0.45	0.51	0.60	0.68	0.77
			tpHL	0.44	0.48	0.55	0.61	0.69
		c_to_z	tpLH	0.29	0.34	0.44	0.52	0.61
			tpHL	0.27	0.32	0.38	0.45	0.52

Name: eon1 Description: 2-OR, 2-NAND into 2-NAND

Coding Syntax: z=eon1*(a,b,c,d)

Logic Symbol: Schematics:





Truth Table:

a	*b*	*c*	*d*	*z*
x	x	1	1	1
1	x	0	x	0
x	1	0	x	0
1	x	x	0	0
x	1	x	0	0
0	0	x	x	1

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*b*	*c*	*d*
eon1	1.0	1.0	1.0	1.0
eon1p	2.0	2.0	1.1	1.1

eon1

2-OR, 2-NAND into 2-NAND

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

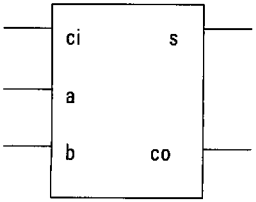
Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
eon1	3	d_to_z	tpLH	0.37	0.44	0.57	0.71	0.87
			tpHL	0.34	0.41	0.54	0.67	0.82
		c_to_z	tpLH	0.39	0.46	0.60	0.74	0.90
			tpHL	0.38	0.44	0.57	0.71	0.85
		b_to_z	tpLH	0.31	0.46	0.78	1.12	1.44
			tpHL	0.20	0.27	0.40	0.53	0.67
		a_to_z	tpLH	0.26	0.41	0.74	1.07	1.39
			tpHL	0.19	0.25	0.38	0.52	0.66
eon1p	4	d_to_z	tpLH	0.38	0.41	0.48	0.55	0.62
			tpHL	0.35	0.39	0.45	0.52	0.58
		c_to_z	tpLH	0.40	0.44	0.51	0.58	0.65
			tpHL	0.39	0.42	0.49	0.55	0.62
		b_to_z	tpLH	0.23	0.31	0.46	0.62	0.79
			tpHL	0.17	0.20	0.27	0.33	0.40
		a_to_z	tpLH	0.19	0.26	0.41	0.57	0.74
			tpHL	0.16	0.19	0.25	0.32	0.38

Name: fa1a

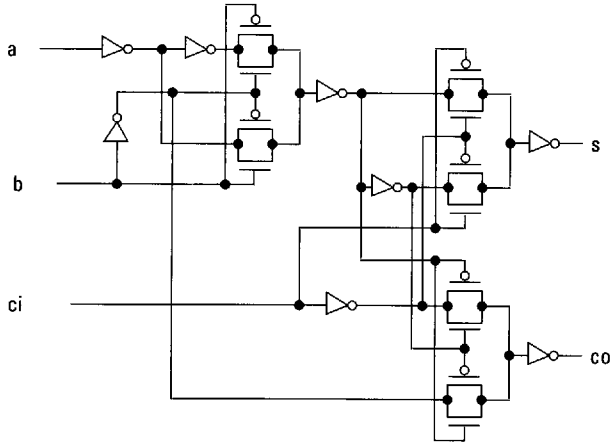
Description: Full Adder

Coding Syntax: u(s,co)=fa1a*(ci,a,b)

Logic Symbol:



Schematics:



Truth Table:

ci	*a*	*b*	*s*	*co*
0	0	0	0	0
1	0	0	1	0
0	1	0	1	0
0	0	1	1	0
1	1	0	0	1
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1

Loading Characteristics:

Values stated in standard loads.

Version	*ci*	*a*	*b*
fa1a	1.3	1.1	1.3
fa1ap	1.3	1.1	1.3

AC Characteristics:

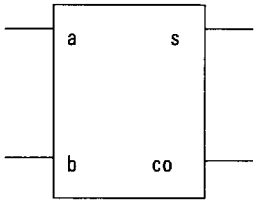
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fa1a	8	a_to_s	tpLH	1.12	1.21	1.37	1.54	1.72
			tpHL	1.15	1.21	1.32	1.41	1.49
		b_to_s	tpLH	1.19	1.27	1.43	1.60	1.79
			tpHL	1.21	1.27	1.38	1.47	1.56
		ci_to_s	tpLH	0.80	0.88	1.05	1.22	1.40
			tpHL	0.83	0.89	0.99	1.08	1.17
		a_to_co	tpLH	1.20	1.28	1.44	1.62	1.80
			tpHL	1.13	1.19	1.29	1.38	1.47
		b_to_co	tpLH	0.75	0.83	0.99	1.17	1.35
			tpHL	1.08	1.14	1.24	1.33	1.42
		ci_to_co	tpLH	0.77	0.85	1.01	1.19	1.37
			tpHL	0.76	0.82	0.92	1.01	1.10
fa1ap	8	a_to_s	tpLH	1.12	1.16	1.24	1.33	1.41
			tpHL	1.16	1.20	1.27	1.32	1.38
		b_to_s	tpLH	1.23	1.28	1.36	1.44	1.53
			tpHL	1.28	1.32	1.38	1.44	1.49
		ci_to_s	tpLH	0.86	0.91	0.99	1.07	1.16
			tpHL	0.91	0.95	1.01	1.07	1.12
		a_to_co	tpLH	1.22	1.26	1.35	1.43	1.51
			tpHL	1.14	1.18	1.24	1.30	1.35
		b_to_co	tpLH	0.78	0.83	0.91	0.99	1.08
			tpHL	1.09	1.13	1.19	1.25	1.30
		ci_to_co	tpLH	0.79	0.84	0.92	1.01	1.09
			tpHL	0.78	0.81	0.88	0.94	0.99

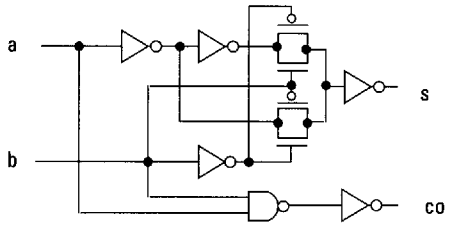
Name: ha1 Description: Half Adder

Coding Syntax: u(s,co)=ha1*(a,b)

Logic Symbol:



Schematics:



Truth Table:

a	*b*	*s*	*co*
0	0	0	0
1	1	1	0
1	0	1	0
1	1	0	1

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*b*
ha1	2.0	2.3
ha1p	2.0	2.3

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
ha1	5	a_to_s	tpLH	0.74	0.82	0.98	1.15	1.33
			tpHL	0.73	0.79	0.89	0.98	1.07
		b_to_s	tpLH	0.57	0.64	0.81	0.97	1.16
			tpHL	0.56	0.62	0.72	0.81	0.89
		a_to_co	tpLH	0.58	0.66	0.83	1.01	1.19
			tpHL	0.50	0.56	0.66	0.75	0.84
		b_to_co	tpLH	0.55	0.64	0.81	0.99	1.17
			tpHL	0.50	0.56	0.66	0.75	0.84

AC Characteristics: (Cont.)

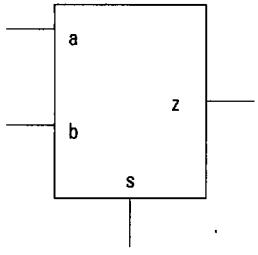
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
ha1p	6	a_to_s	tpLH	0.73	0.77	0.86	0.94	1.02
			tpHL	0.75	0.79	0.85	0.90	0.95
		b_to_s	tpLH	0.56	0.60	0.69	0.77	0.85
			tpHL	0.58	0.62	0.68	0.73	0.78
		a_to_co	tpLH	0.61	0.66	0.74	0.83	0.92
			tpHL	0.54	0.58	0.64	0.70	0.74
		b_to_co	tpLH	0.61	0.66	0.74	0.83	0.91
			tpHL	0.56	0.59	0.66	0.71	0.76

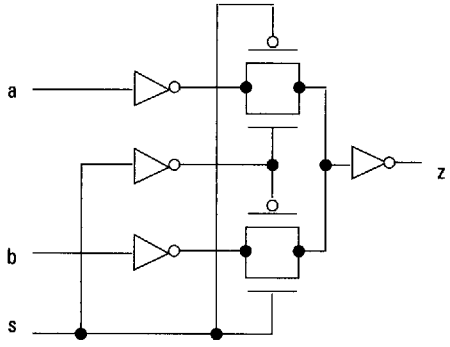
Name: mux21h Description: Non-Inverting Gate MUX

Coding Syntax: z=mux21h*(a,b,s)

Logic Symbol:



Schematics:



Truth Table:

s	*a*	*b*	*z*
0	0	x	0
0	1	x	1
1	x	0	0
1	x	1	1

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*b*	*s*
mux21h	1.1	1.1	1.3
mux21hp	1.1	1.1	1.3

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
mux21h	4	a_to_z	tpLH	0.30	0.35	0.43	0.51	0.59
			tpHL	0.40	0.46	0.56	0.64	0.73
		b_to_z	tpLH	0.30	0.34	0.43	0.51	0.59
			tpHL	0.41	0.46	0.56	0.65	0.73
		s_to_z	tpLH	0.28	0.33	0.41	0.49	0.57
			tpHL	0.40	0.45	0.55	0.63	0.72

AC Characteristics: (Cont.)

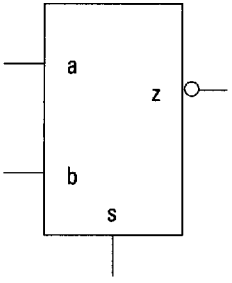
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

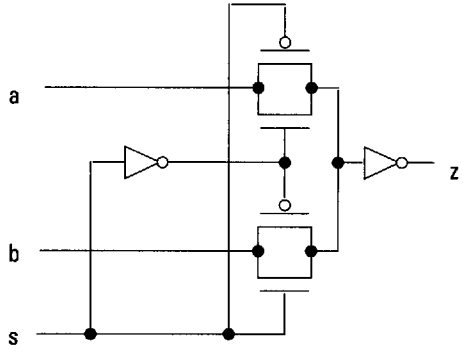
Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
mux21hp	5	a_to_z	tpLH	0.32	0.35	0.40	0.44	0.48
			tpHL	0.45	0.48	0.55	0.60	0.66
		b_to_z	tpLH	0.31	0.34	0.39	0.44	0.48
			tpHL	0.45	0.49	0.55	0.61	0.66
		s_to_z	tpLH	0.29	0.32	0.37	0.41	0.46
			tpHL	0.47	0.51	0.56	0.61	0.66

Name: mux211 Description: Inverting Gate MUX

Coding Syntax: z=mux211*(a,b,s)

Logic Symbol: Schematics:





Truth Table:

s	*a*	*b*	*z*
0	0	x	1
0	1	x	0
1	x	0	1
1	x	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*b*	*s*
mux211	3.8	3.8	2.0
mux211p	5.2	5.2	2.1

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
mux211	4	a_to_z	tpLH	0.16	0.19	0.27	0.35	0.43
			tpHL	0.19	0.23	0.32	0.40	0.48
		b_to_z	tpLH	0.15	0.19	0.27	0.35	0.43
			tpHL	0.19	0.24	0.33	0.40	0.48
		s_to_z	tpLH	0.19	0.23	0.30	0.38	0.46
			tpHL	0.25	0.29	0.38	0.45	0.54

AC Characteristics: (Cont.)

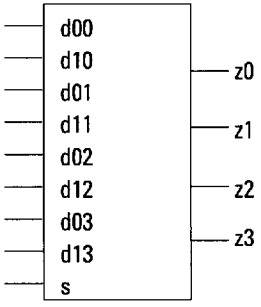
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
mux21lp	5	a_to_z	tpLH	0.16	0.18	0.22	0.26	0.30
			tpHL	0.20	0.22	0.27	0.32	0.36
		b_to_z	tpLH	0.15	0.17	0.22	0.26	0.30
			tpHL	0.20	0.23	0.28	0.33	0.37
		s_to_z	tpLH	0.21	0.23	0.28	0.31	0.35
			tpHL	0.28	0.31	0.36	0.40	0.44

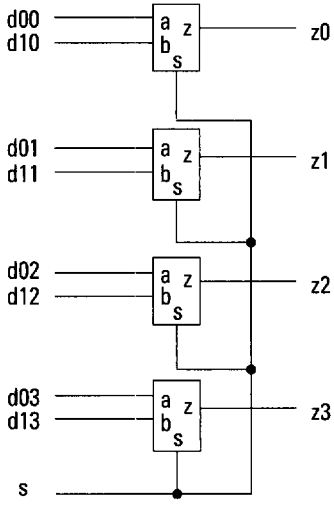
Name: mux24p Description: 4-Bit 2-to-1 MUX, Non-Inverting

Coding Syntax: u(z0,z1,z2,z3)=mux24p(d00,d10,d01,d11,d02,d12,d03,d13,s)

Logic Symbol:



Schematics:



Truth Table:

s	*z0*	*z1*	*z2*	*z3*
0	d00	d01	d02	d03
1	d10	d11	d12	d13

Loading Characteristics:

Values stated in standard loads.

Version	*d00*	*d10*	*d01*	*d11*	*d02*	*d12*	*d03*	*d13*	*s*
mux24p	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	2.0

AC Characteristics:

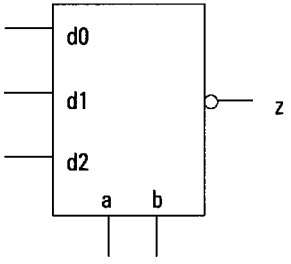
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

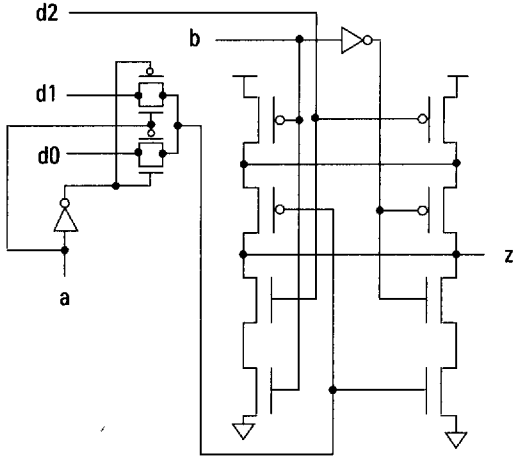
Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
mux24p	14	d to any z	tpLH	0.71	0.76	0.84	0.92	1.01
			tpHL	0.68	0.72	0.79	0.84	0.89
		s to any z	tpLH	0.75	0.80	0.88	0.96	1.05
			tpHL	0.73	0.77	0.83	0.89	0.94

Name: mux311 Description: 3-Bit Inverting MUX

Coding Syntax: z=mux311*(d0,d1,d2,a,b)

Logic Symbol: Schematics:





Truth Table:

a	*b*	*z*
0	0	$\overline{d0}$
1	0	$\overline{d1}$
x	1	$\overline{d2}$

Loading Characteristics:

Values stated in standard loads.

Version	*d0*	*d1*	*d2*	*a*	*b*
mux311	3.2	3.2	1.0	2.0	2.0
mux311p	4.1	4.1	2.0	2.1	3.0

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

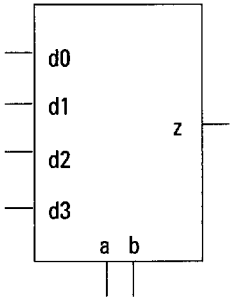
Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
mux31l	4	d0_to_z	tpLH	0.46	0.62	0.95	1.26	1.58
			tpHL	0.29	0.36	0.49	0.63	0.77
		d1_to_z	tpLH	0.46	0.62	0.95	1.26	1.58
			tpHL	0.29	0.36	0.49	0.63	0.77
		d2_to_z	tpLH	0.36	0.51	0.84	1.17	1.49
			tpHL	0.25	0.32	0.45	0.59	0.73
		a_to_z	tpLH	0.52	0.67	0.99	1.32	1.64
			tpHL	0.31	0.38	0.66	0.82	1.09
		b_to_z	tpLH	0.47	0.63	0.95	1.28	1.59
			tpHL	0.26	0.33	0.62	0.78	1.05
mux31lp	6	d0_to_z	tpLH	0.34	0.41	0.57	0.73	0.90
			tpHL	0.24	0.28	0.35	0.41	0.48
		d1_to_z	tpLH	0.34	0.41	0.57	0.73	0.90
			tpHL	0.24	0.28	0.35	0.41	0.48
		d2_to_z	tpLH	0.23	0.30	0.46	0.61	0.78
			tpHL	0.18	0.21	0.28	0.35	0.41
		a_to_z	tpLH	0.41	0.48	0.64	0.80	0.96
			tpHL	0.27	0.32	0.39	0.56	0.67
		b_to_z	tpLH	0.32	0.39	0.54	0.70	0.87
			tpHL	0.19	0.22	0.29	0.46	0.57

mux41
4-Bit Non-Inverting MUX

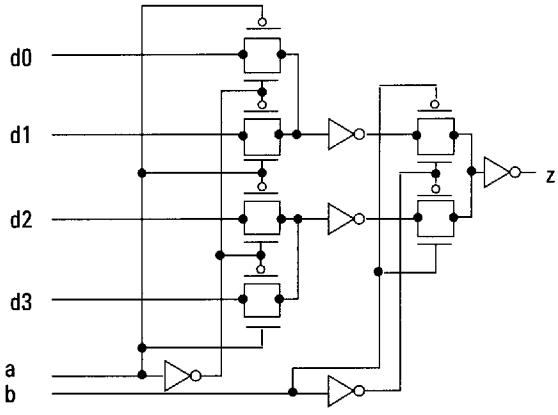
Name: mux41 Description: 4-Bit Non-Inverting MUX

Coding Syntax: z=mux41*(d0,d1,d2,d3,a,b)

Logic Symbol:



Schematics:



Truth Table:

a	*b*	*z*
0	0	d0
1	0	d1
0	1	d2
1	1	d3

Loading Characteristics:

Values stated in standard loads.

Version	*d0*	*d1*	*d2*	*d3*	*a*	*b*
mux41	3.3	3.3	3.3	3.3	2.3	2.1
mux41p	3.3	3.3	3.3	3.3	2.3	2.1

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

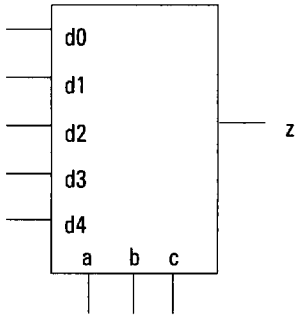
Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
mux41	6	Any d to z	tpLH	0.40	0.48	0.64	0.81	0.99
			tpHL	0.38	0.44	0.54	0.63	0.72
		a-z	tpLH	0.52	0.61	0.77	0.94	1.12
			tpHL	0.50	0.56	0.65	0.74	0.83
		b-z	tpLH	0.28	0.36	0.52	0.69	0.87
			tpHL	0.26	0.31	0.41	0.49	0.58
mux41p	7	Any d to z	tpLH	0.39	0.43	0.52	0.60	0.68
			tpHL	0.40	0.43	0.50	0.55	0.60
		a-z	tpLH	0.51	0.56	0.64	0.73	0.81
			tpHL	0.51	0.55	0.61	0.67	0.71
		b-z	tpLH	0.27	0.32	0.40	0.48	0.56
			tpHL	0.27	0.30	0.37	0.42	0.47

mux51h
Non-Inverting 5-to-1 MUX

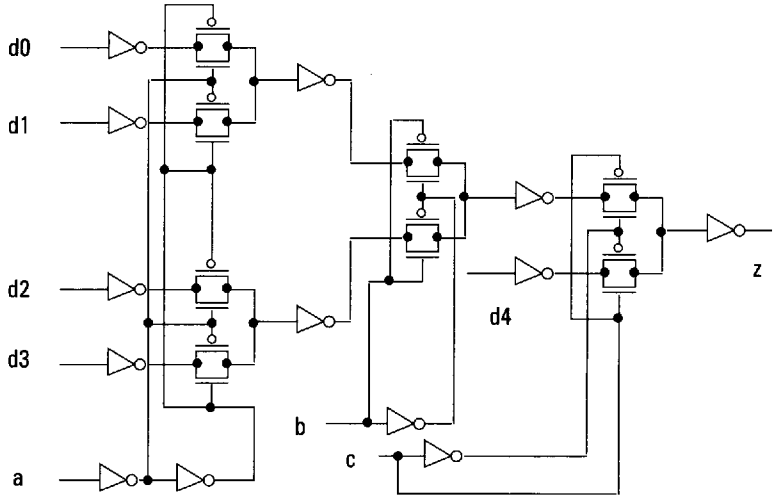
Name: mux51h Description: Non-Inverting 5-to-1 MUX

Coding Syntax: z=mux51h*(d0,d1,d2,d3,d4,a,b,c)

Logic Symbol:



Schematics:



Truth Table:

a	*b*	*c*	*z*
0	0	0	d0
1	0	0	d1
0	1	0	d2
1	1	0	d3
x	x	1	d4

Loading Characteristics:

Values stated in standard loads.

Version	*d0*	*d1*	*d2*	*d3*	*d4*	*a*	*b*	*c*
mux51h	1.1	1.1	1.1	1.1	1.1	1.1	1.3	2.0
mux51hp	1.1	1.1	1.1	1.1	1.1	1.1	1.3	2.0

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

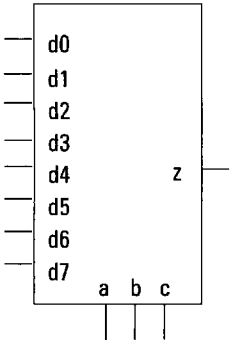
Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
mux51h	11	d0_to_z	tpLH	0.79	0.87	1.04	1.21	1.39
			tpHL	0.78	0.84	0.94	1.03	1.12
		d1_to_z	tpLH	0.79	0.87	1.04	1.21	1.39
			tpHL	0.78	0.84	0.94	1.03	1.12
		d2_to_z	tpLH	0.79	0.87	1.04	1.21	1.39
			tpHL	0.78	0.84	0.94	1.03	1.12
		d3_to_z	tpLH	0.79	0.87	1.04	1.21	1.39
			tpHL	0.78	0.84	0.94	1.03	1.12
		d4_to_z	tpLH	0.35	0.43	0.59	0.76	0.94
			tpHL	0.34	0.39	0.49	0.59	0.67
		a_to_z	tpLH	0.96	1.04	1.21	1.37	1.55
			tpHL	0.92	0.98	1.08	1.17	1.25
		b_to_z	tpLH	0.57	0.66	0.82	0.98	1.16
			tpHL	0.53	0.59	0.69	0.78	0.87
		c_to_z	tpLH	0.30	0.38	0.53	0.70	0.88
			tpHL	0.26	0.31	0.41	0.49	0.58
mux51hp	11	d0_to_z	tpLH	0.78	0.83	0.91	0.99	1.07
			tpHL	0.78	0.81	0.88	0.94	0.99
		d1_to_z	tpLH	0.78	0.83	0.91	0.99	1.07
			tpHL	0.78	0.81	0.88	0.94	0.99
		d2_to_z	tpLH	0.78	0.83	0.91	0.99	1.07
			tpHL	0.78	0.81	0.88	0.94	0.99
		d3_to_z	tpLH	0.78	0.83	0.91	0.99	1.07
			tpHL	0.78	0.81	0.88	0.94	0.99
		d4_to_z	tpLH	0.32	0.36	0.45	0.53	0.61
			tpHL	0.34	0.37	0.44	0.49	0.55
		a_to_z	tpLH	0.94	0.99	1.07	1.15	1.23
			tpHL	0.91	0.95	1.02	1.08	1.12
		b_to_z	tpLH	0.55	0.60	0.68	0.77	0.85
			tpHL	0.53	0.57	0.63	0.69	0.74
		c_to_z	tpLH	0.28	0.33	0.41	0.48	0.56
			tpHL	0.26	0.29	0.35	0.41	0.46

mux81
8-Bit Non-Inverting MUX

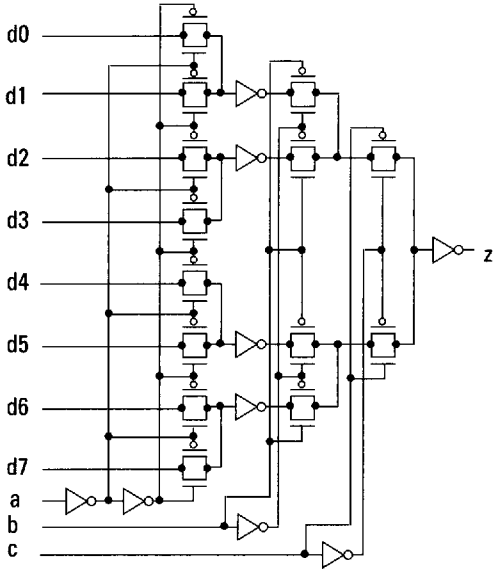
Name: mux81 Description: 8-Bit Non-Inverting MUX

Coding Syntax: z=mux81*(d0,d1,d2,d3,d4,d5,d6,d7,a,b,c)

Logic Symbol:



Schematics:



Truth Table:

a	*b*	*c*	*z*
0	0	0	d0
1	0	0	d1
0	1	0	d2
1	1	0	d3
0	0	1	d4
1	0	1	d5
0	1	1	d6
1	1	1	d7

Loading Characteristics:

Values stated in standard loads.

Version	*d0*	*d1*	*d2*	*d3*	*d4*	*d5*	*d6*	*d7*	*a*	*b*	*c*
mux81	3.3	3.3	3.3	3.3	3.3	3.3	3.3	3.3	1.1	2.6	2.1
mux81p	3.3	3.3	3.3	3.3	3.3	3.3	3.3	3.3	1.1	2.6	2.1

AC Characteristics:

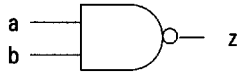
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
mux81	15	d to any z	tpLH	0.54	0.63	0.80	0.97	1.15
			tpHL	0.53	0.60	0.72	0.83	0.93
		a_to_z	tpLH	0.90	0.99	1.17	1.35	1.51
			tpHL	0.80	0.88	1.00	1.11	1.20
		b_to_z	tpLH	0.51	0.60	0.78	0.96	1.12
			tpHL	0.42	0.49	0.61	0.72	0.81
		c_to_z	tpLH	0.37	0.45	0.62	0.79	0.94
			tpHL	0.28	0.34	0.45	0.54	0.64
mux81p	15	d to any z	tpLH	0.53	0.58	0.67	0.76	0.84
			tpHL	0.52	0.57	0.65	0.72	0.78
		a_to_z	tpLH	0.95	1.00	1.05	1.14	1.23
			tpHL	0.80	0.84	0.93	0.99	1.06
		b_to_z	tpLH	0.57	0.61	0.66	0.75	0.84
			tpHL	0.41	0.45	0.54	0.61	0.67
		c_to_z	tpLH	0.44	0.48	0.51	0.60	0.69
			tpHL	0.28	0.32	0.39	0.45	0.51

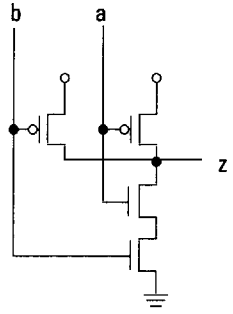
Name: nd2 Description: 2-Input NAND

Coding Syntax: z=nd2*(a,b)

Logic Symbol:



Schematics:



Truth Table:

a	*b*	*z*
0	0	1
0	1	1
1	0	1
1	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*b*
nd2	1.0	1.0
nd2p	2.0	2.0

AC Characteristics:

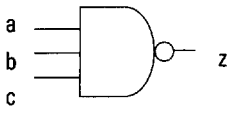
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
nd2	1	in_to_z	tpLH	0.17	0.24	0.41	0.57	0.74
			tpHL	0.18	0.25	0.37	0.51	0.65
nd2p	2	in_to_z	tpLH	0.13	0.17	0.24	0.33	0.41
			tpHL	0.15	0.18	0.25	0.31	0.38

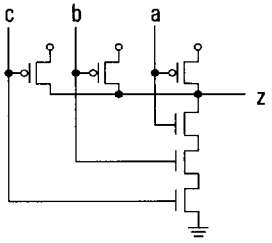
Name: nd3 Description: 3-Input NAND

Coding Syntax: z=nd3*(a,b,c)

Logic Symbol:



Schematics:



Truth Table:

a	*b*	*c*	*z*
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*b*	*c*
nd3	1.0	1.0	1.0
nd3p	2.0	2.0	2.0

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

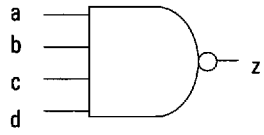
Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
nd3	2	in_to_z	tpLH	0.19	0.27	0.43	0.61	0.78
			tpHL	0.24	0.33	0.51	0.70	0.88
nd3p	3	in_to_z	tpLH	0.15	0.19	0.27	0.35	0.43
			tpHL	0.19	0.24	0.33	0.42	0.50

nd4
4-Input NAND

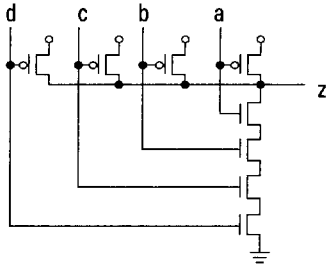
Name: nd4 Description: 4-Input NAND

Coding Syntax: z=nd4*(a,b,c,d)

Logic Symbol:



Schematics:



Truth Table:

a	*b*	*c*	*d*	*z*
0	x	x	x	1
x	0	x	x	1
x	x	0	x	1
x	x	x	0	1
1	1	1	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*b*	*c*	*d*
nd4	1.0	1.0	1.0	1.0
nd4p	2.0	2.0	2.0	2.0

AC Characteristics:

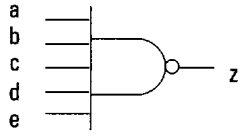
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
nd4	2	in_to_z	tpLH	0.21	0.29	0.46	0.63	0.79
			tpHL	0.30	0.42	0.66	0.91	1.16
nd4p	4	in_to_z	tpLH	0.17	0.21	0.29	0.38	0.46
			tpHL	0.25	0.30	0.42	0.53	0.65

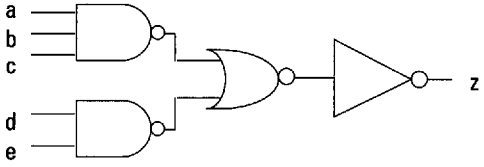
Name: nd5 Description: 5-Input NAND

Coding Syntax: z=nd5*(a,b,c,d,e)

Logic Symbol:



Schematics:



Truth Table:

a	*b*	*c*	*d*	*e*	*z*
0	x	x	x	x	1
x	0	x	x	x	1
x	x	0	x	x	1
x	x	x	0	x	1
x	x	x	x	0	1
1	1	1	1	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*b*	*c*	*d*	*e*
nd5	1.0	1.0	1.0	1.0	1.0
nd5p	1.0	1.0	1.0	1.0	1.0

AC Characteristics:

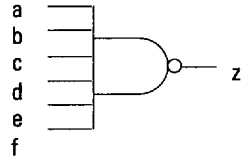
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
nd5	4	in_to_z	tpLH	0.37	0.46	0.62	0.79	0.96
			tpHL	0.49	0.54	0.64	0.72	0.81
nd5p	5	in_to_z	tpLH	0.36	0.40	0.48	0.56	0.64
			tpHL	0.52	0.55	0.61	0.67	0.71

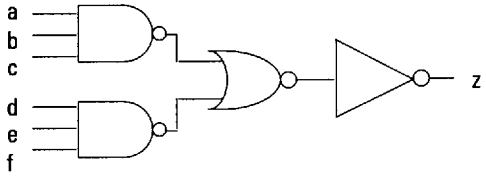
Name: nd6 Description: 6-Input NAND

Coding Syntax: z=nd6*(a,b,c,d,e,f)

Logic Symbol:



Schematics:



Truth Table:

a	*b*	*c*	*d*	*e*	*f*	*z*
0	x	x	x	x	x	1
x	0	x	x	x	x	1
x	x	0	x	x	x	1
x	x	x	0	x	x	1
x	x	x	x	0	x	1
x	x	x	x	x	0	1
1	1	1	1	1	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*b*	*c*	*d*	*e*	*f*
nd6	1.0	1.0	1.0	1.0	1.0	1.0
nd6p	1.0	1.0	1.0	1.0	1.0	1.0

AC Characteristics:

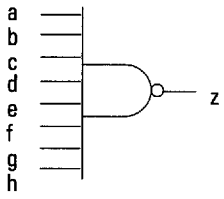
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
nd6	5	in_to_z	tpLH	0.40	0.48	0.64	0.81	0.97
			tpHL	0.52	0.57	0.67	0.75	0.84
nd6p	5	in_to_z	tpLH	0.38	0.42	0.49	0.58	0.66
			tpHL	0.55	0.58	0.65	0.70	0.75

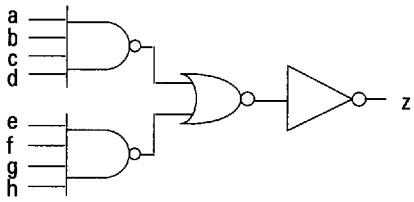
Name: nd8 Description: 8-Input NAND

Coding Syntax: z=nd8*(a,b,c,d,e,f,g,h)

Logic Symbol:



Schematics:



Truth Table:

a	*b*	*c*	*d*	*e*	*f*	*g*	*h*	*z*
0	x	x	x	x	x	x	x	1
x	0	x	x	x	x	x	x	1
x	x	0	x	x	x	x	x	1
x	x	x	0	x	x	x	x	1
x	x	x	x	0	x	x	x	1
x	x	x	x	x	0	x	x	1
x	x	x	x	x	x	0	x	1
x	x	x	x	x	x	x	0	1
1	1	1	1	1	1	1	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*b*	*c*	*d*	*e*	*f*	*g*	*h*
nd8	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
nd8p	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0

AC Characteristics:

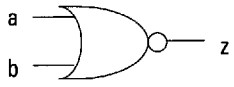
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
nd8	6	in_to_z	tpLH	0.41	0.50	0.66	0.83	1.00
			tpHL	0.58	0.64	0.74	0.82	0.90
nd8p	6	in_to_z	tpLH	0.40	0.45	0.52	0.61	0.69
			tpHL	0.63	0.66	0.72	0.78	0.82

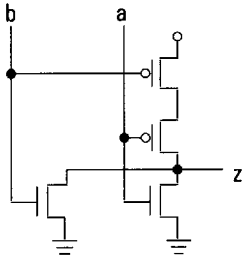
Name: nr2 Description: 2-Input NOR

Coding Syntax: z=nr2*(a,b)

Logic Symbol:



Schematics:



Truth Table:

a	*b*	*z*
0	0	1
0	1	0
1	0	0
1	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*b*
nr2	1.0	1.0
nr2p	2.0	2.0

AC Characteristics:

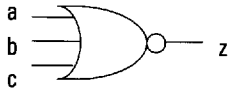
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
nr2	1	in_to_z	tpLH	0.24	0.40	0.71	1.03	1.37
			tpHL	0.14	0.18	0.26	0.34	0.42
nr2p	2	in_to_z	tpLH	0.17	0.24	0.40	0.56	0.71
			tpHL	0.11	0.14	0.18	0.22	0.26

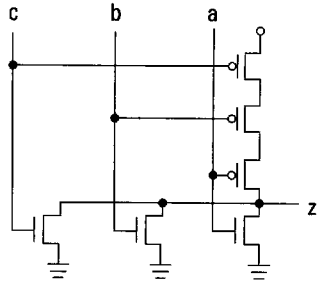
Name: nr3 Description: 3-Input NOR

Coding Syntax: z=nr3*(a,b,c)

Logic Symbol:



Schematics:



Truth Table:

a	*b*	*c*	*z*
0	0	0	1
1	x	x	0
x	1	x	0
x	x	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*b*	*c*
nr3	0.9	1.0	1.0
nr3p	1.9	2.0	2.0

AC Characteristics:

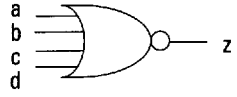
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
nr3	2	in_to_z	tpLH	0.42	0.66	1.14	1.63	2.09
			tpHL	0.16	0.21	0.29	0.37	0.46
nr3p	3	in_to_z	tpLH	0.31	0.42	0.66	0.89	1.14
			tpHL	0.14	0.17	0.21	0.25	0.29

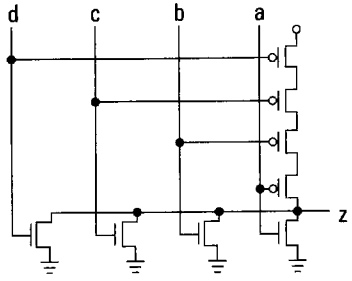
Name: nr4 Description: 4-Input NOR

Coding Syntax: z=nr4*(a,b,c,d)

Logic Symbol:



Schematics:



Truth Table:

a	*b*	*c*	*d*	*z*
0	0	0	0	1
1	x	x	x	0
x	1	x	x	0
x	x	1	x	0
x	x	x	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*b*	*c*	*d*
nr4	0.9	0.9	1.0	1.0
nr4p	1.9	1.9	2.0	2.0

AC Characteristics:

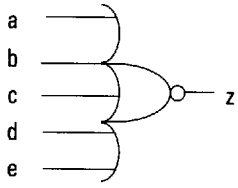
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

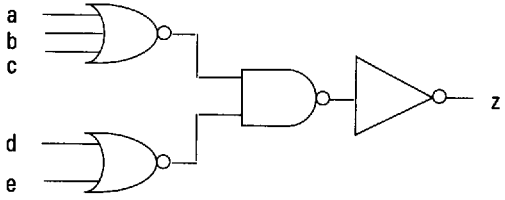
Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
nr4	2	in_to_z	tpLH	0.57	0.90	1.52	2.15	2.78
			tpHL	0.17	0.22	0.30	0.38	0.46
nr4p	4	in_to_z	tpLH	0.42	0.57	0.89	1.22	1.53
			tpHL	0.15	0.17	0.22	0.25	0.30

Name: nr5 Description: 5-Input NOR

Coding Syntax: z=nr5*(a,b,c,d,e)

Logic Symbol: Schematics:





Truth Table:

a	*b*	*c*	*d*	*e*	*z*
0	0	0	0	0	1
1	x	x	x	x	0
x	1	x	x	x	0
x	x	1	x	x	0
x	x	x	1	x	0
x	x	x	x	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*b*	*c*	*d*	*e*
nr5	1.0	1.0	1.0	1.0	1.0
nr5p	1.0	1.0	1.0	1.0	1.0

AC Characteristics:

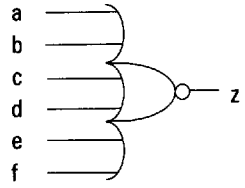
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
nr5	4	in_to_z	tpLH	0.56	0.64	0.81	0.97	1.15
			tpHL	0.37	0.42	0.50	0.58	0.66
nr5p	5	in_to_z	tpLH	0.55	0.59	0.68	0.76	0.85
			tpHL	0.37	0.40	0.45	0.50	0.54

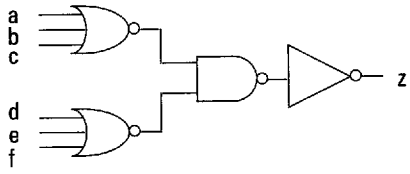
Name: nr6 Description: 6-Input NOR

Coding Syntax: z=nr6*(a,b,c,d,e,f)

Logic Symbol:



Schematics:



Truth Table:

a	*b*	*c*	*d*	*e*	*f*	*z*
0	0	0	0	0	0	1
1	x	x	x	x	x	0
x	1	x	x	x	x	0
x	x	1	x	x	x	0
x	x	x	1	x	x	0
x	x	x	x	1	x	0
x	x	x	x	x	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*b*	*c*	*d*	*e*	*f*
nr6	1.0	1.0	1.0	1.0	1.0	1.0
nr6p	1.0	1.0	1.0	1.0	1.0	1.0

AC Characteristics:

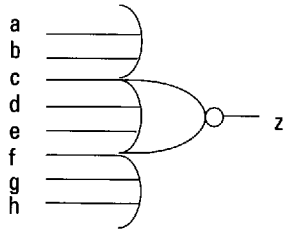
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
nr6	5	in_to_z	tpLH	0.64	0.73	0.90	1.06	1.23
			tpHL	0.38	0.43	0.52	0.60	0.67
nr6p	5	in_to_z	tpLH	0.64	0.68	0.77	0.85	0.93
			tpHL	0.39	0.42	0.47	0.52	0.56

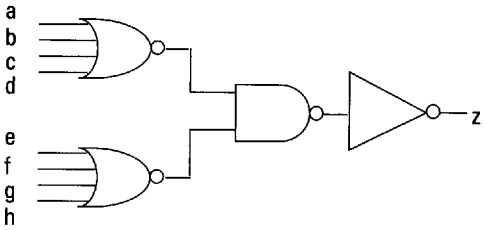
Name: nr8 Description: 8-Input NOR

Coding Syntax: z=nr8*(a,b,c,d,e,f,g,h)

Logic Symbol:



Schematics:



Truth Table:

a	*b*	*c*	*d*	*e*	*f*	*g*	*h*	*z*
0	0	0	0	0	0	0	0	1
1	x	x	x	x	x	x	x	0
x	1	x	x	x	x	x	x	0
x	x	1	x	x	x	x	x	0
x	x	x	1	x	x	x	x	0
x	x	x	x	1	x	x	x	0
x	x	x	x	x	1	x	x	0
x	x	x	x	x	x	1	x	0
x	x	x	x	x	x	x	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*b*	*c*	*d*	*e*	*f*	*g*	*h*
nr8	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
nr8p	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

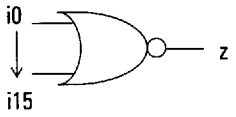
Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
nr8	6	in_to_z	tpLH	0.73	0.81	0.98	1.15	1.32
			tpHL	0.38	0.42	0.50	0.58	0.66
nr8p	6	in_to_z	tpLH	0.73	0.77	0.87	0.95	1.02
			tpHL	0.38	0.41	0.46	0.51	0.54

Name: nr16

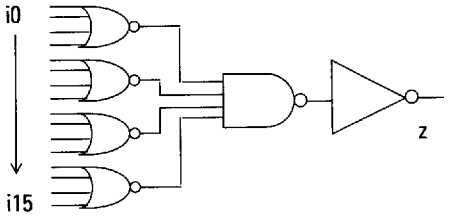
Description: 16-Input NOR

Coding Syntax: z=nr16*(i0,i1,i2,i3,i4,i5,i6,i7,i8,i9,i10,i11,i12,i13,i14,i15)

Logic Symbol:



Schematics:



Truth Table:

io	*i1*	*i2*	*i3*	*i4*	*i5*	*i6*	*i7*	*i8*	*i9*	*i10*	*i11*	*i12*	*i13*	*i14*	*i15*	*z*
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0
x	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0
x	x	1	x	x	x	x	x	x	x	x	x	x	x	x	x	0
x	x	x	1	x	x	x	x	x	x	x	x	x	x	x	x	0
x	x	x	x	1	x	x	x	x	x	x	x	x	x	x	x	0
x	x	x	x	x	1	x	x	x	x	x	x	x	x	x	x	0
x	x	x	x	x	x	1	x	x	x	x	x	x	x	x	x	0
x	x	x	x	x	x	x	1	x	x	x	x	x	x	x	x	0
x	x	x	x	x	x	x	x	1	x	x	x	x	x	x	x	0
x	x	x	x	x	x	x	x	x	1	x	x	x	x	x	x	0
x	x	x	x	x	x	x	x	x	x	1	x	x	x	x	x	0
x	x	x	x	x	x	x	x	x	x	x	1	x	x	x	x	0
x	x	x	x	x	x	x	x	x	x	x	x	1	x	x	x	0
x	x	x	x	x	x	x	x	x	x	x	x	x	1	x	x	0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	1	x	0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*i0*	*i1*	*i2*	*i3*	*i4*	*i5*	*i6*	*i7*	*i8*	*i9*	*i10*	*i11*	*i12*	*i13*	*i14*	*i15*
nr16	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
nr16p	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

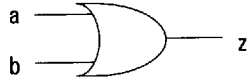
Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
nr16	11	in_to_z	tpLH	0.86	0.95	1.14	1.30	1.48
			tpHL	0.42	0.47	0.56	0.64	0.72
nr16p	11	in_to_z	tpLH	0.88	0.92	1.02	1.12	1.20
			tpHL	0.41	0.45	0.51	0.55	0.59

or2
2-Input OR

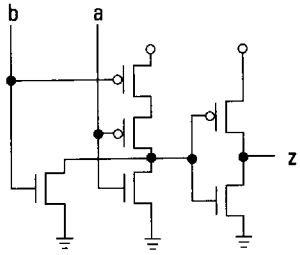
Name: or2 Description: 2-Input OR

Coding Syntax: z=or2*(a,b)

Logic Symbol:



Schematics:



Truth Table:

a	*b*	*z*
0	0	0
0	1	1
1	0	1
1	1	1

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*b*
or2	1.0	1.0
or2p	1.0	1.0

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

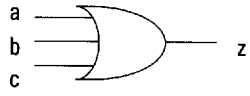
Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
or2	2	in_to_z	tpLH	0.25	0.33	0.49	0.66	0.82
			tpHL	0.29	0.34	0.43	0.52	0.61
or2p	2	in_to_z	tpLH	0.22	0.26	0.34	0.42	0.50
			tpHL	0.32	0.36	0.41	0.47	0.51

Name: or3

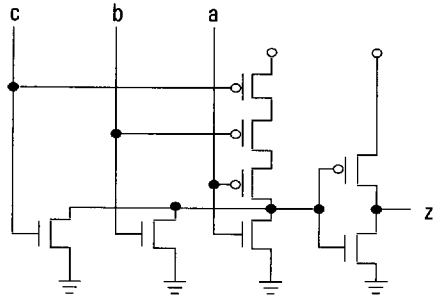
Description: 3-Input OR

Coding Syntax: z=or3*(a,b,c)

Logic Symbol:



Schematics:



Truth Table:

a	*b*	*c*	*z*
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*b*	*c*
or3	1.0	1.0	1.0
or3p	1.0	1.0	1.0

AC Characteristics:

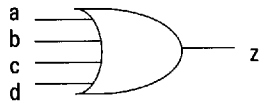
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
or3	2	in_to_z	tpLH	0.28	0.36	0.53	0.70	0.87
			tpHL	0.45	0.51	0.62	0.72	0.81
or3p	3	in_to_z	tpLH	0.25	0.30	0.38	0.46	0.54
			tpHL	0.49	0.54	0.62	0.67	0.73

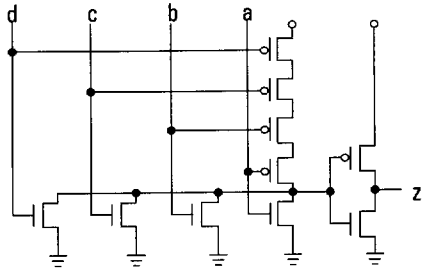
Name: or4 Description: 4-Input OR

Coding Syntax: z=or4*(a,b,c,d)

Logic Symbol:



Schematics:



Truth Table:

a	*b*	*c*	*d*	*z*
0	0	0	0	0
1	x	x	x	1
x	1	x	x	1
x	x	1	x	1
x	x	x	1	1

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*b*	*c*	*d*
or4	1.0	1.0	1.0	1.0
or4p	1.0	1.0	1.0	1.0

AC Characteristics:

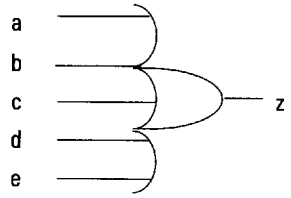
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
or4	3	in_to_z	tpLH	0.28	0.36	0.53	0.70	0.87
			tpHL	0.56	0.64	0.76	0.87	0.98
or4p	3	in_to_z	tpLH	0.26	0.31	0.39	0.47	0.56
			tpHL	0.64	0.69	0.78	0.84	0.90

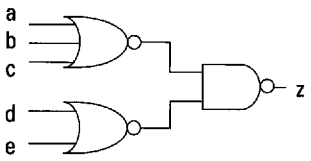
Name: or5 Description: 5-Input OR

Coding Syntax: z=or5*(a,b,c,d,e)

Logic Symbol:



Schematics:



Truth Table:

a	*b*	*c*	*d*	*e*	*z*
0	0	0	0	0	0
1	x	x	x	x	1
x	1	x	x	x	1
x	x	1	x	x	1
x	x	x	1	x	1
x	x	x	x	1	1

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*b*	*c*	*d*	*e*
or5	1.0	1.0	1.0	1.0	1.0
or5p	1.0	1.0	1.0	1.0	1.0

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
or5	4	in_to_z	tpLH	0.29	0.37	0.54	0.70	0.87
			tpHL	0.44	0.52	0.65	0.80	0.94
or5p	5	in_to_z	tpLH	0.29	0.32	0.40	0.49	0.57
			tpHL	0.50	0.54	0.62	0.69	0.76

2.2 Internal Buffers

This section contains data pages for LCA300K internal buffers

Naming Conventions

An internal buffer root name is given at the top of each data page. High output drive strength is indicated by the suffix `p`. Internal buffer names with no suffix have a standard output drive strength.

For example:

`b2ip` has high output drive strength.

`b2i` has standard output drive strength.

➤ ***Note:*** For the coding syntax, an asterisk following the cell name (for example, `b2i*`) is a wildcard symbol for the `p` option.

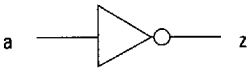
b1a
Inverting Power Buffer

Name: b1a

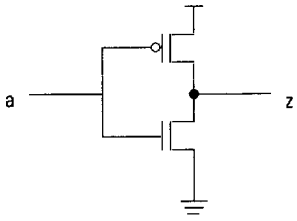
Description: Inverting Power Buffer

Coding Syntax: z=b1a(a)

Logic Symbol:



Schematics:



Truth Table:

a	*z*
0	1
1	0

Loading Characteristics:

Values stated in standard loads.

Version	*a*
b1a	4.4

AC Characteristics:

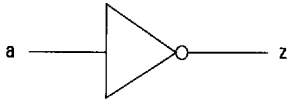
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

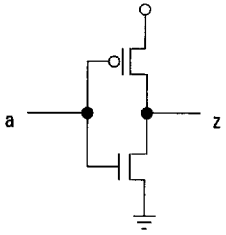
Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				4	*8*	*16*	*32*	*64*
b1a	3	a_to_z	tpLH	0.09	0.11	0.16	0.27	0.50
			tpHL	0.11	0.13	0.19	0.30	0.51

Name: b2a Description: Inverting Buffer, 2 Parallel IVAPs

Coding Syntax: z=b2a(a)

Logic Symbol: Schematics:





Truth Table:

a	*z*
0	1
1	0

Loading Characteristics:

Values stated in standard loads.

Version	*a*
b2a	6.3

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				4	*8*	*16*	*32*	*64*
b2a	4	a_to_z	tpLH	0.07	0.10	0.13	0.21	0.38
			tpHL	0.08	0.11	0.15	0.24	0.40

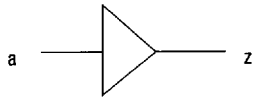
b3a
Power Buffer

Name: b3a

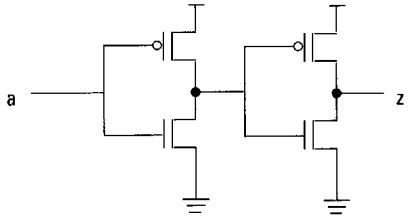
Description: Power Buffer

Coding Syntax: z=b3a(a)

Logic Symbol:



Schematics:



Truth Table:

a	*z*
0	0
1	1

Loading Characteristics:

Values stated in standard loads.

Version	*a*
b3a	5.8

AC Characteristics:

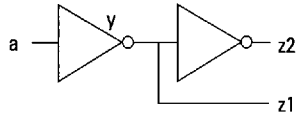
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

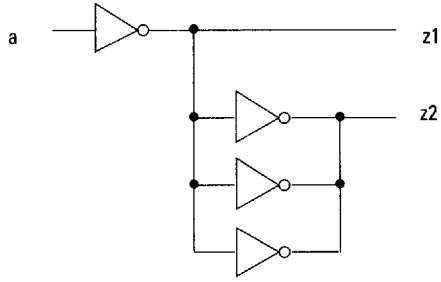
Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				4	*8*	*16*	*32*	*64*
b3a	3	a_to_z	tpLH	0.07	0.10	0.15	0.26	0.49
			tpHL	0.08	0.10	0.13	0.19	0.29

Name: b2i Description: Inverter into 3 Parallel Inverters

Coding Syntax: u(z1,z2)=b2i*(a)

Logic Symbol: Schematics:





Truth Table:

a	*z1*	*z2*
1	0	1
0	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*a*
b2i	1.0
b2ip	2.0

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				4	*8*	*16*	*32*	*64*
b2i	2	a_to_z1	tpLH	0.33	0.51	0.88	1.58	2.99
			tpHL	0.22	0.31	0.48	0.83	1.52
		a_to_z2	tpLH	0.37	0.44	0.55	0.78	1.26
			tpHL	0.39	0.44	0.53	0.66	0.90
b2ip	4	a_to_z1	tpLH	0.24	0.32	0.50	0.86	1.57
			tpHL	0.17	0.21	0.30	0.47	0.82
		a_to_z2	tpLH	0.27	0.30	0.36	0.47	0.69
			tpHL	0.27	0.30	0.35	0.42	0.55

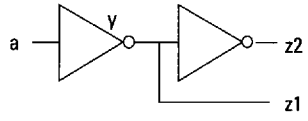
2 Parallel Inverters into 2 Parallel Inverters

Name: b3i

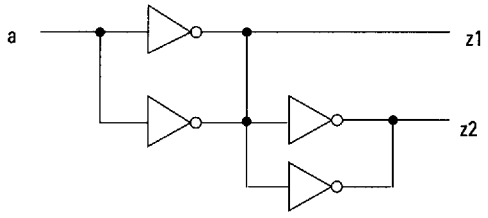
Description: 2 Parallel Inverters into 2 Parallel Inverters

Coding Syntax: u(z1,z2)=b3i*(a)

Logic Symbol:



Schematics:



Truth Table:

a	*z1*	*z2*
1	0	1
0	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*a*
b3i	2.0
b3ip	4.1

AC Characteristics:

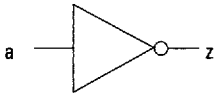
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

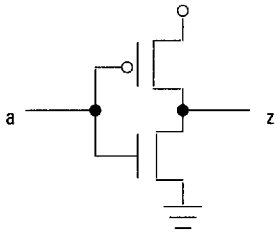
Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				4	*8*	*16*	*32*	*64*
b3i	2	a_to_z1	tpLH	0.16	0.24	0.41	0.78	1.49
			tpHL	0.14	0.18	0.26	0.43	0.78
		a_to_z2	tpLH	0.27	0.36	0.52	0.86	1.57
			tpHL	0.25	0.30	0.40	0.56	0.90
b3ip	4	a_to_z1	tpLH	0.12	0.16	0.24	0.41	0.78
			tpHL	0.11	0.14	0.18	0.26	0.43
		a_to_z2	tpLH	0.20	0.24	0.33	0.48	0.84
			tpHL	0.17	0.20	0.25	0.34	0.50

Name: b4i Description: 4 Parallel Inverters

Coding Syntax: z=b4i*(a)

Logic Symbol: Schematics:





Truth Table:

a	*z*
1	0
0	1

Loading Characteristics:

Values stated in standard loads.

Version	*a*
b4i	4.1
b4ip	8.2

AC Characteristics:

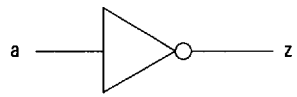
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

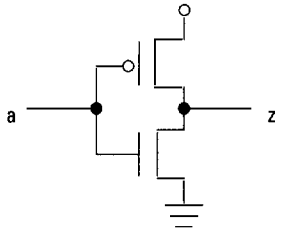
Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				4	*8*	*16*	*32*	*64*
b4i	2	a_to_z	tpLH	0.08	0.12	0.20	0.37	0.74
			tpHL	0.08	0.11	0.16	0.24	0.41
b4ip	4	a_to_z	tpLH	0.07	0.08	0.12	0.20	0.37
			tpHL	0.07	0.08	0.11	0.16	0.24

Name: b5i Description: 3 Parallel Inverters

Coding Syntax: z=b5i*(a)

Logic Symbol: Schematics:





Truth Table:

a	*z*
1	0
0	1

Loading Characteristics:

Values stated in standard loads.

Version	*a*
b5i	3.1
b5ip	6.1

AC Characteristics:

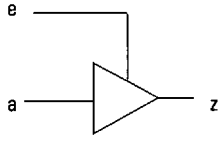
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

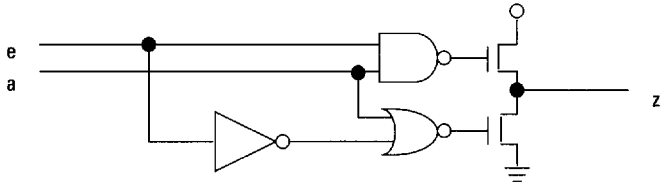
Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				4	*8*	*16*	*32*	*64*
b5i	2	a_to_z	tpLH	0.10	0.15	0.26	0.49	0.98
			tpHL	0.10	0.13	0.19	0.30	0.53
b5ip	3	a_to_z	tpLH	0.08	0.10	0.15	0.26	0.50
			tpHL	0.07	0.10	0.13	0.19	0.30

Name: bts4 Description: 3-State Internal Bus Driver

Coding Syntax: z=bts4*(a,e)

Logic Symbol: Schematics:





Truth Table:

a	*e*	*z*
x	0	hi-z
1	1	1
0	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*e*
bts4	2.0	1.6
bts4p	2.0	1.6

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
bts4	3	a_to_z	tpLH	0.25	0.34	0.50	0.67	0.85
			tpHL	0.27	0.32	0.41	0.49	0.57
		e_to_z	tpLH	0.22	0.35	0.47	0.64	0.82
			tpHL	0.31	0.37	0.46	0.54	0.62
bts4p	4	a_to_z	tpLH	0.22	0.27	0.35	0.43	0.51
			tpHL	0.25	0.28	0.34	0.39	0.43
		e_to_z	tpLH	0.23	0.29	0.37	0.46	0.54
			tpHL	0.29	0.33	0.38	0.43	0.48

bts4n

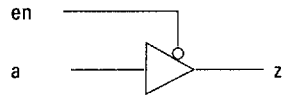
Internal 3-State Bus Driver with Enable Low

Name: bts4n

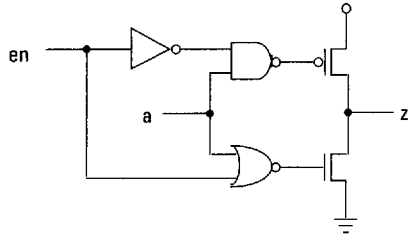
Description: Internal 3-State Bus Driver with Enable Low

Coding Syntax: z=bts4n*(a,en)

Logic Symbol:



Schematics:



Truth Table:

a	*en*	*z*
x	1	hi-z
0	0	0
1	0	1

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*en*
bts4n	2.0	1.9
bts4np	2.0	1.9

AC Characteristics:

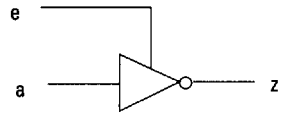
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
bts4n	3	a_to_z	tpLH	0.25	0.34	0.50	0.67	0.85
			tpHL	0.25	0.30	0.38	0.47	0.55
		en_to_z	tpLH	0.29	0.38	0.54	0.71	0.89
			tpHL	0.20	0.32	0.41	0.55	0.63
bts4np	4	a_to_z	tpLH	0.22	0.26	0.35	0.43	0.51
			tpHL	0.23	0.27	0.32	0.37	0.41
		en_to_z	tpLH	0.27	0.31	0.39	0.48	0.56
			tpHL	0.25	0.28	0.34	0.40	0.46

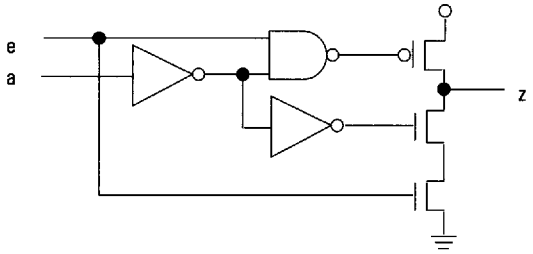
Name: bts5 Description: Inverting 3-State Internal Bus Driver

Coding Syntax: z=bts5*(a,e)

Logic Symbol:



Schematics:



Truth Table:

a	*e*	*z*
x	0	hi-z
1	1	0
0	1	1

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*e*
bts5	1.0	1.1
bts5p	1.0	1.5

AC Characteristics:

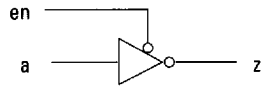
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
bts5	3	a_to_z	tpLH	0.42	0.52	0.62	0.79	0.97
			tpHL	0.35	0.41	0.53	0.67	0.81
		e_to_z	tpLH	0.56	0.71	0.77	0.97	1.08
			tpHL	0.16	0.22	0.35	0.48	0.62
bts5p	4	a_to_z	tpLH	0.46	0.54	0.62	0.56	0.65
			tpHL	0.33	0.36	0.43	0.49	0.55
		e_to_z	tpLH	0.57	0.68	0.81	0.82	0.96
			tpHL	0.12	0.15	0.22	0.28	0.35

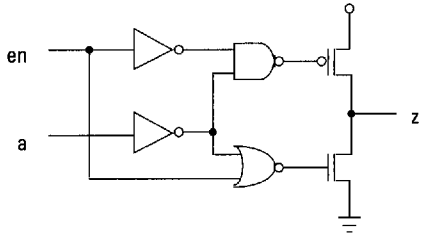
Name: bts5n Description: Internal Inverting 3-State Bus Driver with Enable Low

Coding Syntax: z=bts5n*(a,en)

Logic Symbol:



Schematics:



Truth Table:

a	*en*	*z*
x	1	hi-z
0	0	1
1	0	0

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*en*
bts5n	1.0	1.9
bts5np	1.0	1.9

AC Characteristics:

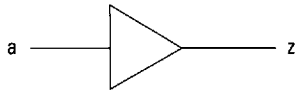
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

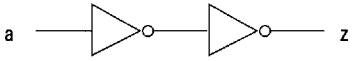
Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
bts5n	4	a_to_z	tpLH	0.36	0.44	0.60	0.77	0.95
			tpHL	0.37	0.42	0.52	0.60	0.68
		en_to_z	tpLH	0.29	0.37	0.53	0.70	0.88
			tpHL	0.29	0.35	0.51	0.60	0.69
bts5np	4	a_to_z	tpLH	0.33	0.38	0.46	0.55	0.63
			tpHL	0.34	0.37	0.43	0.48	0.52
		en_to_z	tpLH	0.32	0.34	0.39	0.48	0.56
			tpHL	0.24	0.27	0.33	0.38	0.43

Name: buf8a Description: Non-Inverting Buffer, IVP Driving 2 Parallel IVAPs

Coding Syntax: z=buf8a(a)

Logic Symbol: Schematics:





Truth Table:

a	*z*
0	0
1	1

Loading Characteristics:

Values stated in standard loads.

Version	*a*
buf8a	2.0

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*16*	*32*
buf8a	5	a_to_z	tpLH	0.17	0.18	0.21	0.25	0.33
			tpHL	0.26	0.27	0.29	0.35	0.43

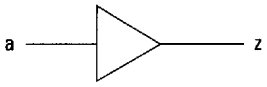
delay1

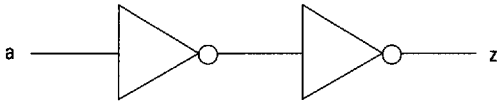
Internal Buffer with 1 ns Nominal Delay

Name: delay1 Description: Internal Buffer with 1 ns Nominal Delay

Coding Syntax: z=delay1(a)

Logic Symbol: Schematics:





Truth Table:

a	*z*
0	0
1	1

Loading Characteristics:

Values stated in standard loads.

Version	*a*
delay1	1.0

AC Characteristics:

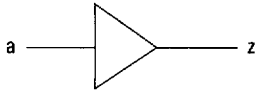
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

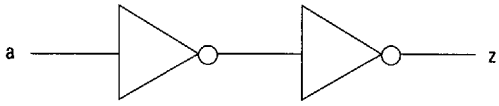
Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
delay1	5	a_to_z	tpLH	0.85	0.89	0.97	1.05	1.13
			tpHL	0.98	1.01	1.06	1.10	1.15

Name: delay2 Description: Internal Buffer with 2 ns Nominal Delay

Coding Syntax: z=delay2(a)

Logic Symbol: Schematics:





Truth Table:

a	*z*
0	0
1	1

Loading Characteristics:

Values stated in standard loads.

Version	*a*
delay2	1.0

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
delay2	8	a_to_z	tpLH	1.83	1.87	1.95	2.04	2.12
			tpHL	2.00	2.04	2.12	2.18	2.23

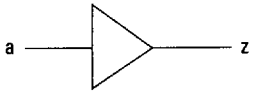
delay3

Internal Buffer with 3 ns Nominal Delay

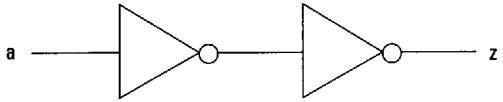
Name: delay3 Description: Internal Buffer with 3 ns Nominal Delay

Coding Syntax: z=delay3(a)

Logic Symbol:



Schematics:



Truth Table:

a	*z*
0	0
1	1

Loading Characteristics:

Values stated in standard loads.

Version	*a*
delay3	1.0

AC Characteristics:

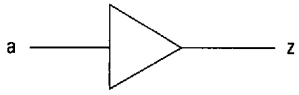
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

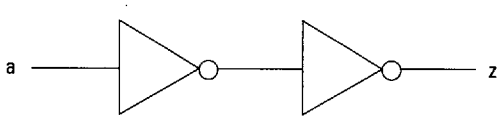
Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
delay3	11	a_to_z	tpLH	2.93	2.98	3.06	3.15	3.24
			tpHL	2.87	2.91	2.97	3.02	3.07

Name: delay4 Description: Internal Buffer with 4 ns Nominal Delay

Coding Syntax: z=delay4(a)

Logic Symbol: Schematics:





Truth Table:

a	*z*
0	0
1	1

Loading Characteristics:

Values stated in standard loads.

Version	*a*
delay4	1.0

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
delay4	10	a_to_z	tpLH	3.96	4.01	4.10	4.19	4.27
			tpHL	3.90	3.95	4.00	4.06	4.11

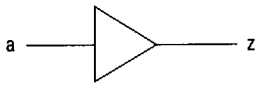
delay5

Internal Buffer with 5 ns Nominal Delay

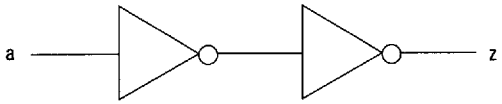
Name: delay5 Description: Internal Buffer with 5 ns Nominal Delay

Coding Syntax: z=delay5(a)

Logic Symbol:



Schematics:



Truth Table:

a	*z*
0	0
1	1

Loading Characteristics:

Values stated in standard loads.

Version	*a*
delay5	1.0

AC Characteristics:

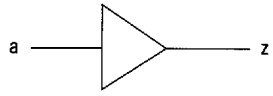
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

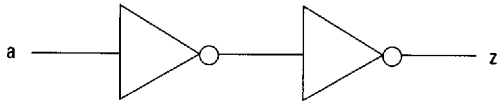
Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
delay5	11	a_to_z	tpLH	4.89	4.94	5.02	5.10	5.18
			tpHL	5.04	5.07	5.14	5.19	5.24

Name: delay10 Description: Internal Buffer with 10 ns Nominal Delay

Coding Syntax: z=delay10(a)

Logic Symbol: Schematics:





Truth Table:

a	*z*
0	0
1	1

Loading Characteristics:

Values stated in standard loads.

Version	*a*
delay10	1.0

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
delay10	20	a_to_z	tpLH	9.89	9.93	10.01	10.09	10.18
			tpHL	10.19	10.23	10.29	10.35	10.39

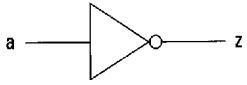
iv
Inverter

Name: iv

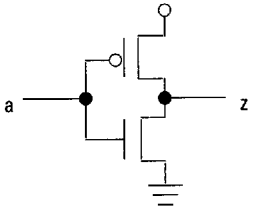
Description: Inverter

Coding Syntax: z=iv*(a)

Logic Symbol:



Schematics:



Truth Table:

a	*z*
1	0
0	1

Loading Characteristics:

Values stated in standard loads.

Version	*a*
iv	1.02
ivp	2.0

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

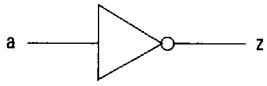
Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
iv	1	a_to_z	tpLH	0.13	0.21	0.37	0.54	0.73
			tpHL	0.12	0.16	0.24	0.32	0.40
ivp	1	a_to_z	tpLH	0.08	0.12	0.20	0.28	0.36
			tpHL	0.08	0.11	0.15	0.20	0.24

Name: iva

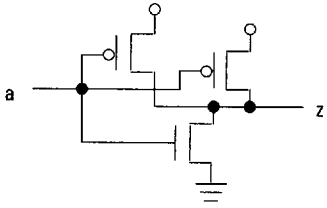
Description: Inverter with Parallel P Transistors

Coding Syntax: z=iva*(a)

Logic Symbol:



Schematics:



Truth Table:

a	*z*
1	0
0	1

Loading Characteristics:

Values stated in standard loads.

Version	*a*
iva	1.6
ivap	3.1

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
iva	1	a_to_z	tpLH	0.11	0.14	0.22	0.30	0.38
			tpHL	0.12	0.17	0.25	0.32	0.40
ivap	2	a_to_z	tpLH	0.09	0.11	0.14	0.18	0.22
			tpHL	0.10	0.12	0.17	0.20	0.25

ivda

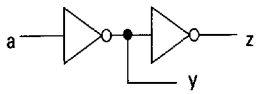
Inverter into Inverter

Name: ivda

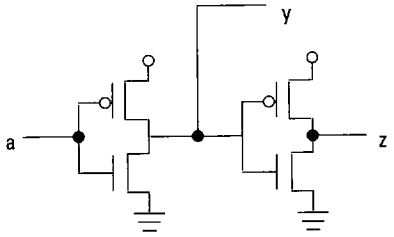
Description: Inverter into Inverter

Coding Syntax: u(y,z)=ivda(a)

Logic Symbol:



Schematics:



Truth Table:

a	*y*	*z*
0	1	0
1	0	1

Loading Characteristics:

Values stated in standard loads.

Version	*a*
ivda	1.0
ivdap	2.0

AC Characteristics:

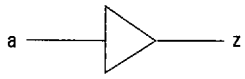
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

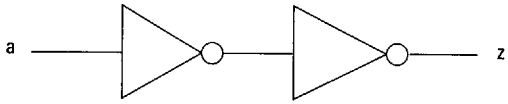
Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*3*	*4*	*8*	*16*
ivda	1	a_to_y	tpLH	0.17	0.25	0.41	0.59	0.77
			tpHL	0.14	0.18	0.26	0.34	0.42
		a_to_z	tpLH	0.27	0.35	0.51	0.68	0.86
			tpHL	0.23	0.28	0.37	0.44	0.52
ivdap	2	a_to_y	tpLH	0.12	0.16	0.24	0.32	0.40
			tpHL	0.11	0.13	0.18	0.21	0.26
		a_to_z	tpLH	0.19	0.23	0.30	0.38	0.47
			tpHL	0.15	0.17	0.23	0.27	0.31

Name: lclkbuf1 Description: Local Clock Buffer

Coding Syntax: z=lclkbuf1(a)

Logic Symbol: Schematics:





Truth Table:

a	*z*
0	0
1	1

Loading Characteristics:

Values stated in standard loads.

Version	*a*
lclkbuf1	1.0

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

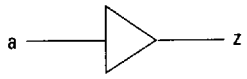
Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
lclkbuf1	2	a_to_z	tpLH	0.19	0.22	0.28	0.33	0.39
			tpHL	0.25	0.28	0.33	0.37	0.41

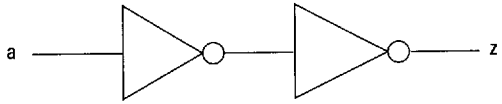
lclkbuf2
Local Clock Buffer

Name: lclkbuf2 Description: Local Clock Buffer

Coding Syntax: z=lclkbuf2(a)

Logic Symbol: Schematics:





Truth Table:

a	*z*
0	0
1	1

Loading Characteristics:

Values stated in standard loads.

Version	*a*
lclkbuf2	2.0

AC Characteristics:

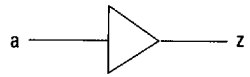
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

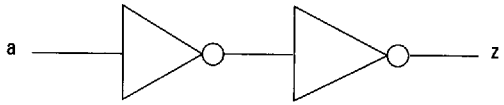
Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
lclkbuf2	3	a_to_z	tpLH	0.16	0.18	0.22	0.26	0.30
			tpHL	0.18	0.20	0.24	0.26	0.29

Name: lclkbuf3 Description: Local Clock Buffer

Coding Syntax: z=lclkbuf3(a)

Logic Symbol: Schematics:





Truth Table:

a	*z*
0	0
1	1

Loading Characteristics:

Values stated in standard loads.

Version	*a*
lclkbuf3	2.0

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*16*	*32*
lclkbuf3	4	a_to_z	tpLH	0.19	0.20	0.23	0.30	0.43
			tpHL	0.19	0.21	0.24	0.28	0.35

2.3 Flip-Flops

This section contains data pages for LCA300K flip-flops.

Naming Conventions

A flip-flop root name is given at the top of each data page. Flip-flop names with the suffix `p` have a high output drive strength. Flip-flop names with no suffix have a standard output drive strength.

For example:

`fd1p` has high output drive strength.

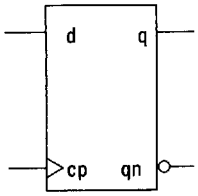
`fd1` has standard output drive strength.

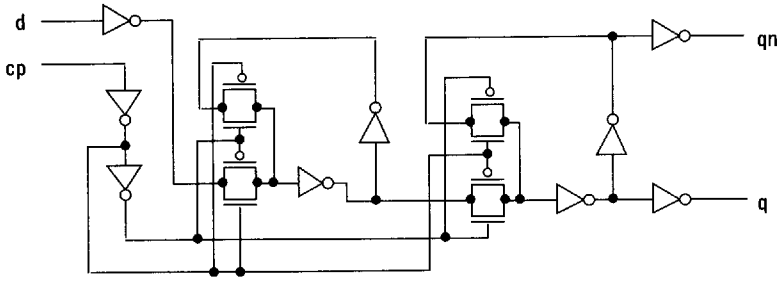
➤ ***Note:*** For the coding syntax, an asterisk following the cell name (for example, `fd1*`) is a wildcard symbol for the `p` option.

Name: fd1 Description: D Flip-Flop

Coding Syntax: u(q,qn)=fd1*(d,cp)

Logic Symbol: Schematics:





Truth Table:

d	*cp*	*q*	*qn*
0	↑	0	1
1	↑	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*d*	*cp*
fd1	1.0	1.0
fd1p	1.0	1.0

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fd1	7	cp_to_q	tpLH	0.96	1.04	1.21	1.38	1.56
			tpHL	0.99	1.04	1.13	1.22	1.29
		cp_to_qn	tpLH	1.14	1.22	1.38	1.55	1.73
			tpHL	1.07	1.12	1.20	1.28	1.37
fd1p	8	cp_to_q	tpLH	0.95	0.99	1.06	1.14	1.23
			tpHL	0.99	1.03	1.08	1.13	1.17
		cp_to_qn	tpLH	1.17	1.21	1.29	1.37	1.45
			tpHL	1.11	1.14	1.19	1.24	1.29

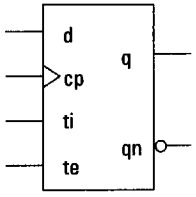
Timing Constraints:

Version	*Parameters*	*Value*	*Version*	*Parameters*	*Value*
fd1	d_setup	0.31	fd1p	d_setup	0.30
	d_hold	0.08		d_hold	0.09
	cp_pw0	0.38		cp_pw0	0.40
	cp_pw1	0.47		cp_pw1	0.47

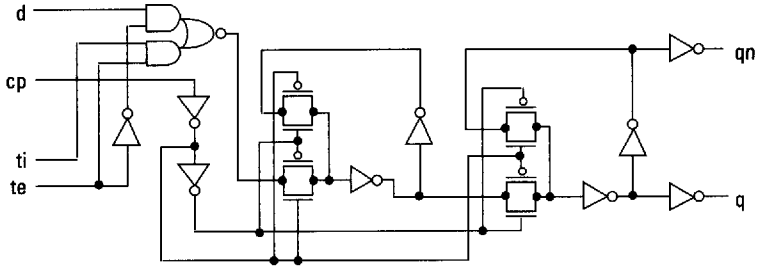
Name: fd1s Description: D Flip-Flop with Scan

Coding Syntax: u(q,qn)=fd1s*(d,cp,ti,te)

Logic Symbol:



Schematics:



Truth Table:

d	*ti*	*te*	*cp*	*q*	*qn*
0	x	0	↑	0	1
1	x	0	↑	1	0
x	0	1	↑	0	1
x	1	1	↑	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*d*	*cp*	*ti*	*te*
fd1s	1.0	1.0	1.0	2.0
fd1sp	1.0	1.0	1.0	2.0

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fd1s	9	cp_to_qn	tpLH	1.13	1.20	1.37	1.54	1.72
			tpHL	1.06	1.10	1.19	1.27	1.35
		cp_to_q	tpLH	0.95	1.03	1.19	1.36	1.55
			tpHL	0.98	1.03	1.12	1.20	1.28
fd1sp	10	cp_to_qn	tpLH	1.16	1.20	1.28	1.36	1.44
			tpHL	1.09	1.13	1.18	1.23	1.27
		cp_to_q	tpLH	0.93	0.97	1.05	1.13	1.21
			tpHL	0.98	1.01	1.07	1.11	1.16

Timing Constraints:

Version	*Parameters*	*Value*	*Version*	*Parameters*	*Value*
fd1s	d_setup	0.57	fd1sp	d_setup	0.56
	d_hold	0.00		d_hold	0.10
	ti_setup	0.57		ti_setup	0.56
	ti_hold	0.00		ti_hold	0.10
	te_setup	0.74		te_setup	0.61
	te_hold	-0.18		te_hold	0.05
	cp_pw0	0.57		cp_pw0	0.45
	cp_pw1	0.47		cp_pw1	0.47

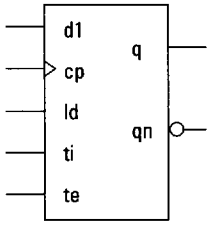
fd1sl
D Flip-Flop with Enable Scan

Name: fd1sl

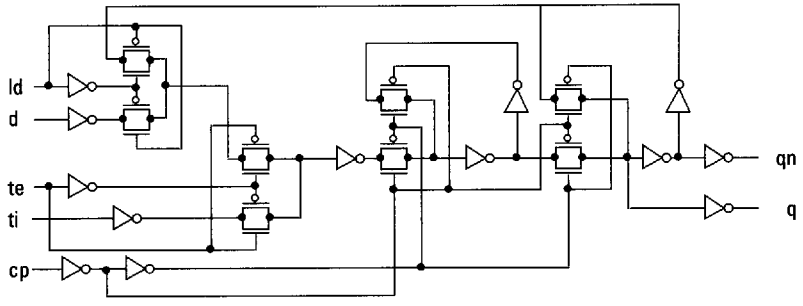
Description: D Flip-Flop with Enable Scan

Coding Syntax: u(q,qn)=fd1sl*(d,cp,ld,ti,te)

Logic Symbol:



Schematics:



Truth Table:

d	*ti*	*te*	*cp*	*ld*	*q*	*qn*
0	x	0	↑	1	0	1
1	x	0	↑	1	1	0
x	0	1	↑	x	0	1
x	1	1	↑	x	1	0
x	x	0	↑	0	q	qn

Loading Characteristics:

Values stated in standard loads.

Version	*d*	*cp*	*ld*	*ti*	*te*
fd1sl	1.0	1.0	1.9	1.0	1.9
fd1slp	1.0	1.0	1.9	1.0	1.9

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fd1sl	11	cp_to_qn	tpLH	1.02	1.10	1.26	1.43	1.62
			tpHL	1.03	1.08	1.17	1.25	1.33
		cp_to_q	tpLH	0.91	1.00	1.16	1.33	1.52
			tpHL	0.87	0.93	1.04	1.13	1.23

AC Characteristics: (Cont.)

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fd1slp	12	cp_to_qn	tpLH	1.06	1.11	1.19	1.27	1.35
			tpHL	1.07	1.11	1.16	1.21	1.26
		cp_to_q	tpLH	0.88	0.93	1.02	1.10	1.19
			tpHL	0.86	0.90	0.97	1.03	1.08

Timing Constraints:

Version	*Parameters*	*Value*	*Version*	*Parameters*	*Value*
fd1sl	d_setup	0.83	fd1slp	d_setup	0.80
	d_hold	-0.17		d_hold	-0.02
	ld_setup	0.65		ld_setup	0.65
	ld_hold	-0.17		ld_hold	-0.02
	ti_setup	0.57		ti_setup	0.55
	ti_hold	0.03		ti_hold	0.19
	te_setup	0.35		te_setup	0.34
	te_hold	0.13		te_hold	0.30
	cp_pw0	0.48		cp_pw0	0.63
	cp_pw1	0.47		cp_pw1	0.47

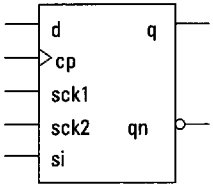
fd1s2
D Flip-Flop with 2 Scan Clock Control

Name: fd1s2

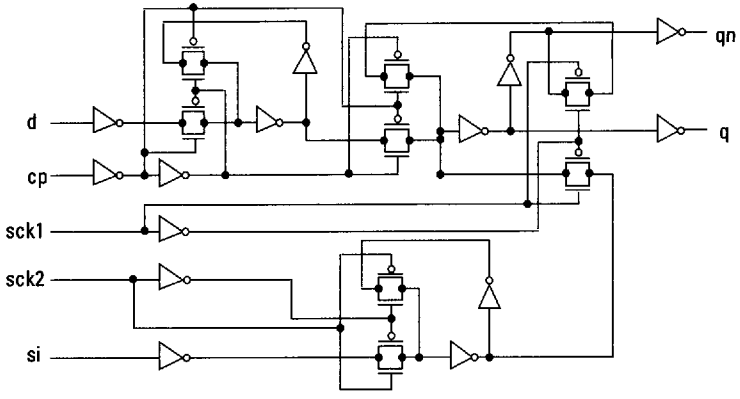
Description: D Flip-Flop with 2 Scan Clock Control

Coding Syntax: u(q,qn)=fd1s2*(d,cp,sck1,sck2,si)

Logic Symbol:



Schematics:



Truth Table:

d	*cp*	*si*	*sck1*	*sck2*	*q*	*qn*
0	↑	x	0	x	0	1
1	↑	x	0	x	1	0
x	0	0	⎍	⎍	0	1*
x	0	0	⎍	⎍	1	0*

** sck2 ⎍*
sck1 ⎍
sck2 must occur before sck1 in order to load si to outputs

Loading Characteristics:

Values stated in standard loads.

Version	*d*	*cp*	*sck1*	*sck2*	*si*
fd1s2	1.0	1.0	1.7	1.4	1.0
fd1s2p	1.0	1.0	1.7	1.4	1.0

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fd1s2	11	cp_to_q	tpLH	1.05	1.13	1.30	1.47	1.65
			tpHL	1.10	1.15	1.24	1.32	1.41
		cp_to_qn	tpLH	1.25	1.33	1.49	1.66	1.84
			tpHL	1.20	1.26	1.35	1.43	1.52
		sck1_to_q	tpLH	0.98	1.06	1.22	1.40	1.58
			tpHL	1.03	1.08	1.17	1.25	1.33
		sck1_to_qn	tpLH	1.17	1.25	1.41	1.58	1.77
			tpHL	1.13	1.18	1.28	1.36	1.44
		sck2_to_q	tpLH	1.07	1.15	1.31	1.48	1.66
			tpHL	1.12	1.17	1.25	1.34	1.42
		sck2_to_qn	tpLH	1.26	1.34	1.50	1.67	1.85
			tpHL	1.22	1.27	1.36	1.45	1.53
fd1s2p	12	cp_to_q	tpLH	1.04	1.08	1.16	1.24	1.32
			tpHL	1.10	1.14	1.19	1.24	1.29
		cp_to_qn	tpLH	1.29	1.33	1.41	1.49	1.57
			tpHL	1.25	1.28	1.34	1.39	1.44
		sck1_to_q	tpLH	0.97	1.01	1.09	1.17	1.25
			tpHL	1.03	1.07	1.12	1.17	1.22
		sck1_to_qn	tpLH	1.22	1.26	1.34	1.42	1.50
			tpHL	1.18	1.21	1.27	1.32	1.37
		sck2_to_q	tpLH	1.06	1.10	1.18	1.26	1.34
			tpHL	1.12	1.15	1.21	1.26	1.30
		sck2_to_qn	tpLH	1.31	1.35	1.43	1.51	1.59
			tpHL	1.27	1.30	1.36	1.41	1.46

Timing Constraints:

Version	*Parameters*	*Value*	*Version*	*Parameters*	*Value*
fd1s2	d_setup	0.30	fd1s2p	d_setup	0.31
	d_hold	0.09		d_hold	0.09
	cp_pw1	0.47		cp_pw1	0.47
	cp_pw0	0.39		cp_pw0	0.40
	sck2_pw	1.42		sck2_pw	1.42
	si_setup	1.98		si_setup	1.98
	si_hold	-0.18		si_hold	-0.18

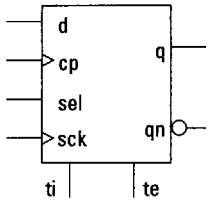
fd1ss
D Flip-Flop with Scan, Scan Clock, Scan Select

Name: fd1ss

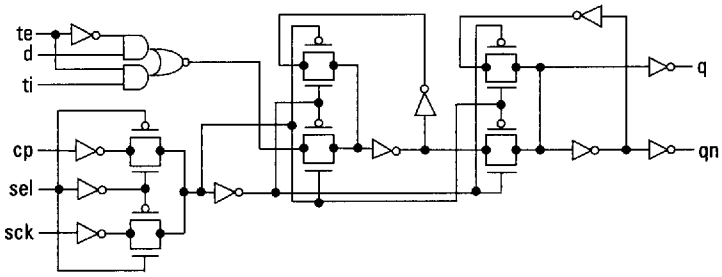
Description: D Flip-Flop with Scan, Scan Clock, Scan Select

Coding Syntax: u(q,qn)=fd1ss*(d,sel,cp,sck,ti,te)

Logic Symbol:



Schematics:



Truth Table:

d	*ti*	*te*	*cp*	*sck*	*sel*	*q*	*qn*
0	x	0	↑	x	0	0	1
1	x	0	↑	x	0	1	0
x	0	1	↑	x	0	0	1
x	1	1	↑	x	0	1	0
0	x	0	x	↑	1	0	1
1	x	0	x	↑	1	0	1
x	0	1	x	↑	1	0	1
x	1	1	x	↑	1	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*d*	*sel*	*cp*	*sck*	*ti*	*te*
fd1ss	1.0	1.6	1.0	1.0	0.9	1.9

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fd1ss	11	cp_to_qn	tpLH	1.25	1.33	1.49	1.66	1.85
			tpHL	1.19	1.24	1.32	1.40	1.48
		cp_to_q	tpLH	1.11	1.19	1.36	1.53	1.71
			tpHL	1.14	1.19	1.28	1.36	1.45
		sck_to_qn	tpLH	1.27	1.35	1.52	1.69	1.87
			tpHL	1.22	1.26	1.35	1.43	1.51
		sck_to_q	tpLH	1.14	1.22	1.39	1.56	1.74
			tpHL	1.16	1.22	1.31	1.39	1.47

Timing Constraints:

Version	*Parameters*	*Value*
fd1ss	d_setup	0.35
	d_hold	0.10
	ti_setup	0.43
	ti_hold	0.02
	te_setup	0.43
	te_hold	0.02
	sck_pw0	0.45
	sck_pw1	0.47
	sel_pw0	0.45
	sel_pw1	0.47
	cp_pw0	0.45
	cp_pw1	0.47

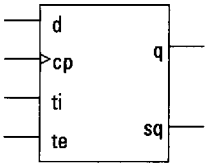
fd1sso
D Flip-Flop with Scan, Scan Out

Name: fd1sso

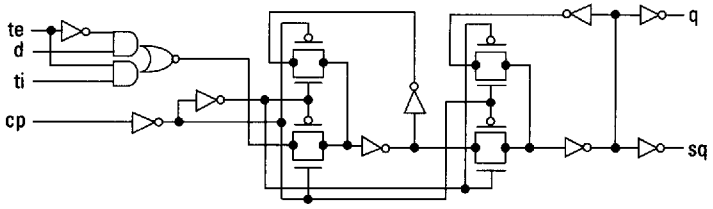
Description: D Flip-Flop with Scan, Scan Out

Coding Syntax: u(q,sq)=fd1sso(d,cp,ti,te)

Logic Symbol:



Schematics:



Truth Table:

d	*cp*	*ti*	*te*	*q*	*sq*
0	!	x	0	0	0
1	!	x	0	1	1
x	!	0	1	0	0
x	!	1	1	1	1
0	!	0	x	0	0
0	!	0	x	0	0
x	0	x	x	q	sq

! = positive trigger
x = don't care

Loading Characteristics:

Values stated in standard loads.

Version	*d*	*cp*	*ti*	*te*
fd1sso	1.0	1.0	1.0	2.0

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fd1sso	9	cp_to_q	tpLH	0.99	1.07	1.23	1.40	1.58
			tpHL	1.03	1.08	1.18	1.26	1.34
		cp_to_sq	tpLH	0.99	1.07	1.23	1.40	1.58
			tpHL	1.03	1.08	1.18	1.26	1.34

Timing Constraints:

Version	*Parameters*	*Value*
fd1sso	d_setup	0.54
	d_hold	0.11
	ti_setup	0.56
	ti_hold	0.07
	te_setup	0.56
	te_hold	0.07
	cp_pw0	0.42
	cp_pw1	0.47

fd1ss1

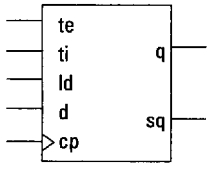
D Flip-Flop with Sychronous Load, Scan, Scan Out

Name: fd1ss1

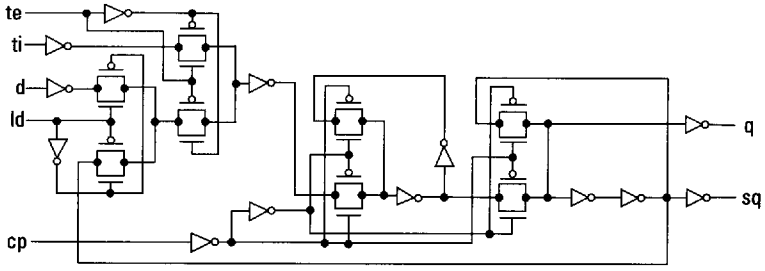
Description: D Flip-Flop with Sychronous Load, Scan, Scan Out

Coding Syntax: u(q,sq)=fd1ssl(d,cp,ld,ti,te)

Logic Symbol:



Schematics:



Truth Table:

d	*cp*	*ld*	*ti*	*te*	*q*	*sq*
0	!	1	x	0	0	0
1	!	1	x	0	1	1
x	!	x	0	1	0	0
x	!	x	1	1	1	1
x	!	0	x	0	q	q
x	0	x	x	x	q	q

! = positive trigger
x = don't care

Loading Characteristics:

Values stated in standard loads.

Version	*d*	*cp*	*ld*	*ti*	*te*
fd1ssl	1.0	1.0	1.9	1.0	1.9

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fd1ssl	11	cp_to_q	tpLH	0.91	1.00	1.16	1.34	1.52
			tpHL	0.87	0.93	1.04	1.13	1.22
		cp_to_sq	tpLH	1.15	1.23	1.39	1.56	1.74
			tpHL	1.12	1.17	1.26	1.34	1.42

Timing Constraints:

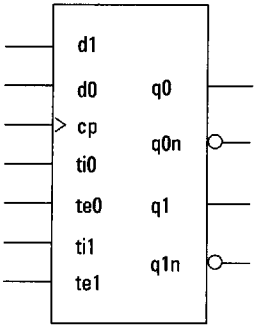
Version	*Parameters*	*Value*
fd1ssl	d_setup	0.66
	d_hold	-0.20
	ti_setup	0.46
	ti_hold	-0.00
	te_setup	0.31
	te_hold	0.11
	ld_setup	0.65
	ld_hold	-0.23
	cp_pw0	0.42
	cp_pw1	0.47

fd1sx2
2-Bit Buffered D Flip-Flop with Scan

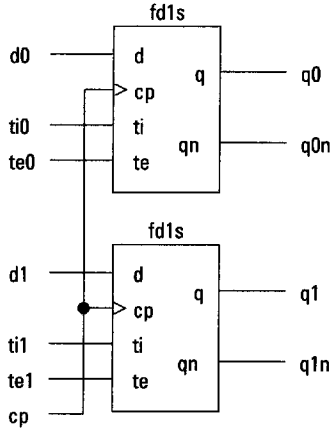
Name: fd1sx2 Description: 2-Bit Buffered D Flip-Flop with Scan

Coding Syntax: u(q0,q0n,q1,q1n)=fd1sx2(d0,d1,cp,ti0,te0,ti1,te1)

Logic Symbol:



Schematics:



Truth Table:

te0	*te1*	*cp*	*q0*	*q0n*	*q1*	*q1n*
0	0	↑	d0	$\overline{d0}$	d1	$\overline{d1}$
0	1	↑	d0	$\overline{d0}$	ti1	$\overline{ti1}$
1	0	↑	ti0	$\overline{ti0}$	d1	$\overline{d1}$
1	1	↑	ti0	$\overline{ti0}$	ti1	$\overline{ti1}$

Loading Characteristics:

Values stated in standard loads.

Version	*d0*	*d1*	*cp*	*ti0*	*te0*	*ti1*	*te1*
fd1sx2	0.5	0.5	1.0	0.5	1.0	0.5	1.0

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fd1sx2	17	cp_to_q0	tpLH	1.13	1.30	1.65	2.01	2.35
			tpHL	1.13	1.21	1.38	1.55	1.72
		cp_to_q0n	tpLH	1.36	1.52	1.88	2.24	2.58
			tpHL	1.27	1.36	1.53	1.70	1.88
		cp_to_q1	tpLH	1.13	1.30	1.65	2.01	2.35
			tpHL	1.13	1.21	1.38	1.55	1.72
		cp_to_q1n	tpLH	1.36	1.52	1.88	2.24	2.58
			tpHL	1.27	1.36	1.53	1.70	1.88

Timing Constraints:

Version	*Parameters*	*Value*
fd1sx2	d0_setup	0.85
	d0_hold	-0.24
	d1_setup	0.85
	d1_hold	-0.24
	ti0_setup	0.85
	ti0_hold	-0.24
	ti1_setup	0.85
	ti1_hold	-0.24
	te0_setup	0.95
	te0_hold	-0.35
	te1_setup	0.95
	te1_hold	-0.35
	cp_pw0	0.45
	cp_pw1	0.47

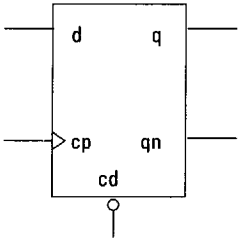
fd2
D Flip-Flop with Clear

Name: fd2

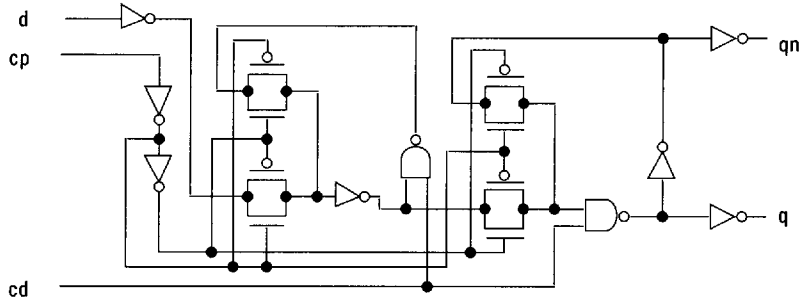
Description: D Flip-Flop with Clear

Coding Syntax: u(q,qn)=fd2*(d,cp,cd)

Logic Symbol:



Schematics:



Truth Table:

d	*cp*	*cd*	*q*	*qn*
0	↑	1	0	1
1	↑	1	1	0
x	x	0	0	1

Loading Characteristics:

Values stated in standard loads.

Version	*d*	*cp*	*cd*
fd2	1.0	1.0	1.8
fd2p	1.0	1.0	1.8

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fd2	8	cp_to_q	tpLH	1.03	1.11	1.28	1.45	1.63
			tpHL	1.04	1.10	1.20	1.28	1.36
		cp_to_qn	tpLH	1.30	1.38	1.54	1.71	1.89
			tpHL	1.14	1.19	1.27	1.35	1.44
		cd_to_qn	tpLH	0.92	1.00	1.16	1.33	1.51
			tpHL	0.92	1.00	1.16	1.33	1.51
		cd_to_q	tpLH	0.66	0.72	0.82	0.90	0.98
			tpHL	0.66	0.72	0.82	0.90	0.98

AC Characteristics: (Cont.)

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fd2p	9	cp_to_q	tpLH	1.02	1.07	1.15	1.24	1.32
			tpHL	1.00	1.03	1.09	1.15	1.20
		cp_to_qn	tpLH	1.29	1.34	1.42	1.50	1.58
			tpHL	1.20	1.23	1.29	1.33	1.38
		cd_to_qn	tpLH	0.99	1.04	1.13	1.21	1.29
			tpHL	0.99	1.04	1.13	1.21	1.29
		cd_to_q	tpLH	0.70	0.74	0.80	0.85	0.90
			tpHL	0.70	0.74	0.80	0.85	0.90

Timing Constraints:

Version	*Parameters*	*Value*	*Version*	*Parameters*	*Value*
fd2	d_setup	0.31	fd2p	d_setup	0.63
	d_hold	0.08		d_hold	0.08
	cp_pw0	0.40		cp_pw0	0.70
	cp_pw1	0.51		cp_pw1	0.51
	cd_rcvry	-0.53		cd_rcvry	-0.50
	cd_hold	0.80		cd_hold	0.80

fd2ess

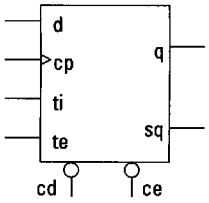
D Flip-Flop with Clear, Clear Enable, Scan, Scan Out

Name: fd2ess

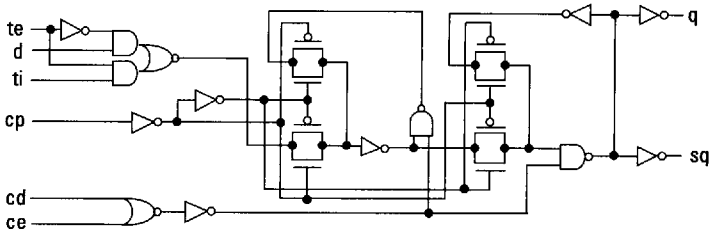
Description: D Flip-Flop with Clear, Clear Enable, Scan, Scan Out

Coding Syntax: u(q,sq)=fd2ess(d,cp,cd,ti,te,ce)

Logic Symbol:



Schematics:



Truth Table:

d	*cp*	*cd*	*ti*	*te*	*ce*	*q*	*sq*
x	x	0	x	x	0	0	0
d	!	0	x	0	1	d	d
d	!	1	x	0	1	d	d
d	!	1	x	0	0	d	d
x	!	0	ti	1	1	ti	ti
x	!	1	ti	1	1	ti	ti
x	!	1	ti	1	0	ti	ti
x	0	0	x	x	1	q	sq
x	0	1	x	x	1	q	sq
x	0	1	x	x	0	q	sq
0	!	0	0	x	1	0	0
0	!	1	0	x	1	0	0
0	!	1	0	x	0	0	0

! = positive trigger
x = don't care

Loading Characteristics:

Values stated in standard loads.

Version	*d*	*cp*	*cd*	*ti*	*te*	*ce*
fd2ess	1.0	1.0	1.0	1.0	2.0	0.9

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fd2ess	11	cp_to_sq	tpLH	1.08	1.17	1.34	1.51	1.69
			tpHL	1.05	1.10	1.20	1.28	1.36
		cp_to_q	tpLH	1.08	1.17	1.34	1.51	1.69
			tpHL	1.05	1.10	1.20	1.28	1.36
		cd_to_sq	tpLH	0.94	0.99	1.09	1.17	1.25
			tpHL	0.94	0.99	1.09	1.17	1.25
		cd_to_q	tpLH	0.94	0.99	1.09	1.17	1.25
			tpHL	0.94	0.99	1.09	1.17	1.25
		ce_to_sq	tpLH	0.94	0.99	1.09	1.17	1.25
			tpHL	0.94	0.99	1.09	1.17	1.25
		ce_to_q	tpLH	0.94	0.99	1.09	1.17	1.25
			tpHL	0.94	0.99	1.09	1.17	1.25

Timing Constraints:

Version	*Parameters*	*Value*
fd2ess	d_setup	0.55
	d_hold	0.01
	ti_setup	0.57
	ti_hold	0.00
	te_setup	0.57
	te_hold	0.00
	cp_pw0	0.57
	cp_pw1	0.51
	cd_rcvry	-0.26
	cd_hold	0.31
	ce_rcvry	-0.26
	ce_hold	0.31

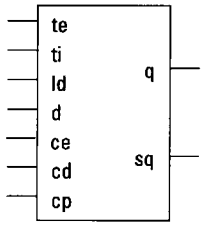
D Flip-Flop with Clear, Clear Enable, Synchronous Load, Scan, Scan Out

Name: fd2essl

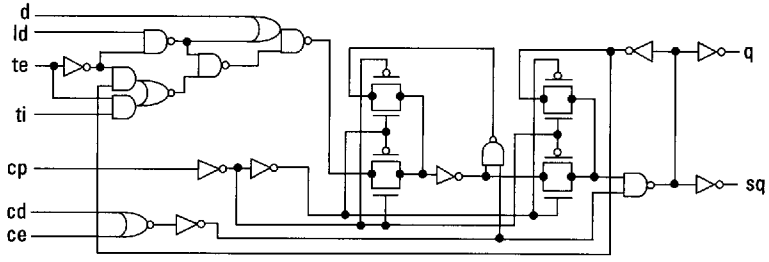
Description: D Flip-Flop with Clear, Clear Enable, Synchronous Load, Scan, Scan Out

Coding Syntax: u(q,sq)=fd2essl(d,ld,cp,cd,ti,te,ce)

Logic Symbol:



Schematics:



Truth Table:

d	*ld*	*cp*	*cd*	*tu*	*te*	*ce*	*q*	*sq*
x	x	x	0	x	x	0	0	0
x	x	!	1	0	1	x	0	0
x	x	!	1	1	1	x	1	1
0	1	!	1	x	0	x	0	0
1	1	!	1	x	0	x	1	1
x	0	x	1	x	0	x	q	q
x	x	!	x	0	1	1	0	0
x	x	!	x	1	1	1	1	1
0	1	!	x	x	0	1	0	0
1	1	!	x	x	0	1	1	1
x	0	x	x	x	0	1	q	q

! = positive trigger
x = don't care

Loading Characteristics:

Values stated in standard loads.

Version	*d*	*ld*	*cp*	*cd*	*ti*	*te*	*ce*
fd2essl	0.9	1.0	1.0	0.9	1.0	1.8	1.0

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fd2essl	15	cp_to_q	tpLH	1.08	1.16	1.32	1.50	1.69
			tpHL	1.17	1.20	1.26	1.33	1.40
		cp_to_sq	tpLH	1.08	1.16	1.32	1.50	1.69
			tpHL	1.17	1.20	1.26	1.33	1.40
		cd_to_q	tpLH	0.99	1.02	1.08	1.15	1.22
			tpHL	0.99	1.02	1.08	1.15	1.22
		cd_to_sq	tpLH	0.99	1.02	1.08	1.15	1.22
			tpHL	0.99	1.02	1.08	1.15	1.22
		ce_to_q	tpLH	0.99	1.02	1.08	1.15	1.22
			tpHL	0.99	1.02	1.08	1.15	1.22
		ce_to_sq	tpLH	0.99	1.02	1.08	1.15	1.22
			tpHL	0.99	1.02	1.08	1.15	1.22

Timing Constraints:

Version	*Parameters*	*Value*
fd2essl	d_setup	0.57
	d_hold	0.10
	ti_setup	0.82
	ti_hold	-0.15
	te_setup	0.82
	te_hold	-0.15
	ld_setup	0.99
	ld_hold	-0.09
	cp_pw0	0.67
	cp_pw1	0.51
	cd_rcvry	-0.33
	cd_hold	0.39
	ce_rcvry	-0.33
	ce_hold	0.39

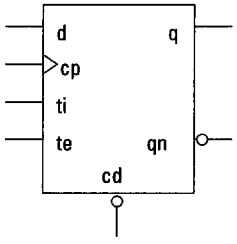
fd2s
D Flip-Flop with Clear, Scan

Name: fd2s

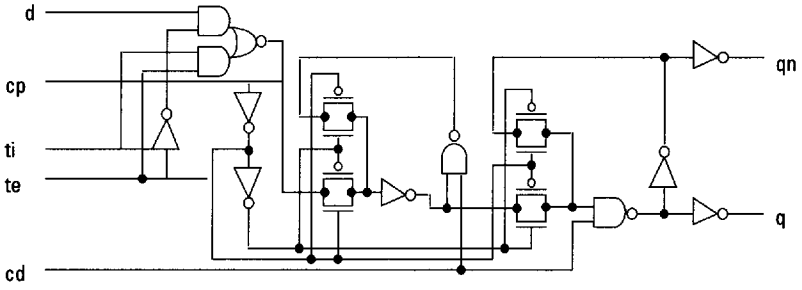
Description: D Flip-Flop with Clear, Scan

Coding Syntax: u (q,qn)=fd2s*(d,cp,cd,ti,te)

Logic Symbol:



Schematics:



Truth Table:

d	*ti*	*te*	*cp*	*cd*	*q*	*qn*
0	x	0	↑	1	0	1
1	x	0	↑	1	1	0
x	0	1	↑	1	0	1
x	1	1	↑	1	1	0
x	x	x	x	0	0	1

Loading Characteristics:

Values stated in standard loads.

Version	*d*	*cp*	*cd*	*ti*	*te*
fd2s	1.0	1.0	1.8	1.0	2.0
fd2sp	1.0	1.0	1.8	1.0	2.0

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fd2s	10	cp_to_qn	tpLH	1.24	1.32	1.48	1.65	1.83
			tpHL	1.14	1.19	1.27	1.35	1.44
		cp_to_q	tpLH	1.03	1.11	1.28	1.45	1.63
			tpHL	0.99	1.04	1.14	1.22	1.30
		cd_to_qn	tpLH	0.92	1.00	1.16	1.33	1.51
			tpHL	0.92	1.00	1.16	1.33	1.51
		cd_to_q	tpLH	0.67	0.72	0.82	0.90	0.98
			tpHL	0.67	0.72	0.82	0.90	0.98
fd2sp	11	cp_to_qn	tpLH	1.28	1.33	1.41	1.49	1.57
			tpHL	1.20	1.23	1.29	1.33	1.38
		cp_to_q	tpLH	1.03	1.11	1.28	1.45	1.63
			tpHL	0.99	1.04	1.13	1.22	1.30
		cd_to_qn	tpLH	0.99	1.04	1.12	1.21	1.29
			tpHL	0.99	1.04	1.12	1.21	1.29
		cd_to_q	tpLH	0.71	0.76	0.85	0.93	1.01
			tpHL	0.71	0.76	0.85	0.93	1.01

Timing Constraints:

Version	*Parameters*	*Value*	*Version*	*Parameters*	*Value*
fd2s	d_setup	0.57	fd2sp	d_setup	0.57
	d_hold	0.00		d_hold	0.00
	ti_setup	0.57		ti_setup	0.57
	ti_hold	0.00		ti_hold	0.00
	te_setup	0.57		te_setup	0.57
	te_hold	0.00		te_hold	0.00
	cp_pw0	0.57		cp_pw0	0.57
	cp_pw1	0.51		cp_pw1	0.51
	cd_rcvry	-0.53		cd_rcvry	-0.50
	cd_hold	0.80		cd_hold	0.80

fd2sl

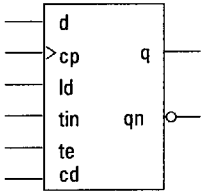
D Flip-Flop with Scan, Synchronous Load, and Clear

Name: fd2sl

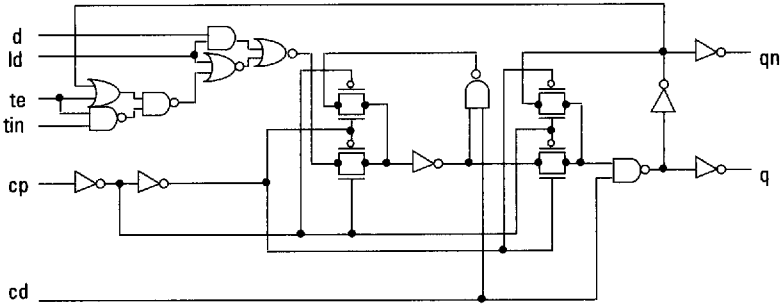
Description: D Flip-Flop with Scan, Synchronous Load, and Clear

Coding Syntax: u(q,qn)=fd2sl*(d,cp,cd,ti,te,ld)

Logic Symbol:



Schematics:



Truth Table:

cp	*cd*	*ld*	*te*	*q*	*qn*
x	0	x	x	0	1
↑	1	1	x	d	$\bar{d}$
↑	1	0	0	q	qn
↑	1	0	1	$\overline{tin}$	tin

Loading Characteristics:

Values stated in standard loads.

Version	*d*	*ld*	*cp*	*cd*	*tin*	*te*
fd2sl	2.3	2.9	1.0	1.6	2.4	3.1
fd2slp	2.3	2.9	1.0	1.6	2.4	3.1

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fd2sl	14	cp_to_qn	tpLH	1.29	1.38	1.54	1.71	1.89
			tpHL	1.15	1.20	1.29	1.37	1.46
		cp_to_q	tpLH	1.02	1.10	1.27	1.44	1.62
			tpHL	1.03	1.08	1.17	1.26	1.34
		cd_to_qn	tpLH	0.98	1.06	1.23	1.39	1.58
			tpHL	0.98	1.06	1.23	1.39	1.58
		cd_to_q	tpLH	0.72	0.77	0.86	0.94	1.03
			tpHL	0.72	0.77	0.86	0.94	1.03
fd2slp	16	cp_to_qn	tpLH	1.33	1.38	1.46	1.54	1.63
			tpHL	1.19	1.23	1.29	1.34	1.38
		cp_to_q	tpLH	1.00	1.05	1.13	1.21	1.30
			tpHL	1.03	1.07	1.12	1.17	1.22
		cd_to_qn	tpLH	1.08	1.12	1.21	1.29	1.37
			tpHL	1.08	1.12	1.21	1.29	1.37
		cd_to_q	tpLH	0.78	0.82	0.87	0.92	0.96
			tpHL	0.78	0.82	0.87	0.92	0.96

Timing Constraints:

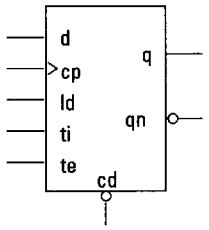
Version	*Parameters*	*Value*	*Version*	*Parameters*	*Value*
fd2sl	ld_setup	0.90	fd2slp	d_setup	0.63
	ld_hold	-0.48		d_hold	0.10
	d_setup	1.04		ld_setup	0.63
	d_hold	-0.62		ld_hold	0.10
	cp_pw0	0.42		te_hold	-0.22
	cp_pw1	0.51		te_setup	1.10
	te_setup	0.57		tin_setup	1.10
	te_hold	-0.13		tin_hold	-0.22
	ti_setup	0.52		cp_pw0	0.73
	ti_hold	-0.08		cp_pw1	0.90
	cd_rcvry	-0.53		cd_rcvry	-0.25
	cd_hold	0.80		cd_hold	0.98

fd2sl2
D Flip-Flop with Clear, Scan, and Load

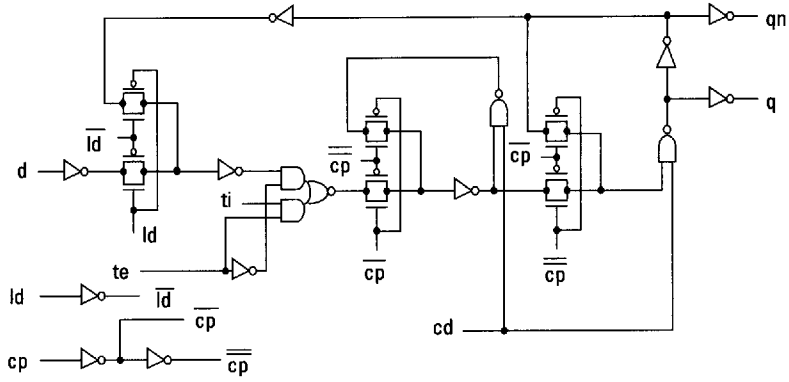
Name: fd2sl2 Description: D Flip-Flop with Clear, Scan, and Load

Coding Syntax: u(q,qn)=fd2sl2*(d,cp,cd,ti,te,ld)

Logic Symbol:



Schematics:



Truth Table:

cp	*cd*	*ld*	*te*	*q*	*qn*
x	0	x	x	0	1
↑	1	0	0	q	qn
↑	1	1	0	d	$\overline{d}$
↑	1	x	1	ti	$\overline{ti}$

Loading Characteristics:

Values stated in standard loads.

Version	*d*	*cp*	*cd*	*ti*	*te*	*ld*
fd2sl2	1.0	1.0	1.8	1.0	1.9	2.0
fd2sl2p	1.0	1.0	1.8	1.0	1.9	2.0

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fd2sl2	13	cp_to_qn	tpLH	1.33	1.41	1.57	1.74	1.92
			tpHL	1.18	1.24	1.33	1.41	1.50
		cp_to_q	tpLH	1.03	1.11	1.28	1.45	1.63
			tpHL	1.04	1.10	1.20	1.28	1.36
		cd_to_qn	tpLH	0.95	1.03	1.20	1.36	1.55
			tpHL	0.95	1.03	1.20	1.36	1.55
		cd_to_q	tpLH	0.66	0.72	0.82	0.90	0.99
			tpHL	0.66	0.72	0.82	0.90	0.99
fd2sl2p	14	cp_to_qn	tpLH	1.29	1.34	1.42	1.51	1.59
			tpHL	1.23	1.26	1.32	1.37	1.42
		cp_to_q	tpLH	1.00	1.05	1.14	1.22	1.30
			tpHL	0.98	1.02	1.07	1.12	1.17
		cd_to_qn	tpLH	1.03	1.07	1.16	1.24	1.32
			tpHL	1.03	1.07	1.16	1.24	1.32
		cd_to_q	tpLH	0.72	0.75	0.81	0.85	0.90
			tpHL	0.72	0.75	0.81	0.85	0.90

Timing Constraints:

Version	*Parameters*	*Value*	*Version*	*Parameters*	*Value*
fd2sl2	ld_setup	0.90	fd2sl2p	ld_setup	0.90
	ld_hold	-0.48		ld_hold	-0.48
	d_setup	1.04		d_setup	1.04
	d_hold	-0.62		d_hold	-0.62
	cp_pw0	0.42		cp_pw0	0.42
	cp_pw1	0.51		cp_pw1	0.51
	te_setup	0.57		te_setup	0.57
	te_hold	-0.13		te_hold	-0.13
	ti_setup	0.52		ti_setup	0.52
	ti_hold	-0.08		ti_hold	-0.08
	cd_rcvry	-0.53		cd_rcvry	-0.50
	cd_hold	0.80		cd_hold	0.80

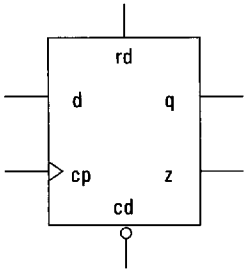
fd2ts
D Flip-Flop with Clear and 3-State Output

Name: fd2ts

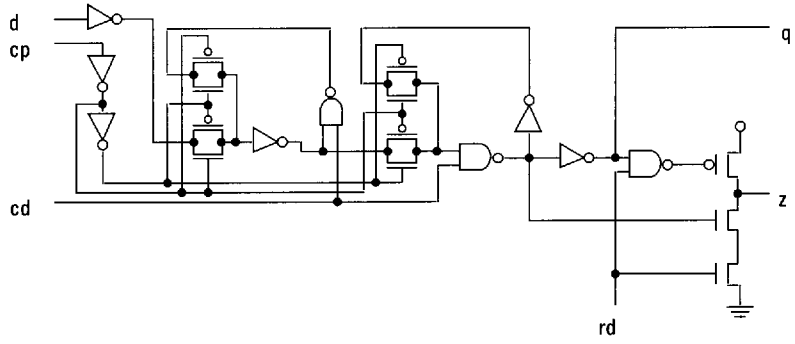
Description: D Flip-Flop with Clear and 3-State Output

Coding Syntax: u(z,q)=fd2ts*(d,cp,cd,rd)

Logic Symbol:



Schematics:



Truth Table:

d	*cp*	*cd*	*q*
0	↑	1	0
1	↑	1	1
x	x	0	0

rd	*q*	*z*
0	x	hi-z
1	0	0
1	1	1

Loading Characteristics:

Values stated in standard loads.

Version	*d*	*cp*	*cd*	*rd*
fd2ts	1.0	1.0	1.8	1.4
fd2tsp	1.0	1.0	1.8	1.8

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fd2ts	9	rd_to_z	tpLH	0.49	0.60	0.80	1.00	1.20
			tpHL	0.10	0.16	0.29	0.55	0.80
		cp_to_z	tpLH	1.54	1.66	1.85	2.05	2.23
			tpHL	1.22	1.27	1.42	1.71	1.96
		cp_to_q	tpLH	1.09	1.18	1.34	1.52	1.70
			tpHL	1.13	1.15	1.24	1.33	1.41
		cd_to_q	tpLH	0.75	0.77	0.86	0.94	1.02
			tpHL	0.75	0.77	0.86	0.94	1.02
		cd_to_z	tpLH	0.84	0.89	1.04	1.32	1.58
			tpHL	0.84	0.89	1.04	1.32	1.58
fd2tsp	11	rd_to_z	tpLH	0.44	0.52	0.64	0.74	0.84
			tpHL	0.08	0.11	0.18	0.24	0.30
		cp_to_z	tpLH	1.51	1.61	1.73	1.84	1.93
			tpHL	1.25	1.29	1.34	1.42	1.49
		cp_to_q	tpLH	1.08	1.13	1.22	1.30	1.39
			tpHL	1.18	1.20	1.21	1.25	1.30
		cd_to_q	tpLH	0.83	0.85	0.86	0.91	0.95
			tpHL	0.83	0.85	0.86	0.91	0.95
		cd_to_z	tpLH	0.91	0.94	0.99	1.07	1.15
			tpHL	0.91	0.94	0.99	1.07	1.15

Timing Constraints:

Version	*Parameters*	*Value*	*Version*	*Parameters*	*Value*
fd2ts	d_setup	0.31	fd2tsp	d_setup	0.31
	d_hold	0.08		d_hold	0.08
	cp_pw0	0.39		cp_pw0	0.39
	cp_pw1	0.51		cp_pw1	0.51
	cd_rcvry	-0.53		cd_rcvry	-0.42
	cd_hold	0.80		cd_hold	0.80

fd3

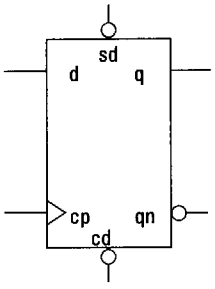
D Flip-Flop with Clear, Set

Name: fd3

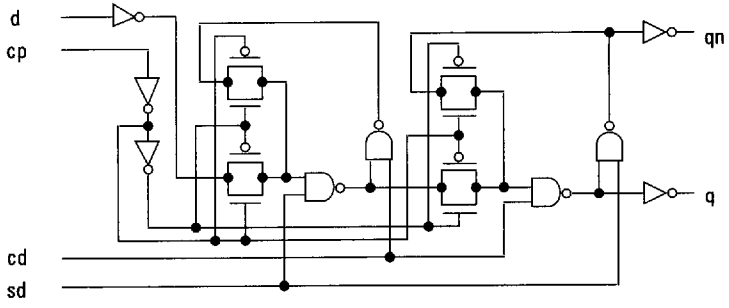
Description: D Flip-Flop with Clear, Set

Coding Syntax: u(q,qn)=fd3*(d,cp,cd,sd)

Logic Symbol:



Schematics:



Truth Table:

d	*cp*	*cd*	*sd*	*q*	*qn*
0	↑	1	1	0	1
1	↑	1	1	1	0
x	x	0	1	0	1
x	x	1	0	1	0
x	x	0	0	0	0

Loading Characteristics:

Values stated in standard loads.

Version	*d*	*cp*	*cd*	*sd*
fd3	1.0	1.0	1.8	1.8
fd3p	1.0	1.0	1.8	1.8

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fd3	9	cp_to_q	tpLH	1.01	1.10	1.26	1.43	1.61
			tpHL	1.02	1.07	1.16	1.24	1.32
		cp_to_qn	tpLH	1.32	1.41	1.58	1.75	1.93
			tpHL	1.12	1.17	1.26	1.34	1.42
		cd_to_q	tpLH	0.68	0.73	0.82	0.91	0.99
			tpHL	0.68	0.73	0.82	0.91	0.99
		cd_to_qn	tpLH	0.98	1.07	1.24	1.41	1.59
			tpHL	0.98	1.07	1.24	1.41	1.59
		sd_to_q	tpLH	1.12	1.21	1.37	1.54	1.72
			tpHL	1.12	1.21	1.37	1.54	1.72
		sd_to_qn	tpLH	0.86	0.91	1.00	1.08	1.16
			tpHL	0.86	0.91	1.00	1.08	1.16
fd3p	10	cp_to_q	tpLH	1.00	1.05	1.13	1.22	1.30
			tpHL	1.02	1.06	1.11	1.16	1.20
		cp_to_qn	tpLH	1.43	1.48	1.57	1.66	1.74
			tpHL	1.18	1.21	1.27	1.31	1.36
		cd_to_q	tpLH	0.72	0.76	0.81	0.86	0.90
			tpHL	0.72	0.76	0.81	0.86	0.90
		cd_to_qn	tpLH	1.13	1.18	1.27	1.36	1.44
			tpHL	1.13	1.18	1.27	1.36	1.44
		sd_to_q	tpLH	1.21	1.26	1.34	1.42	1.51
			tpHL	1.21	1.26	1.34	1.42	1.51
		sd_to_qn	tpLH	0.89	0.92	0.98	1.03	1.07
			tpHL	0.89	0.92	0.98	1.03	1.07

Timing Constraints:

Version	*Parameters*	*Value*	*Version*	*Parameters*	*Value*
fd3	d_setup	0.31	fd3p	d_setup	0.31
	d_hold	0.07		d_hold	0.07
	cd_rcvry	-0.42		cd_rcvry	-0.50
	cd_hold	0.86		cd_hold	0.86
	sd_rcvry	-0.20		sd_rcvry	-0.20
	sd_hold	0.18		sd_hold	0.23
	cp_pw0	0.38		cp_pw0	0.38
	cp_pw1	0.49		cp_pw1	0.49

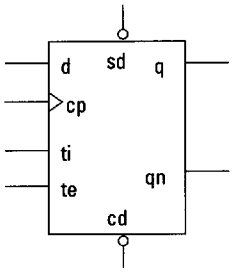
fd3s
D Flip-Flop with Clear, Set, and Scan

Name: fd3s

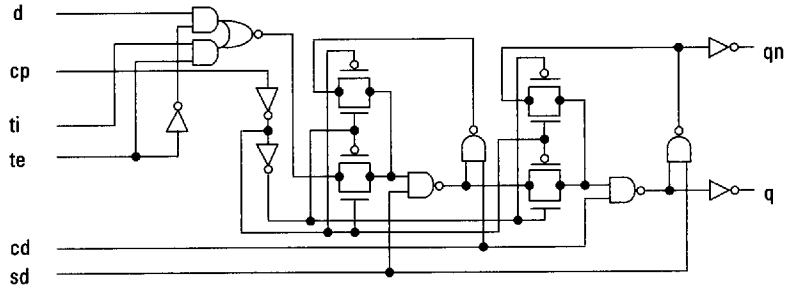
Description: D Flip-Flop with Clear, Set, and Scan

Coding Syntax: u(q,qn)=fd3s*(d,cp,cd,sd,ti,te)

Logic Symbol:



Schematics:



Truth Table:

d	*ti*	*te*	*cp*	*cd*	*sd*	*q*	*qn*
0	x	0	↑	1	1	0	1
1	x	0	↑	1	1	1	0
x	0	1	↑	1	1	0	1
x	1	1	↑	1	1	1	0
x	x	x	x	0	1	0	1
x	x	x	x	1	0	1	0
x	x	x	x	0	0	0	0

Loading Characteristics:

Values stated in standard loads.

Version	*d*	*cp*	*cd*	*sd*	*ti*	*te*
fd3s	1.8	1.0	1.8	1.8	1.0	2.0
fd3sp	1.0	1.0	1.8	1.8	1.0	2.0

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fd3s	11	cp_to_q	tpLH	1.01	1.10	1.26	1.43	1.61
			tpHL	1.02	1.07	1.16	1.24	1.32
		cp_to_qn	tpLH	1.38	1.46	1.63	1.80	1.98
			tpHL	1.12	1.17	1.26	1.34	1.42
		cd_to_qn	tpLH	1.04	1.13	1.30	1.47	1.65
			tpHL	1.04	1.13	1.30	1.47	1.65
		cd_to_q	tpLH	0.68	0.73	0.82	0.91	0.99
			tpHL	0.68	0.73	0.82	0.91	0.99
		sd_to_q	tpLH	1.12	1.20	1.37	1.54	1.72
			tpHL	0.89	0.98	1.14	1.31	1.49
		sd_to_qn	tpLH	0.86	0.91	1.00	1.08	1.16
			tpHL	0.86	0.91	1.00	1.08	1.16
fd3sp	12	cp_to_q	tpLH	1.01	1.05	1.13	1.22	1.30
			tpHL	1.02	1.06	1.11	1.16	1.20
		cp_to_qn	tpLH	1.42	1.48	1.57	1.66	1.74
			tpHL	1.18	1.21	1.27	1.31	1.36
		cd_to_qn	tpLH	1.13	1.18	1.27	1.36	1.44
			tpHL	1.13	1.18	1.27	1.36	1.44
		cd_to_q	tpLH	0.72	0.76	0.81	0.86	0.90
			tpHL	0.72	0.76	0.81	0.86	0.90
		sd_to_q	tpLH	1.21	1.26	1.34	1.42	1.51
			tpHL	1.01	1.06	1.14	1.22	1.31
		sd_to_qn	tpLH	0.89	0.92	0.98	1.03	1.07
			tpHL	0.89	0.92	0.98	1.03	1.07

fd3s

D Flip-Flop with Clear, Set, and Scan

Timing Constraints:

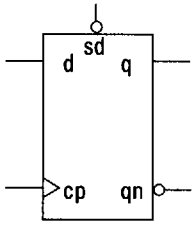
Version	*Parameters*	*Value*	*Version*	*Parameters*	*Value*
fd3s	d_setup	0.55	fd3sp	d_setup	0.55
	d_hold	0.00		d_hold	0.00
	ti_setup	0.55		ti_setup	0.55
	ti_hold	0.00		ti_hold	0.00
	te_setup	0.55		te_setup	0.55
	te_hold	0.00		te_hold	0.00
	cp_pw0	0.55		cp_pw0	0.55
	cp_pw1	0.53		cp_pw1	0.53
	cd_rcvry	-0.53		cd_rcvry	-0.50
	cd_hold	0.86		cd_hold	0.86
	sd_rcvry	-0.20		sd_rcvry	-0.20
	sd_hold	0.61		sd_hold	0.61

Name: fd4

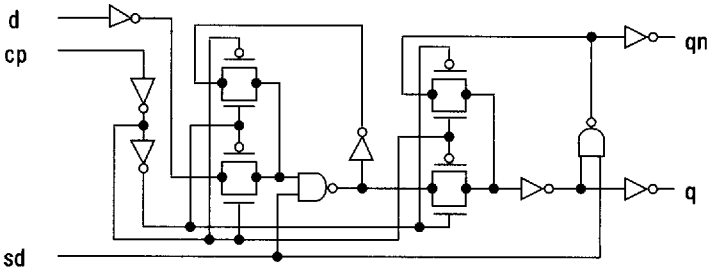
Description: D Flip-Flop with Set

Coding Syntax: u(q,qn)=fd4*(d,cp,sd)

Logic Symbol:



Schematics:



Truth Table:

d	*cp*	*sd*	*q*	*qn*
0	↑	1	0	1
1	↑	1	1	0
x	x	0	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*d*	*cp*	*sd*
fd4	1.0	1.0	1.7
fd4p	1.0	1.0	1.8

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fd4	8	cp_to_q	tpLH	0.96	1.04	1.20	1.37	1.55
			tpHL	1.03	1.08	1.17	1.25	1.33
		cp_to_qn	tpLH	1.24	1.33	1.49	1.66	1.84
			tpHL	1.07	1.11	1.20	1.29	1.37
		sd_to_q	tpLH	1.01	1.09	1.25	1.42	1.60
			tpHL	1.01	1.09	1.25	1.42	1.60
		sd_to_qn	tpLH	0.84	0.88	0.97	1.06	1.14
			tpHL	0.84	0.88	0.97	1.06	1.14

fd4

D Flip-Flop with Set

AC Characteristics: (Cont.)

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fd4p	9	cp_to_q	tpLH	0.94	0.98	1.06	1.14	1.23
			tpHL	1.03	1.07	1.12	1.17	1.21
		cp_to_qn	tpLH	1.29	1.34	1.42	1.50	1.59
			tpHL	1.10	1.14	1.19	1.24	1.28
		sd_to_q	tpLH	1.09	1.13	1.21	1.29	1.38
			tpHL	1.09	1.13	1.21	1.29	1.38
		sd_to_qn	tpLH	0.87	0.90	0.96	1.00	1.05
			tpHL	0.87	0.90	0.96	1.00	1.05

Timing Constraints:

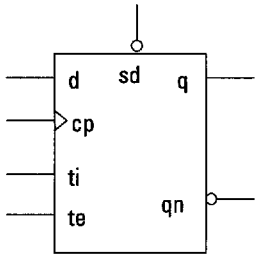
Version	*Parameters*	*Value*	*Version*	*Parameters*	*Value*
fd4	d_setup	0.31	fd4p	d_setup	0.31
	d_hold	0.07		d_hold	0.06
	cp_pw0	0.38		cp_pw0	0.37
	cp_pw1	0.49		cp_pw1	0.49
	sd_rcvry	-0.20		sd_rcvry	-0.20
	sd_hold	0.36		sd_hold	0.36

Name: fd4s

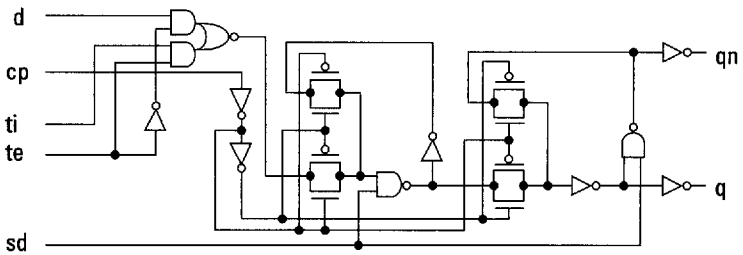
Description: D Flip-Flop with Set, Scan

Coding Syntax: u(q,qn)=fd4s*(d,cp,sd,ti,te)

Logic Symbol:



Schematics:



Truth Table:

d	*ti*	*te*	*cp*	*sd*	*q*	*qn*
0	x	0	↑	1	0	1
1	x	0	↑	1	1	0
x	0	1	↑	1	0	1
x	1	1	↑	1	1	0
x	x	x	x	0	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*d*	*cp*	*sd*	*ti*	*te*
fd4s	1.7	1.0	1.8	1.0	2.0
fd4sp	1.0	1.0	1.8	1.0	2.0

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fd4s	10	cp_to_qn	tpLH	1.24	1.33	1.49	1.66	1.84
			tpHL	1.07	1.11	1.20	1.29	1.37
		cp_to_q	tpLH	0.96	1.04	1.20	1.37	1.55
			tpHL	1.03	1.08	1.17	1.25	1.33
		sd_to_qn	tpLH	0.84	0.88	0.97	1.06	1.14
			tpHL	0.84	0.88	0.97	1.06	1.14
		sd_to_q	tpLH	1.01	1.09	1.25	1.42	1.60
			tpHL	1.01	1.09	1.25	1.42	1.60

fd4s

D Flip-Flop with Set, Scan

AC Characteristics: (Cont.)

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fd4sp	11	cp_to_qn	tpLH	1.29	1.34	1.42	1.50	1.59
			tpHL	1.10	1.13	1.19	1.24	1.28
		cp_to_q	tpLH	0.94	0.98	1.06	1.14	1.22
			tpHL	1.03	1.07	1.12	1.17	1.21
		sd_to_qn	tpLH	0.87	0.90	0.96	1.00	1.05
			tpHL	0.87	0.90	0.96	1.00	1.05
		sd_to_q	tpLH	1.09	1.13	1.21	1.29	1.38
			tpHL	1.09	1.13	1.21	1.29	1.38

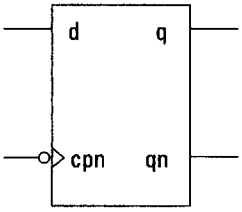
Timing Constraints:

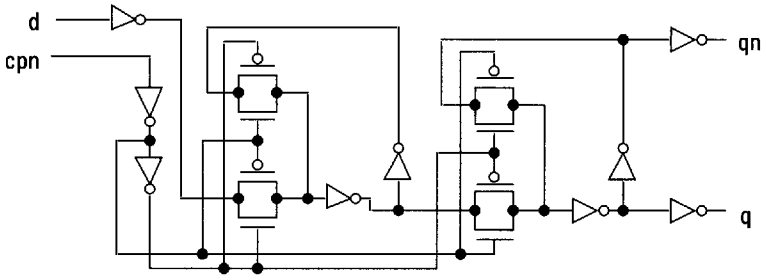
Version	*Parameters*	*Value*	*Version*	*Parameters*	*Value*
fd4s	d_setup	0.57	fd4sp	d_setup	0.57
	d_hold	0.00		d_hold	0.00
	ti_setup	0.57		ti_setup	0.57
	ti_hold	0.00		ti_hold	0.00
	te_setup	0.57		te_setup	0.57
	te_hold	0.00		te_hold	0.00
	cp_pw0	0.57		cp_pw0	0.57
	cp_pw1	0.49		cp_pw1	0.49
	sd_rcvry	-0.19		sd_rcvry	-0.19
	sd_hold	0.69		sd_hold	0.69

Name: fdn1 Description: D Flip-Flop

Coding Syntax: u(q,qn)=fdn1*(d,cpn)

Logic Symbol: Schematics:





Truth Table:

d	*cpn*	*q*	*qn*
0	↓	0	1
1	↓	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*d*	*cpn*
fdn1	1.0	1.0
fdn1p	1.0	1.0

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fdn1	7	cpn_to_q	tpLH	0.98	1.05	1.22	1.39	1.57
			tpHL	0.95	1.00	1.09	1.17	1.25
		cpn_to_qn	tpLH	1.09	1.17	1.33	1.51	1.69
			tpHL	1.08	1.13	1.22	1.30	1.38
fdn1p	8	cpn_to_q	tpLH	0.95	1.00	1.08	1.16	1.24
			tpHL	0.95	0.98	1.04	1.09	1.13
		cpn_to_qn	tpLH	1.13	1.17	1.25	1.33	1.41
			tpHL	1.12	1.15	1.21	1.25	1.30

fdn1
D Flip-Flop

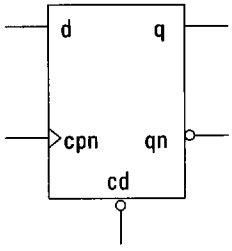
Timing Constraints:

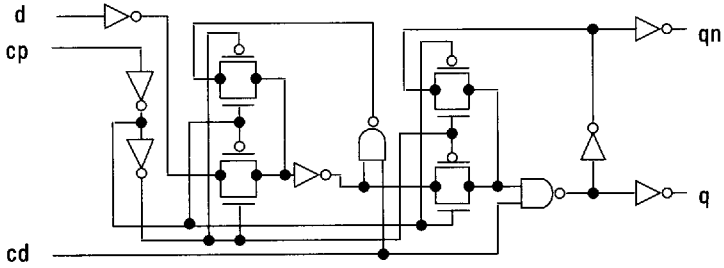
Version	*Parameters*	*Value*	*Version*	*Parameters*	*Value*
fdn1	d_setup	0.35	fdn1p	d_setup	0.35
	d_hold	0.10		d_hold	0.10
	cpn_pw1	0.47		cpn_pw1	0.47
	cpn_pw0	0.42		cpn_pw0	0.42

Name: fdn2 Description: D Flip-Flop with Clear

Coding Syntax: u(q,qn)=fdn2*(d,cpn,cd)

Logic Symbol: Schematics:





Truth Table:

d	*cpn*	*cd*	*q*	*qn*
0	↓	1	0	1
1	↓	1	1	0
x	x	0	0	1

Loading Characteristics:

Values stated in standard loads.

Version	*d*	*cpn*	*cd*
fdn2	1.0	1.0	1.8
fdn2p	1.0	1.0	1.8

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fdn2	8	cpn_to_q	tpLH	1.04	1.13	1.30	1.47	1.65
			tpHL	0.95	1.00	1.09	1.17	1.26
		cpn_to_qn	tpLH	1.19	1.27	1.44	1.60	1.78
			tpHL	1.15	1.20	1.29	1.37	1.45
		cd_to_qn	tpLH	0.91	1.00	1.16	1.33	1.51
			tpHL	0.91	1.00	1.16	1.33	1.51
		cd_to_q	tpLH	0.68	0.73	0.82	0.90	0.98
			tpHL	0.68	0.73	0.82	0.90	0.98

fdn2
D Flip-Flop with Clear

AC Characteristics: (Cont.)

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fdn2p	9	cpn_to_q	tpLH	1.03	1.08	1.16	1.25	1.33
			tpHL	0.95	0.99	1.04	1.09	1.13
		cpn_to_qn	tpLH	1.23	1.27	1.36	1.44	1.52
			tpHL	1.20	1.24	1.30	1.34	1.39
		cd_to_qn	tpLH	0.99	1.04	1.13	1.21	1.29
			tpHL	0.99	1.04	1.13	1.21	1.29
		cd_to_q	tpLH	0.72	0.75	0.81	0.85	0.90
			tpHL	0.72	0.75	0.81	0.85	0.90

Timing Constraints:

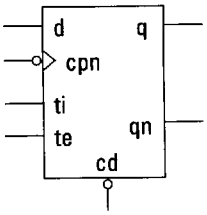
Version	*Parameters*	*Value*	*Version*	*Parameters*	*Value*
fdn2	d_setup	0.28	fdn2p	d_setup	0.28
	d_hold	0.00		d_hold	0.00
	cpn_pw0	0.28		cpn_pw0	0.28
	cpn_pw1	0.51		cpn_pw1	0.51
	cd_rcvry	-0.47		cd_rcvry	-0.34
	cd_hold	0.74		cd_hold	0.74

Name: fdn2s

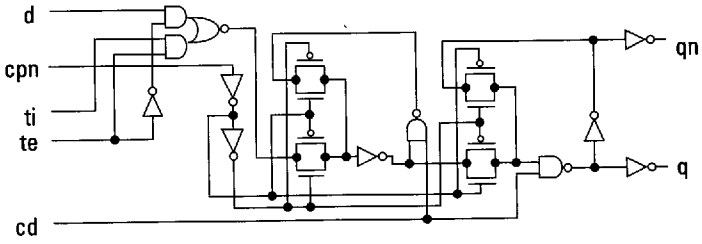
Description: D Flip-Flop with Clear, Scan

Coding Syntax: u(q,qn)=fdn2s*(d,cpn,cd,ti,te)

Logic Symbol:



Schematics:



Truth Table:

d	*ti*	*te*	*cpn*	*cd*	*q*	*qn*
0	x	0	↓	1	0	1
1	x	0	↓	1	1	0
x	0	1	↓	1	0	1
x	1	1	↓	1	1	0
x	x	x	x	0	0	1

Loading Characteristics:

Values stated in standard loads.

Version	*d*	*cpn*	*cd*	*ti*	*te*
fdn2s	0.9	1.0	1.8	1.0	1.9
fdn2sp	0.9	1.0	1.8	1.0	1.9

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fdn2s	10	cpn_to_qn	tpLH	1.19	1.27	1.43	1.60	1.78
			tpHL	1.15	1.20	1.29	1.37	1.45
		cpn_to_q	tpLH	1.04	1.13	1.30	1.47	1.65
			tpHL	0.95	1.00	1.09	1.17	1.26
		cd_to_qn	tpLH	0.91	0.99	1.16	1.33	1.51
			tpHL	0.91	0.99	1.16	1.33	1.51
		cd_to_q	tpLH	0.68	0.73	0.82	0.90	0.98
			tpHL	0.68	0.73	0.82	0.90	0.98

AC Characteristics: (Cont.)

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fdn2sp	11	cpn_to_qn	tpLH	1.23	1.27	1.36	1.44	1.52
			tpHL	1.20	1.24	1.30	1.34	1.39
		cpn_to_q	tpLH	1.03	1.08	1.16	1.24	1.33
			tpHL	0.95	0.99	1.04	1.09	1.13
		cd_to_qn	tpLH	0.99	1.04	1.13	1.21	1.29
			tpHL	0.99	1.04	1.13	1.21	1.29
		cd_to_q	tpLH	0.72	0.75	0.81	0.86	0.90
			tpHL	0.72	0.75	0.81	0.86	0.90

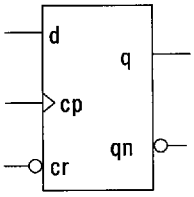
Timing Constraints:

Version	*Parameters*	*Value*	*Version*	*Parameters*	*Value*
fdn2s	d_setup	0.51	fdn2sp	d_setup	0.51
	d_hold	0.00		d_hold	0.00
	ti_setup	0.51		ti_setup	0.51
	ti_hold	0.00		ti_hold	0.00
	te_setup	0.51		te_setup	0.51
	te_hold	0.00		te_hold	0.00
	cpn_pw0	0.51		cpn_pw0	0.51
	cpn_pw1	0.51		cpn_pw1	0.51
	cd_rcvry	-0.47		cd_rcvry	-0.34
	cd_hold	0.74		cd_hold	0.74

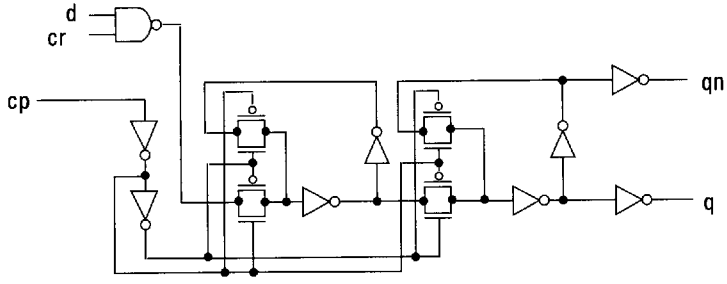
Name: fds2 Description: D Flip-Flop with Synchronous Clear

Coding Syntax: u(q,qn)=fds2*(d,cp,cr)

Logic Symbol:



Schematics:



Truth Table:

d	*cr*	*cp*	*q*	*qn*
x	0	↑	0	1
0	x	↑	0	1
1	1	↑	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*d*	*cp*	*cr*
fds2	1.0	1.0	1.0
fds2p	1.0	1.0	1.0

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fds2	7	cp_to_q	tpLH	0.96	1.04	1.21	1.37	1.56
			tpHL	0.99	1.04	1.13	1.22	1.29
		cp_to_qn	tpLH	1.14	1.22	1.38	1.55	1.73
			tpHL	1.07	1.12	1.20	1.28	1.36
fds2p	8	cp_to_q	tpLH	0.94	0.99	1.06	1.14	1.23
			tpHL	0.99	1.03	1.08	1.13	1.17
		cp_to_qn	tpLH	1.17	1.21	1.29	1.37	1.45
			tpHL	1.11	1.14	1.19	1.24	1.29

fds2
D Flip-Flop with Synchronous Clear

Timing Constraints:

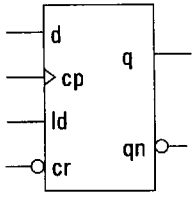
Version	*Parameters*	*Value*	*Version*	*Parameters*	*Value*
fds2	d_setup	0.43	fds2p	d_setup	0.48
	d_hold	0.29		d_hold	0.29
	cr_setup	0.43		cr_setup	0.48
	cr_hold	0.29		cr_hold	0.29
	cp_pw0	0.45		cp_pw0	0.53
	cp_pw1	0.47		cp_pw1	0.47

Name: fds2l

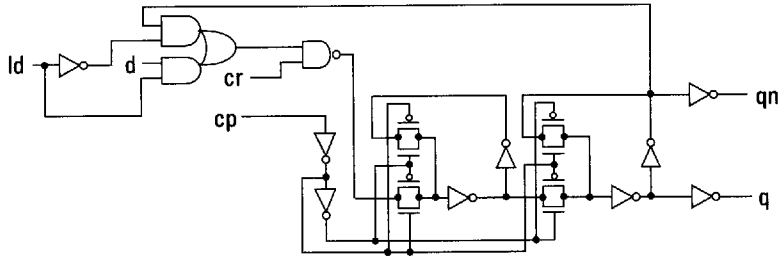
Description: D Flip-Flop with Synchronous Clear and Load

Coding Syntax: u(q,qn)=fds2l*(d,cp,cr,ld)

Logic Symbol:



Schematics:



Truth Table:

d	*ld*	*cr*	*cp*	*q*	*qn*
0	1	x	↑	0	1
1	1	1	↑	1	0
x	0	1	↑	q	qn
x	x	0	↑	0	1

Loading Characteristics:

Values stated in standard loads.

Version	*d*	*cp*	*cr*	*ld*
fds2l	1.0	1.0	1.0	1.0
fds2lp	1.0	1.0	1.0	1.0

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fds2l	10	cp_to_q	tpLH	0.95	1.03	1.19	1.36	1.55
			tpHL	0.98	1.03	1.12	1.20	1.28
		cp_to_qn	tpLH	1.16	1.24	1.40	1.57	1.75
			tpHL	1.08	1.13	1.22	1.30	1.38
fds2lp	11	cp_to_q	tpLH	0.93	0.97	1.05	1.13	1.21
			tpHL	0.98	1.01	1.07	1.12	1.16
		cp_to_qn	tpLH	1.19	1.23	1.31	1.39	1.48
			tpHL	1.12	1.15	1.21	1.26	1.30

fds2l

D Flip-Flop with Synchronous Clear and Load

Timing Constraints:

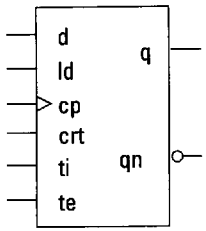
Version	*Parameters*	*Value*	*Version*	*Parameters*	*Value*
fds2l	d_setup	0.99	fds2lp	d_setup	0.95
	d_hold	-0.25		d_hold	-0.25
	cr_setup	0.92		cr_setup	0.88
	cr_hold	-0.18		cr_hold	-0.18
	ld_setup	0.99		ld_setup	0.95
	ld_hold	-0.25		ld_hold	-0.25
	cp_pw0	0.42		cp_pw0	0.42
	cp_pw1	0.47		cp_pw1	0.47

Name: fds2sl

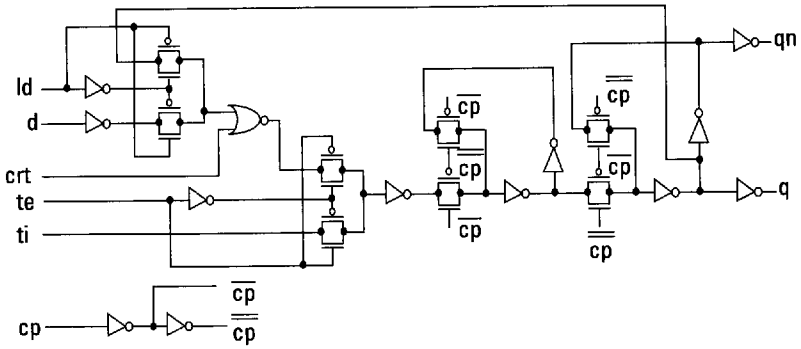
Description: D Flip-Flop with Enable, Synchronous Clear and Scan

Coding Syntax: u (q,qn) = fds2sl* (d,cp,crt,ld,ti,te)

Logic Symbol:



Schematics:



Truth Table:

d	*cp*	*crt*	*ld*	*ti*	*te*	*q*	*qn*
0	↑	0	1	x	0	0	1
1	↑	0	1	x	0	1	0
x	↑	0	0	0	1	0	1
x	↑	0	0	1	1	1	0
x	↑	1	x	x	0	0	1
x	↑	0	0	x	0	q	qn

Loading Characteristics:

Values stated in standard loads.

Version	*d*	*cp*	*crt*	*ld*	*ti*	*te*
fds2sl	1.0	1.0	1.0	1.5	3.2	2.0
fds2slp	1.0	1.0	1.0	1.5	3.2	2.0

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fds2sl	11	cp_to_qn	tpLH	1.18	1.25	1.43	1.61	1.81
			tpHL	1.17	1.20	1.26	1.33	1.41
		cp_to_q	tpLH	1.00	1.08	1.25	1.44	1.63
			tpHL	1.11	1.13	1.20	1.27	1.34

AC Characteristics: (Cont.)

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fds2slp	12	cp_to_qn	tpLH	1.23	1.26	1.33	1.42	1.51
			tpHL	1.23	1.25	1.28	1.31	1.34
		cp_to_q	tpLH	1.00	1.03	1.10	1.17	1.26
			tpHL	1.15	1.17	1.19	1.22	1.25

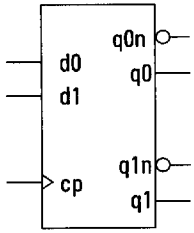
Timing Constraints:

Version	*Parameters*	*Value*	*Version*	*Parameters*	*Value*
fds2sl	d_setup	1.02	fds2slp	d_setup	1.02
	d_hold	-0.40		d_hold	-0.40
	crt_setup	0.64		crt_setup	0.64
	crt_hold	-0.16		crt_hold	-0.16
	ld_setup	0.77		ld_setup	0.77
	ld_hold	-0.16		ld_hold	-0.16
	ti_setup	0.49		ti_setup	0.49
	ti_hold	0.11		ti_hold	0.11
	te_setup	0.49		te_setup	0.49
	te_hold	0.11		te_hold	0.11
	cp_pw0	0.60		cp_pw0	0.60
	cp_pw1	0.47		cp_pw1	0.47

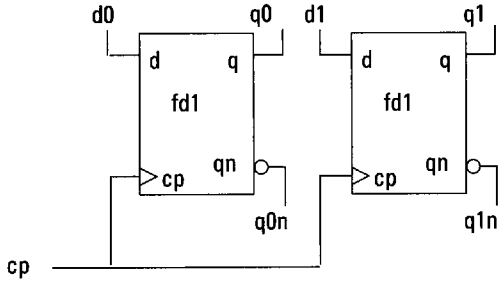
Name: fd1x2 Description: 2-Bit D Flip-Flop, Buffered

Coding Syntax: u(q0,q1,q0n,q1n)=fd1x2(d0,d1,cp)

Logic Symbol:



Schematics:



Truth Table:

d0	*d1*	*cp*	*q0*	*q0n*	*q1*	*q1n*
0	0	↑	0	1	0	1
0	1	↑	0	1	1	0
1	0	↑	1	0	0	1
1	1	↑	1	0	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*d0*	*d1*	*cp*
fd1x2	1.0	1.0	1.0

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fd1x2	12	cp_to_q0	tpLH	1.09	1.17	1.33	1.50	1.68
			tpHL	1.17	1.22	1.31	1.39	1.47
		cp_to_q0n	tpLH	1.31	1.39	1.55	1.72	1.91
			tpHL	1.19	1.24	1.33	1.41	1.49
		cp_to_q1	tpLH	1.09	1.17	1.33	1.50	1.68
			tpHL	1.17	1.22	1.31	1.39	1.47
		cp_to_q1n	tpLH	1.31	1.39	1.55	1.72	1.91
			tpHL	1.19	1.24	1.33	1.41	1.49

fd1x2

2-Bit D Flip-Flop, Buffered

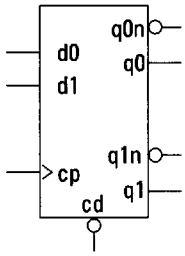
Timing Constraints:

Version	*Parameters*	*Value*
fd1x2	d0_setup	0.23
	d0_hold	0.24
	d1_setup	0.23
	d1_hold	0.24
	cp_pw0	0.47
	cp_pw1	0.47

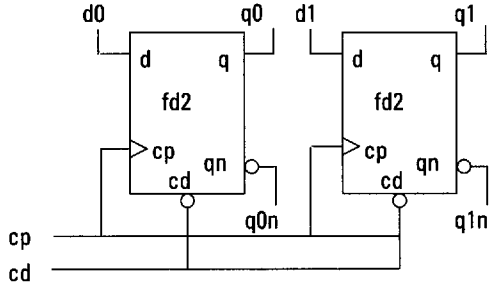
Name: fd2x2 Description: 2-Bit D Flip-Flop, CD, Buffered

Coding Syntax: u(q0,q1,q0n,q1n)=fd2x2(d0,d1,cp,cd)

Logic Symbol:



Schematics:



Truth Table:

d0	*d1*	*cp*	*cd*	*q0*	*q0n*	*q1*	*q1n*
0	0	↑	1	0	1	0	1
0	1	↑	1	0	1	1	0
1	0	↑	1	1	0	0	1
1	1	↑	1	1	0	1	0
x	x	x	0	0	1	0	1

Loading Characteristics:

Values stated in standard loads.

Version	*d0*	*d1*	*cp*	*cd*
fd2x2	1.0	1.0	1.0	3.6

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fd2x2	16	cp_to_q0	tpLH	1.16	1.25	1.41	1.59	1.77
			tpHL	1.23	1.29	1.39	1.47	1.55
		cp_to_q0n	tpLH	1.48	1.56	1.72	1.90	2.07
			tpHL	1.27	1.32	1.41	1.49	1.57
		cp_to_q1	tpLH	1.16	1.25	1.41	1.59	1.77
			tpHL	1.23	1.29	1.39	1.47	1.55
		cp_to_q1n	tpLH	1.48	1.56	1.72	1.90	2.07
			tpHL	1.27	1.32	1.41	1.49	1.57
		cd_to_q0n	tpLH	0.91	0.99	1.15	1.32	1.50
			tpHL	0.91	0.99	1.15	1.32	1.50
		cd_to_q0	tpLH	0.66	0.72	0.81	0.90	0.98
			tpHL	0.66	0.72	0.81	0.90	0.98
		cd_to_q1n	tpLH	0.91	0.99	1.15	1.32	1.50
			tpHL	0.91	0.99	1.15	1.32	1.50
		cd_to_q1	tpLH	0.66	0.72	0.81	0.90	0.98
			tpHL	0.66	0.72	0.81	0.90	0.98

Timing Constraints:

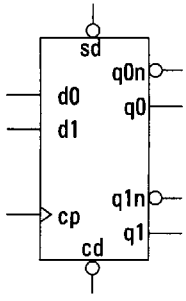
Version	*Parameters*	*Value*
fd2x2	d0_setup	0.23
	d0_hold	0.26
	d1_setup	0.23
	d1_hold	0.26
	cp_pw0	0.49
	cp_pw1	0.51
	cd_rcvry	-0.75
	cd_hold	1.00

Name: fd3x2

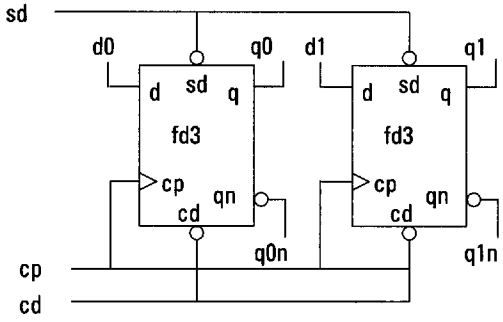
Description: 2-Bit D Flip-Flop, CD, SD, Buffered

Coding Syntax: u(q0,q1,q0n,q1n)=fd3x2(d0,d1,cp,cd,sd)

Logic Symbol:



Schematics:



Truth Table:

d0	*d1*	*cp*	*cd*	*sd*	*q0*	*q0n*	*q1*	*q1n*
0	0	↑	1	1	0	1	0	1
0	1	↑	1	1	0	1	1	0
1	0	↑	1	1	1	0	0	1
1	1	↑	1	1	1	0	1	0
x	x	x	0	1	0	1	0	1
x	x	x	1	0	1	0	1	0
x	x	x	0	0	0	0	0	0

Loading Characteristics:

Values stated in standard loads.

Version	*d0*	*d1*	*cp*	*cd*	*sd*
fd3x2	1.0	1.0	1.0	3.6	3.6

fd3x2

2-Bit D Flip-Flop, CD, SD, Buffered

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fd3x2	18	cp to any q	tpLH	1.21	1.29	1.45	1.62	1.81
			tpHL	1.20	1.25	1.34	1.43	1.51
		cd to any q	tpLH	0.68	0.73	0.82	0.90	0.99
			tpHL	0.68	0.73	0.82	0.90	0.99
		sd to any q	tpLH	1.12	1.20	1.36	1.53	1.72
			tpHL	1.12	1.20	1.36	1.53	1.72
		cp to any qn	tpLH	1.50	1.59	1.76	1.93	2.11
			tpHL	1.25	1.30	1.39	1.47	1.56
		cd to any qn	tpLH	0.98	1.07	1.24	1.41	1.59
			tpHL	0.98	1.07	1.24	1.41	1.59
		sd to any qn	tpLH	0.86	0.91	0.99	1.08	1.16
			tpHL	0.86	0.91	0.99	1.08	1.16

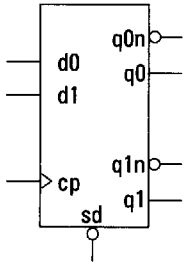
Timing Constraints:

Version	*Parameters*	*Value*
fd3x2	Any d setup	0.23
	Any d hold	0.25
	cp_pw0	0.47
	cp_pw1	0.49
	cd_rcvry	-0.70
	cd_hold	1.08
	sd_rcvry	-0.31
	sd_hold	0.37

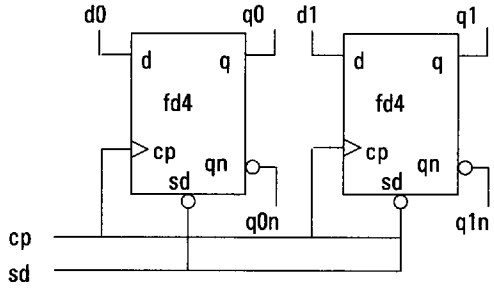
Name: fd4x2 Description: 2-Bit D Flip-Flop, SD, Buffered

Coding Syntax: u(q0,q1,q0n,q1n)=fd4x2(d0,d1,cp,sd)

Logic Symbol:



Schematics:



Truth Table:

d0	*d1*	*cp*	*cd*	*q0*	*q0n*	*q1*	*q1n*
0	0	↑	1	0	1	0	1
0	1	↑	1	0	1	1	0
1	0	↑	1	1	0	0	1
1	1	↑	1	1	0	1	0
x	x	x	0	0	1	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*d0*	*d1*	*cp*	*sd*
fd4x2	1.0	1.0	1.0	3.6

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fd4x2	16	Any cp to q	tpLH	1.09	1.17	1.33	1.50	1.68
			tpHL	1.21	1.26	1.35	1.44	1.52
		Any cp to qn	tpLH	1.43	1.51	1.68	1.85	2.03
			tpHL	1.20	1.25	1.33	1.42	1.50
		Any sd to q	tpLH	1.00	1.08	1.25	1.42	1.60
			tpHL	1.00	1.08	1.25	1.42	1.60
		Any sd to qn	tpLH	0.84	0.89	0.97	1.06	1.14
			tpHL	0.84	0.89	0.97	1.06	1.14

fd4x2

2-Bit D Flip-Flop, SD, Buffered

Timing Constraints:

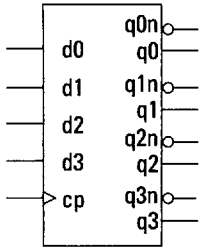
Version	*Parameters*	*Value*
fd4x2	Any d setup	0.22
	Any d hold	0.24
	cp_pw0	0.46
	cp_pw1	0.49
	sd_rcvry	-0.37
	sd_hold	0.42

Name: fd1x4

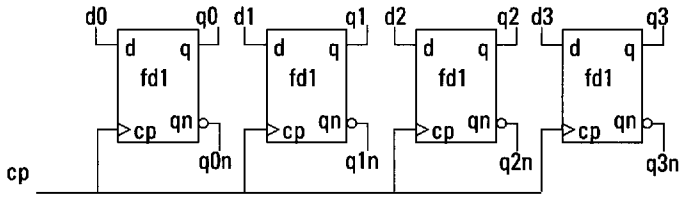
Description: 4-Bit D Flip-Flop, Buffered

Coding Syntax: u(q0,q1,q2,q3,q0n,q1n,q2n,q3n)=fd1x4(d0,d1,d2,d3,cp)

Logic Symbol:



Schematics:



Truth Table:

d0	*d1*	*d2*	*d3*	*cp*	*q0*	*q0n*	*q1*	*q1n*	*q2*	*q2n*	*q3*	*q3n*
0	0	0	0	↑	0	1	0	1	0	1	0	1
0	0	0	1	↑	0	1	0	1	0	1	1	0
0	0	1	0	↑	0	1	0	1	1	0	0	1
0	0	0	1	↑	0	1	0	1	1	0	1	0
0	1	0	0	↑	0	1	1	0	0	1	0	1
0	1	0	1	↑	0	1	1	0	0	1	1	0
0	1	1	0	↑	0	1	1	0	1	0	0	1
0	1	1	1	↑	0	1	1	0	1	0	1	0
1	0	0	0	↑	1	0	0	1	0	1	0	1
1	0	0	1	↑	1	0	0	1	0	1	1	0
1	0	1	0	↑	1	0	0	1	1	0	0	1
1	0	1	1	↑	1	0	0	1	1	0	1	0
1	1	0	0	↑	1	0	1	0	0	1	0	1
1	1	0	1	↑	1	0	1	0	0	1	1	0
1	1	1	0	↑	1	0	1	0	1	0	0	1
1	1	1	1	↑	1	0	1	0	1	0	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*d0*	*d1*	*d2*	*d3*	*cp*
fd1x4	1.0	1.0	1.0	1.0	1.9

fd1x4
4-Bit D Flip-Flop, Buffered

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fd1x4	24	cp to any q	tpLH	1.05	1.13	1.30	1.47	1.65
			tpHL	1.12	1.17	1.26	1.34	1.42
		cp to any qn	tpLH	1.26	1.34	1.51	1.67	1.86
			tpHL	1.16	1.21	1.29	1.38	1.46

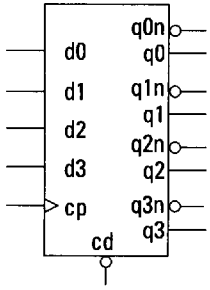
Timing Constraints:

Version	*Parameters*	*Value*
fd1x4	Any d setup	0.24
	Any d hold	0.22
	cp_pw0	0.46
	cp_pw1	0.47

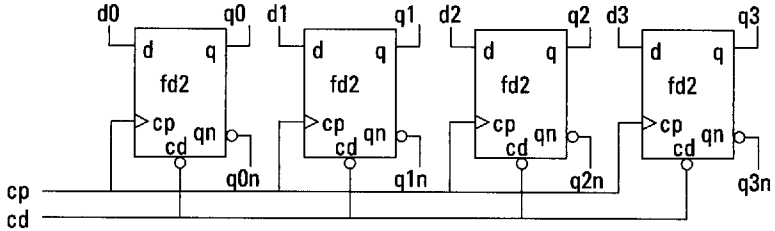
Name: fd2x4 Description: 4-Bit D Flip-Flop, CD, Buffered

Coding Syntax: u(q0,q1,q2,q3,q0n,q1n,q2n,q3n)=fd2x4(d0,d1,d2,d3,cp,cd)

Logic Symbol:



Schematics:



Truth Table:

d0	*d1*	*d2*	*d3*	*cp*	*cd*	*q0*	*q0n*	*q1*	*q1n*	*q2*	*q2n*	*q3*	*q3n*
0	0	0	0	↑	1	0	1	0	1	0	1	0	1
0	0	0	1	↑	1	0	1	0	1	0	1	1	0
0	0	1	0	↑	1	0	1	0	1	1	0	0	1
0	0	1	1	↑	1	0	1	0	1	1	0	1	0
0	1	0	0	↑	1	0	1	1	0	0	1	0	1
0	1	0	1	↑	1	0	1	1	0	0	1	1	0
0	1	1	0	↑	1	0	1	1	0	1	0	0	1
0	1	1	1	↑	1	0	1	1	0	1	0	1	0
1	0	0	0	↑	1	1	0	0	1	0	1	0	1
1	0	0	1	↑	1	1	0	0	1	0	1	1	0
1	0	1	0	↑	1	1	0	0	1	1	0	0	1
1	0	1	1	↑	1	1	0	0	1	1	0	1	0
1	1	0	0	↑	1	1	0	1	0	0	1	0	1
1	1	0	1	↑	1	1	0	1	0	0	1	1	0
1	1	1	0	↑	1	1	0	1	0	1	0	0	1
1	1	1	1	↑	1	1	0	1	0	1	0	1	0
x	x	x	x	x	0	0	1	0	1	0	1	0	1

Loading Characteristics:

Values stated in standard loads.

Version	*d0*	*d1*	*d2*	*d3*	*cp*	*cd*
fd2x4	1.0	1.0	1.0	1.0	1.9	7.3

fd2x4

4-Bit D Flip-Flop, CD, Buffered

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fd2x4	31	cp to any q	tpLH	1.13	1.22	1.38	1.55	1.74
			tpHL	1.18	1.24	1.34	1.42	1.50
		cp to any qn	tpLH	1.43	1.52	1.68	1.85	2.03
			tpHL	1.24	1.29	1.38	1.46	1.54
		cd to any qn	tpLH	0.91	0.99	1.15	1.33	1.50
			tpHL	0.91	0.99	1.15	1.33	1.50
		cd to any q	tpLH	0.66	0.72	0.82	0.90	0.98
			tpHL	0.66	0.72	0.82	0.90	0.98

Timing Constraints:

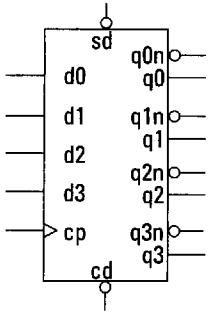
Version	*Parameters*	*Value*
fd2x4	Any d setup	0.24
	Any d hold	0.22
	cp_pw0	0.46
	cp_pw1	0.51
	cd_rcvry	-0.64
	cd_hold	0.97

Name: fd3x4

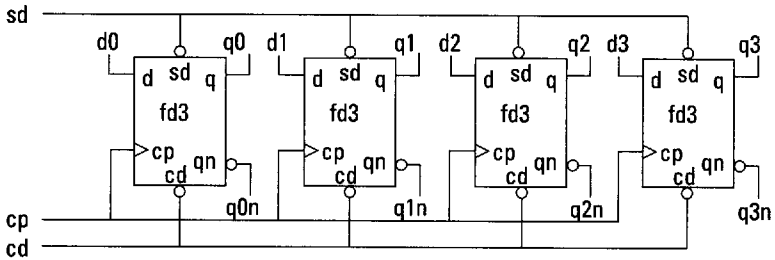
Description: 4-Bit D Flip-Flop, CD, SD, Buffered

Coding Syntax: u(q0,q1,q2,q3,q0n,q1n,q2n,q3n)=fd3x4(d0,d1,d2,d3,cp,cd,sd)

Logic Symbol:



Schematics:



Truth Table:

d0	*d1*	*d2*	*d3*	*cp*	*cd*	*sd*	*q0*	*q0n*	*q1*	*q1n*	*q2*	*q2n*	*q3*	*q3n*
0	0	0	0	↑	1	1	0	1	0	1	0	1	0	1
0	0	0	1	↑	1	1	0	1	0	1	0	1	1	0
0	0	1	0	↑	1	1	0	1	0	1	1	0	0	1
0	0	1	1	↑	1	1	0	1	0	1	1	0	1	0
0	1	0	0	↑	1	1	0	1	1	0	0	1	0	1
0	1	0	1	↑	1	1	0	1	1	0	0	1	1	0
0	1	1	0	↑	1	1	0	1	1	0	1	0	0	1
0	1	1	1	↑	1	1	0	1	1	0	1	0	1	0
1	0	0	0	↑	1	1	1	0	0	1	0	1	0	1
1	0	0	1	↑	1	1	1	0	0	1	0	1	1	0
1	0	1	0	↑	1	1	1	0	0	1	1	0	0	1
1	0	1	1	↑	1	1	1	0	0	1	1	0	1	0
1	1	0	0	↑	1	1	1	0	1	0	0	1	0	1
1	1	0	1	↑	1	1	1	0	1	0	0	1	1	0
1	1	1	0	↑	1	1	1	0	1	0	1	0	0	1
1	1	1	1	↑	1	1	1	0	1	0	1	0	1	0
x	x	x	x	x	0	1	0	1	0	1	0	1	0	1
x	x	x	x	x	1	0	1	0	1	0	1	0	1	0
x	x	x	x	x	0	0	0	0	0	0	0	0	0	0

fd3x4
4-Bit D Flip-Flop, CD, SD, Buffered

Loading Characteristics:

Values stated in standard loads.

Version	*d0*	*d1*	*d2*	*d3*	*cp*	*cd*	*sd*
fd3x4	1.0	1.0	1.0	1.0	1.9	7.2	7.2

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fd3x4	35	cp to any q	tpLH	1.18	1.26	1.42	1.59	1.77
			tpHL	1.15	1.20	1.29	1.38	1.46
		cd to any q	tpLH	0.68	0.73	0.82	0.91	0.99
			tpHL	0.68	0.73	0.82	0.91	0.99
		sd to any q	tpLH	1.12	1.20	1.36	1.53	1.71
			tpHL	1.12	1.20	1.36	1.53	1.71
		cp to any qn	tpLH	1.45	1.54	1.71	1.88	2.06
			tpHL	1.22	1.27	1.36	1.44	1.53
		cd to any qn	tpLH	0.98	1.07	1.24	1.41	1.59
			tpHL	0.98	1.07	1.24	1.41	1.59
		sd to any qn	tpLH	0.86	0.91	1.00	1.08	1.16
			tpHL	0.86	0.91	1.00	1.08	1.16

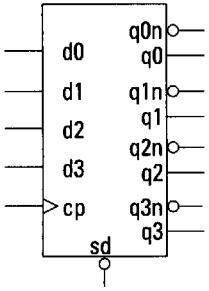
Timing Constraints:

Version	*Parameters*	*Value*
fd3x4	Any d setup	0.23
	Any d hold	0.21
	cp_pw1	0.49
	cp_pw0	0.44
	cd_hold	1.00
	cd_rcvry	-0.63
	sd_hold	0.37
	sd_rcvry	-0.31

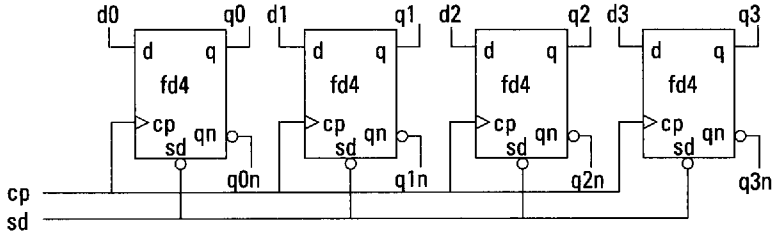
Name: fd4x4 Description: 4-Bit D Flip-Flop, SD, Buffered

Coding Syntax: u(q0,q1,q2,q3,q0n,q1n,q2n,q3n)=fd4x4(d0,d1,d2,d3,cp,sd)

Logic Symbol:



Schematics:



Truth Table:

d0	*d1*	*d2*	*d3*	*cp*	*sd*	*q0*	*q0n*	*q1*	*q1n*	*q2*	*q2n*	*q3*	*q3n*
0	0	0	0	↑	1	0	1	0	1	0	1	0	1
0	0	0	1	↑	1	0	1	0	1	0	1	1	0
0	0	1	0	↑	1	0	1	0	1	1	0	0	1
0	0	1	1	↑	1	0	1	0	1	1	0	1	0
0	1	0	0	↑	1	0	1	1	0	0	1	0	1
0	1	0	1	↑	1	0	1	1	0	0	1	1	0
0	1	1	0	↑	1	0	1	1	0	1	0	0	1
0	1	1	1	↑	1	0	1	1	0	1	0	1	0
1	0	0	0	↑	1	1	0	0	1	0	1	0	1
1	0	0	1	↑	1	1	0	0	1	0	1	1	0
1	0	1	0	↑	1	1	0	0	1	1	0	0	1
1	0	1	1	↑	1	1	0	0	1	1	0	1	0
1	1	0	0	↑	1	1	0	1	0	0	1	0	1
1	1	0	1	↑	1	1	0	1	0	0	1	1	0
1	1	1	0	↑	1	1	0	1	0	1	0	0	1
1	1	1	1	↑	1	1	0	1	0	1	0	1	0
x	x	x	x	x	0	1	0	1	0	1	0	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*d0*	*d1*	*d2*	*d3*	*cp*	*sd*
fd4x4	1.0	1.0	1.0	1.0	1.9	7.2

fd4x4
4-Bit D Flip-Flop, SD, Buffered

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fd4x4	31	sd to any q	tpLH	1.00	1.08	1.25	1.42	1.60
			tpHL	1.00	1.08	1.25	1.42	1.60
		cp to any q	tpLH	1.06	1.14	1.30	1.47	1.65
			tpHL	1.16	1.21	1.30	1.39	1.47
		cp to any qn	tpLH	1.38	1.46	1.62	1.80	1.98
			tpHL	1.17	1.21	1.30	1.39	1.47
		sd to any qn	tpLH	0.83	0.88	0.97	1.06	1.14
			tpHL	0.83	0.88	0.97	1.06	1.14

Timing Constraints:

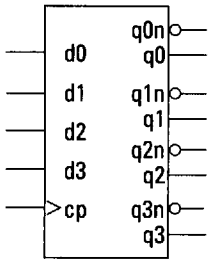
Version	*Parameters*	*Value*
fd4x4	Any d setup	0.23
	Any d hold	0.23
	cp_pw0	0.46
	cp_pw1	0.49
	sd_rcvry	-0.29
	sd_hold	0.31

Name: fd1x4l

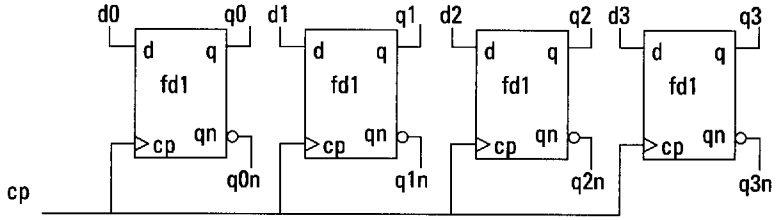
Description: 4-Bit D Flip-Flop, Buffered

Coding Syntax: u(q0,q1,q2,q3,q0n,q1n,q2n,q3n)=fd1x4l(d0,d1,d2,d3,cp)

Logic Symbol:



Schematics:



Truth Table:

d0	*d1*	*d2*	*d3*	*cp*	*q0*	*q0n*	*q1*	*q1n*	*q2*	*q2n*	*q3*	*q3n*
0	0	0	0	↑	0	1	0	1	0	1	0	1
0	0	0	1	↑	0	1	0	1	0	1	1	0
0	0	1	0	↑	0	1	0	1	1	0	0	1
0	0	1	1	↑	0	1	0	1	1	0	1	0
0	1	0	0	↑	0	1	1	0	0	1	0	1
0	1	0	1	↑	0	1	1	0	0	1	1	0
0	1	1	0	↑	0	1	1	0	1	0	0	1
0	1	1	1	↑	0	1	1	0	1	0	1	0
1	0	0	0	↑	1	0	0	1	0	1	0	1
1	0	0	1	↑	1	0	0	1	0	1	1	0
1	0	1	0	↑	1	0	0	1	1	0	0	1
1	0	1	1	↑	1	0	0	1	1	0	1	0
1	1	0	0	↑	1	0	1	0	0	1	0	1
1	1	0	1	↑	1	0	1	0	0	1	1	0
1	1	1	0	↑	1	0	1	0	1	0	0	1
1	1	1	1	↑	1	0	1	0	1	0	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*d0*	*d1*	*d2*	*d3*	*cp*
fd1x4l	1.0	1.0	1.0	1.0	1.0

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fd1x4l	23	cp to any q	tpLH	1.31	1.39	1.56	1.73	1.91
			tpHL	1.49	1.54	1.63	1.71	1.80
		cp to any qn	tpLH	1.64	1.71	1.88	2.05	2.23
			tpHL	1.42	1.47	1.55	1.64	1.72

Timing Constraints:

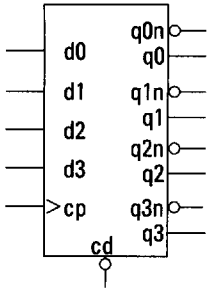
Version	*Parameters*	*Value*
fd1x4l	Any d setup	0.04
	Any d hold	0.52
	cp_pw0	0.56
	cp_pw1	0.47

Name: fd2x4l

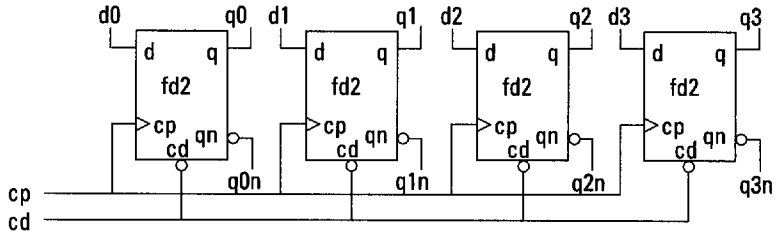
Description: 4-Bit D Flip-Flop, CD, Buffered

Coding Syntax: u(q0,q1,q2,q3,q0n,q1n,q2n,q3n)=fd2x4l(d0,d1,d2,d3,cp,cd)

Logic Symbol:



Schematics:



Truth Table:

d0	*d1*	*d2*	*d3*	*cp*	*cd*	*q0*	*q0n*	*q1*	*q1n*	*q2*	*q2n*	*q3*	*q3n*
0	0	0	0	↑	1	0	1	0	1	0	1	0	1
0	0	0	1	↑	1	0	1	0	1	0	1	1	0
0	0	1	0	↑	1	0	1	0	1	1	0	0	1
0	0	1	1	↑	1	0	1	0	1	1	0	1	0
0	1	0	0	↑	1	0	1	1	0	0	1	0	1
0	1	0	1	↑	1	0	1	1	0	0	1	1	0
0	1	1	0	↑	1	0	1	1	0	1	0	0	1
0	1	1	1	↑	1	0	1	1	0	1	0	1	0
1	0	0	0	↑	1	1	0	0	1	0	1	0	1
1	0	0	1	↑	1	1	0	0	1	0	1	1	0
1	0	1	0	↑	1	1	0	0	1	1	0	0	1
1	0	1	1	↑	1	1	0	0	1	1	0	1	0
1	1	0	0	↑	1	1	0	1	0	0	1	0	1
1	1	0	1	↑	1	1	0	1	0	0	1	1	0
1	1	1	0	↑	1	1	0	1	0	1	0	0	1
1	1	1	1	↑	1	1	0	1	0	1	0	1	0
x	x	x	x	x	0	0	1	0	1	0	1	0	1

Loading Characteristics:

Values stated in standard loads.

Version	*d0*	*d1*	*d2*	*d3*	*cp*	*cd*
fd2x4l	1.0	1.0	1.0	1.0	1.0	7.3

fd2x4l

4-Bit D Flip-Flop, CD, Buffered

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fd2x4l	30	cp to any q	tpLH	1.39	1.47	1.64	1.81	2.00
			tpHL	1.55	1.61	1.71	1.79	1.87
		cd to any q	tpLH	0.66	0.72	0.82	0.90	0.98
			tpHL	0.66	0.72	0.82	0.90	0.98
		cd to any qn	tpLH	0.91	0.99	1.15	1.32	1.50
			tpHL	0.91	0.99	1.15	1.32	1.50
		cp to any qn	tpLH	1.80	1.88	2.04	2.22	2.39
			tpHL	1.50	1.55	1.63	1.72	1.80

Timing Constraints:

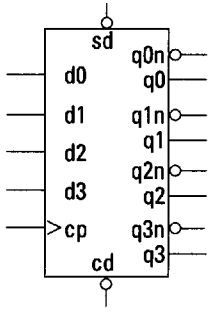
Version	*Parameters*	*Value*
fd2x4l	Any d setup	0.05
	Any d hold	0.51
	cp_pw0	0.56
	cp_pw1	0.51
	cd_rcvry	-1.02
	cd_hold	1.30

Name: fd3x4l

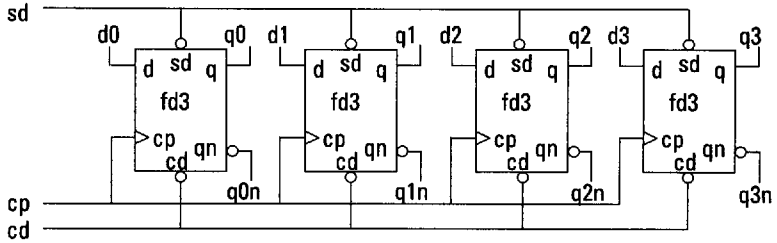
Description: 4-Bit D Flip-Flop, CD, SD, Buffered

Coding Syntax: u(q0,q1,q2,q3,q0n,q1n,q2n,q3n)=fd3x4l(d0,d1,d2,d3,cp,cd,sd)

Logic Symbol:



Schematics:



Truth Table:

d0	*d1*	*d2*	*d3*	*cp*	*cd*	*sd*	*q0*	*q0n*	*q1*	*q1n*	*q2*	*q2n*	*q3*	*q3n*
0	0	0	0	↑	1	1	0	1	0	1	0	1	0	1
0	0	0	1	↑	1	1	0	1	0	1	0	1	1	0
0	0	1	0	↑	1	1	0	1	0	1	1	0	0	1
0	0	1	1	↑	1	1	0	1	0	1	1	0	1	0
0	1	0	0	↑	1	1	0	1	1	0	0	1	0	1
0	1	0	1	↑	1	1	0	1	1	0	0	1	1	0
0	1	1	0	↑	1	1	0	1	1	0	1	0	0	1
0	1	1	1	↑	1	1	0	1	1	0	1	0	1	0
1	0	0	0	↑	1	1	1	0	0	1	0	1	0	1
1	0	0	1	↑	1	1	1	0	0	1	0	1	1	0
1	0	1	0	↑	1	1	1	0	0	1	1	0	0	1
1	0	1	1	↑	1	1	1	0	0	1	1	0	1	0
1	1	0	0	↑	1	1	1	0	1	0	0	1	0	1
1	1	0	1	↑	1	1	1	0	1	0	0	1	1	0
1	1	1	0	↑	1	1	1	0	1	0	1	0	0	1
1	1	1	1	↑	1	1	1	0	1	0	1	0	1	0
x	x	x	x	x	0	1	0	1	0	1	0	1	0	1
x	x	x	x	x	1	0	1	0	1	0	1	0	1	0
x	x	x	x	x	0	0	0	0	0	0	0	0	0	0

fd3x4l

4-Bit D Flip-Flop, CD, SD, Buffered

Loading Characteristics:

Values stated in standard loads.

Version	*d0*	*d1*	*d2*	*d3*	*cp*	*cd*	*sd*
fd3x4l	1.0	1.0	1.0	1.0	2.0	7.2	7.2

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fd3x4l	33	cp to any q	tpLH	1.43	1.52	1.68	1.85	2.03
			tpHL	1.53	1.57	1.66	1.75	1.84
		cd to any q	tpLH	0.68	0.73	0.82	0.90	0.99
			tpHL	0.68	0.73	0.82	0.90	0.99
		sd to any q	tpLH	1.11	1.20	1.36	1.53	1.71
			tpHL	1.11	1.20	1.36	1.53	1.71
		cp to any qn	tpLH	1.88	1.97	2.14	2.31	2.50
			tpHL	1.48	1.52	1.63	1.72	1.81
		cd to any qn	tpLH	1.03	1.12	1.30	1.46	1.65
			tpHL	1.03	1.12	1.30	1.46	1.65
		sd to any qn	tpLH	0.83	0.88	0.99	1.08	1.16
			tpHL	0.83	0.88	0.99	1.08	1.16

Timing Constraints:

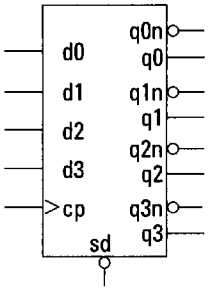
Version	*Parameters*	*Value*
fd3x4l	Any d setup	0.03
	Any d hold	0.49
	cp_pw0	0.52
	cp_pw1	0.49
	cd_rcvry	-0.97
	cd_hold	1.30
	sd_rcvry	-0.59
	sd_hold	0.64

Name: fd4x4l

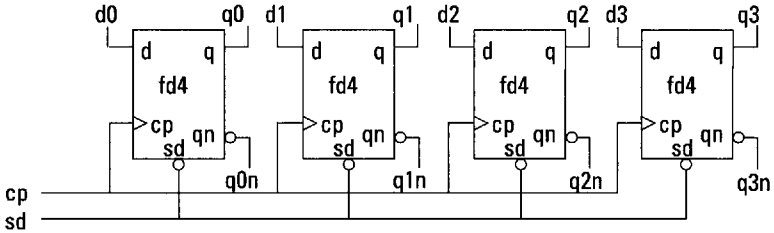
Description: 4-Bit D Flip-Flop, SD, Buffered

Coding Syntax: u(q0,q1,q2,q3,q0n,q1n,q2n,q3n)=fd4x4l(d0,d1,d2,d3,cp,sd)

Logic Symbol:



Schematics:



Truth Table:

d0	*d1*	*d2*	*d3*	*cp*	*sd*	*q0*	*q0n*	*q1*	*q1n*	*q2*	*q2n*	*q3*	*q3n*
0	0	0	0	↑	1	0	1	0	1	0	1	0	1
0	0	0	1	↑	1	0	1	0	1	0	1	1	0
0	0	1	0	↑	1	0	1	0	1	1	0	0	1
0	0	1	1	↑	1	0	1	0	1	1	0	1	0
0	1	0	0	↑	1	0	1	1	0	0	1	0	1
0	1	0	1	↑	1	0	1	1	0	0	1	1	0
0	1	1	0	↑	1	0	1	1	0	1	0	0	1
0	1	1	1	↑	1	0	1	1	0	1	0	1	0
1	0	0	0	↑	1	1	0	0	1	0	1	0	1
1	0	0	1	↑	1	1	0	0	1	0	1	1	0
1	0	1	0	↑	1	1	0	0	1	1	0	0	1
1	0	1	1	↑	1	1	0	0	1	1	0	1	0
1	1	0	0	↑	1	1	0	1	0	0	1	0	1
1	1	0	1	↑	1	1	0	1	0	0	1	1	0
1	1	1	0	↑	1	1	0	1	0	1	0	0	1
1	1	1	1	↑	1	1	0	1	0	1	0	1	0
x	x	x	x	x	0	1	0	1	0	1	0	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*d0*	*d1*	*d2*	*d3*	*cp*	*sd*
fd4x4l	1.0	1.0	1.0	1.0	1.0	7.2

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fd4x4l	30	sd to any q	tpLH	1.00	1.08	1.24	1.41	1.60
			tpHL	1.00	1.08	1.24	1.41	1.60
		cp to any q	tpLH	1.32	1.40	1.56	1.73	1.91
			tpHL	1.54	1.59	1.68	1.76	1.85
		cp to any qn	tpLH	1.76	1.84	2.00	2.17	2.35
			tpHL	1.42	1.47	1.56	1.65	1.73
		sd to any qn	tpLH	0.83	0.88	0.97	1.06	1.14
			tpHL	0.83	0.88	0.97	1.06	1.14

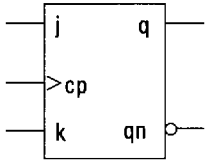
Timing Constraints:

Version	*Parameters*	*Value*
fd4x4l	Any d setup	0.04
	Any d hold	0.50
	cp_pw0	0.53
	cp_pw1	0.49
	sd_rcvry	-0.53
	sd_hold	0.59

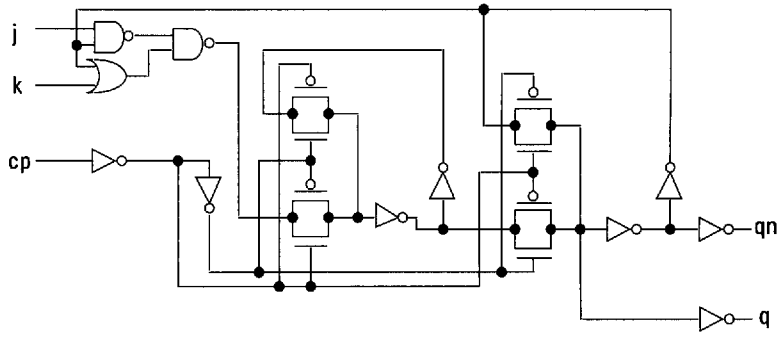
Name: fjk1 Description: JK Flip-Flop

Coding Syntax: u(q,qn)=fjk1*(j,k,cp)

Logic Symbol:



Schematics:



Truth Table:

j	*k*	*cp*	*q*	*qn*
0	0	↑	q	qn
0	1	↑	0	1
1	0	↑	1	0
1	1	↑	qn	q

Loading Characteristics:

Values stated in standard loads.

Version	*j*	*k*	*cp*
fjk1	1.0	0.5	1.0
fjk1p	1.0	0.9	1.0

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fjk1	9	cp_to_q	tpLH	0.91	0.99	1.16	1.33	1.51
			tpHL	0.87	0.93	1.04	1.13	1.22
		cp_to_qn	tpLH	1.02	1.09	1.26	1.43	1.61
			tpHL	1.03	1.07	1.16	1.24	1.33
fjk1p	10	cp_to_q	tpLH	0.88	0.93	1.02	1.10	1.18
			tpHL	0.85	0.89	0.96	1.02	1.08
		cp_to_qn	tpLH	1.06	1.10	1.18	1.26	1.35
			tpHL	1.07	1.11	1.16	1.21	1.25

fjk1
JK Flip-Flop

Timing Constraints:

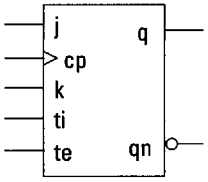
Version	*Parameters*	*Value*	*Version*	*Parameters*	*Value*
fjk1	j_setup	0.58	fjk1p	j_setup	0.58
	j_hold	0.04		j_hold	0.03
	k_setup	0.58		k_setup	0.58
	k_hold	0.04		k_hold	0.03
	cp_pw0	0.63		cp_pw0	0.61
	cp_pw1	0.47		cp_pw1	0.47

Name: fjk1s

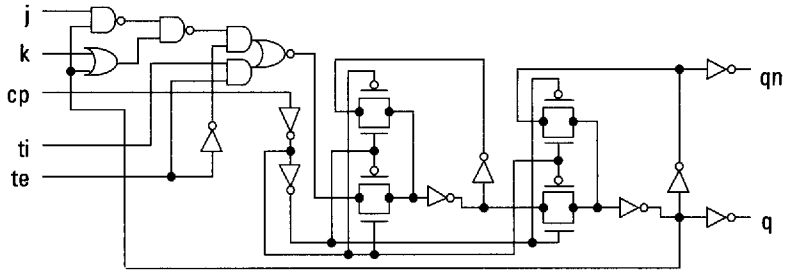
Description: JK Flip-Flop with Scan

Coding Syntax: u(q,qn)=fjk1s*(j,k,cp,ti,te)

Logic Symbol:



Schematics:



Truth Table:

j	*k*	*ti*	*te*	*cp*	*q*	*qn*
0	0	x	0	↑	q	qn
0	1	x	0	↑	0	1
1	0	x	0	↑	1	0
1	1	x	0	↑	qn	q
x	x	0	1	↑	0	1
x	x	1	1	↑	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*j*	*k*	*cp*	*ti*	*te*
fjk1s	1.0	0.9	1.0	0.5	1.9
fjk1sp	1.0	0.9	1.0	1.0	1.9

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fjk1s	11	cp_to_qn	tpLH	1.25	1.33	1.49	1.66	1.85
			tpHL	1.16	1.21	1.29	1.38	1.46
		cp_to_q	tpLH	1.05	1.13	1.30	1.47	1.65
			tpHL	1.11	1.16	1.26	1.34	1.43

AC Characteristics: (Cont.)

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fjk1sp	12	cp_to_qn	tpLH	1.29	1.33	1.41	1.49	1.57
			tpHL	1.19	1.23	1.28	1.33	1.37
		cp_to_q	tpLH	1.02	1.07	1.15	1.23	1.32
			tpHL	1.10	1.13	1.20	1.25	1.30

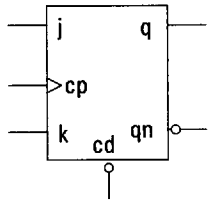
Timing Constraints:

Version	*Parameters*	*Value*	*Version*	*Parameters*	*Value*
fjk1s	j_setup	0.73	fjk1sp	j_setup	0.75
	j_hold	-0.09		j_hold	-0.09
	k_setup	0.73		k_setup	0.75
	k_hold	-0.09		k_hold	-0.09
	te_setup	0.58		te_setup	0.56
	te_hold	0.07		te_hold	0.06
	ti_setup	0.56		ti_setup	0.56
	ti_hold	0.09		ti_hold	0.06
	cp_pw0	0.42		cp_pw0	0.43
	cp_pw1	0.47		cp_pw1	0.47

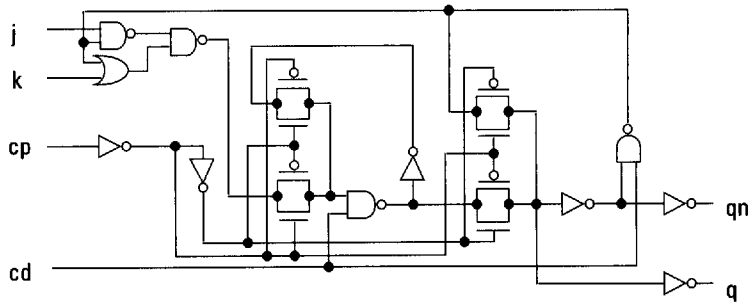
Name: fjk2 Description: JK Flip-Flop with Clear

Coding Syntax: u(q,qn)=fjk2*(j,k,cp,cd)

Logic Symbol:



Schematics:



Truth Table:

j	*k*	*cp*	*cd*	*q*	*qn*
0	0	↑	1	q	qn
0	1	↑	1	0	1
1	0	↑	1	1	0
1	1	↑	1	qn	q
x	x	x	0	0	1

Loading Characteristics:

Values stated in standard loads.

Version	*j*	*k*	*cp*	*cd*
fjk2	1.0	0.9	1.0	1.8
fjk2p	1.0	0.9	1.0	1.8

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fjk2	10	cp_to_q	tpLH	0.96	1.06	1.23	1.41	1.59
			tpHL	0.88	0.94	1.06	1.15	1.24
		cd_to_q	tpLH	0.94	1.00	1.12	1.21	1.30
			tpHL	0.94	1.00	1.12	1.21	1.30
		cp_to_qn	tpLH	1.03	1.11	1.27	1.44	1.62
			tpHL	1.08	1.13	1.22	1.30	1.39
		cd_to_qn	tpLH	1.09	1.17	1.33	1.50	1.68
			tpHL	1.09	1.17	1.33	1.50	1.68
fjk2p	11	cp_to_q	tpLH	0.95	1.00	1.09	1.18	1.28
			tpHL	0.86	0.90	0.98	1.03	1.09
		cd_to_q	tpLH	0.96	1.00	1.07	1.13	1.19
			tpHL	0.96	1.00	1.07	1.13	1.19
		cp_to_qn	tpLH	1.08	1.12	1.20	1.28	1.36
			tpHL	1.15	1.18	1.24	1.29	1.33
		cd_to_qn	tpLH	1.17	1.21	1.29	1.38	1.46
			tpHL	1.17	1.21	1.29	1.38	1.46

Timing Constraints:

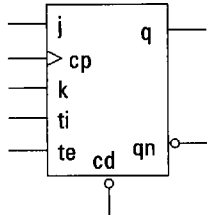
Version	*Parameters*	*Value*	*Version*	*Parameters*	*Value*
fjk2	j_setup	0.57	fjk2p	j_setup	0.57
	j_hold	-0.30		j_hold	-0.29
	k_setup	0.57		k_setup	0.57
	k_hold	-0.30		k_hold	-0.29
	cp_pw0	0.27		cp_pw0	0.28
	cp_pw1	0.49		cp_pw1	0.49
	cd_rcvry	-0.15		cd_rcvry	-0.10
	cd_hold	0.25		cd_hold	0.20

Name: fjk2s

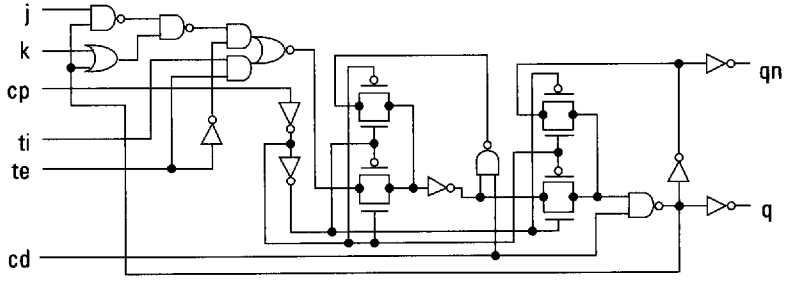
Description: JK Flip-Flop with Clear, Scan

Coding Syntax: u(q,qn)=fjk2s*(j,k,cp,cd,ti,te)

Logic Symbol:



Schematics:



Truth Table:

j	*k*	*ti*	*te*	*cp*	*cd*	*q*	*qn*
0	0	x	0	↑	1	q	qn
0	1	x	0	↑	1	0	1
1	0	x	0	↑	1	1	0
1	1	x	0	↑	1	qn	q
x	x	0	1	↑	1	0	1
x	x	1	1	↑	1	1	0
x	x	x	x	x	0	0	1

Loading Characteristics:

Values stated in standard loads.

Version	*j*	*k*	*cp*	*cd*	*ti*	*te*
fjk2s	1.0	0.9	1.0	1.8	1.0	1.9
fjk2sp	1.0	0.9	1.0	1.8	1.0	1.9

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fjk2s	13	cp_to_qn	tpLH	1.34	1.42	1.58	1.75	1.93
			tpHL	1.23	1.28	1.37	1.45	1.53
		cd_to_qn	tpLH	1.01	1.09	1.26	1.42	1.61
			tpHL	1.01	1.09	1.26	1.42	1.61
		cp_to_q	tpLH	1.12	1.21	1.38	1.56	1.73
			tpHL	1.08	1.13	1.24	1.33	1.42
		cd_to_q	tpLH	0.75	0.81	0.92	1.01	1.09
			tpHL	0.75	0.81	0.92	1.01	1.09
fjk2sp	14	cp_to_qn	tpLH	1.37	1.42	1.50	1.58	1.66
			tpHL	1.28	1.32	1.37	1.42	1.47
		cd_to_qn	tpLH	1.07	1.12	1.21	1.29	1.37
			tpHL	1.07	1.12	1.21	1.29	1.37
		cp_to_q	tpLH	1.10	1.15	1.24	1.33	1.41
			tpHL	1.07	1.11	1.17	1.23	1.28
		cd_to_q	tpLH	0.77	0.81	0.87	0.93	0.99
			tpHL	0.77	0.81	0.87	0.93	0.99

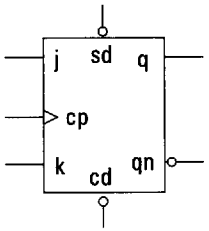
Timing Constraints:

Version	*Parameters*	*Value*	*Version*	*Parameters*	*Value*
fjk2s	j_setup	0.97	fjk2sp	j_setup	0.97
	j_hold	-0.27		j_hold	-0.28
	k_setup	0.97		k_setup	0.97
	k_hold	-0.27		k_hold	-0.28
	ti_setup	0.67		ti_setup	0.67
	ti_hold	-0.03		ti_hold	-0.04
	te_setup	0.67		te_setup	0.67
	te_hold	-0.03		te_hold	-0.04
	cd_rcvry	-0.42		cd_rcvry	-0.50
	cd_hold	0.78		cd_hold	0.78
	cp_pw0	0.63		cp_pw0	0.63
	cp_pw1	0.51		cp_pw1	0.51

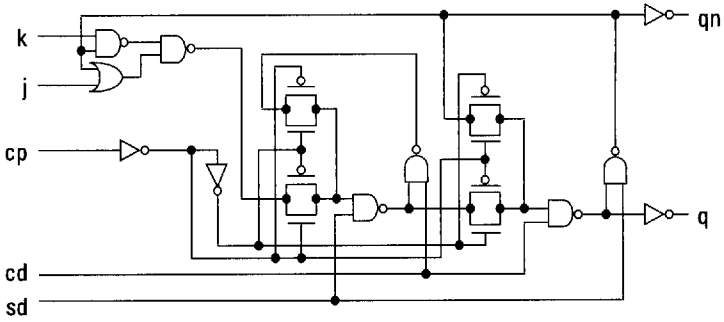
Name: fjk3 Description: JK Flip-Flop with Clear, Set

Coding Syntax: u(q,qn)=fjk3*(j,k,cp,cd,sd)

Logic Symbol:



Schematics:



Truth Table:

j	*k*	*cp*	*cd*	*sd*	*q*	*qn*
0	0	↑	1	1	q	qn
0	1	↑	1	1	0	1
1	0	↑	1	1	1	0
1	1	↑	1	1	qn	q
x	x	x	0	1	0	1
x	x	x	1	0	1	0
x	x	x	0	0	0	0

Loading Characteristics:

Values stated in standard loads.

Version	*j*	*k*	*cp*	*cd*	*sd*
fjk3	0.9	1.0	1.0	1.8	1.8
fjk3p	0.9	1.0	1.0	1.8	1.8

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fjk3	11	cp_to_q	tpLH	1.07	1.16	1.32	1.49	1.67
			tpHL	1.02	1.07	1.16	1.24	1.32
		cd_to_q	tpLH	0.63	0.68	0.77	0.85	0.93
			tpHL	0.63	0.68	0.77	0.85	0.93
		sd_to_q	tpLH	1.26	1.34	1.50	1.67	1.85
			tpHL	1.26	1.34	1.50	1.67	1.85
		cp_to_qn	tpLH	1.45	1.54	1.72	1.89	2.08
			tpHL	1.20	1.26	1.35	1.44	1.52
		cd_to_qn	tpLH	1.06	1.15	1.33	1.50	1.68
			tpHL	1.06	1.15	1.33	1.50	1.68
		sd_to_qn	tpLH	0.99	1.04	1.14	1.22	1.31
			tpHL	0.99	1.04	1.14	1.22	1.31
fjk3p	12	cp_to_q	tpLH	1.05	1.10	1.19	1.27	1.35
			tpHL	1.02	1.06	1.11	1.16	1.21
		cd_to_q	tpLH	0.66	0.70	0.75	0.80	0.85
			tpHL	0.66	0.70	0.75	0.80	0.85
		sd_to_q	tpLH	1.33	1.38	1.47	1.55	1.64
			tpHL	1.33	1.38	1.47	1.55	1.64
		cp_to_qn	tpLH	1.50	1.55	1.64	1.74	1.82
			tpHL	1.25	1.29	1.35	1.40	1.45
		cd_to_qn	tpLH	1.14	1.20	1.29	1.38	1.47
			tpHL	1.14	1.20	1.29	1.38	1.47
		sd_to_qn	tpLH	1.00	1.04	1.10	1.15	1.20
			tpHL	1.00	1.04	1.10	1.15	1.20

Timing Constraints:

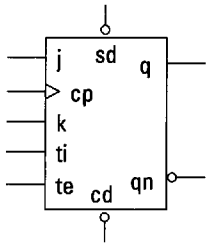
Version	*Parameters*	*Value*	*Version*	*Parameters*	*Value*
fjk3	j_setup	0.58	fjk3p	j_setup	0.59
	j_hold	-0.00		j_hold	-0.00
	k_setup	0.58		k_setup	0.59
	k_hold	-0.00		k_hold	-0.00
	cp_pw0	0.58		cp_pw0	0.58
	cp_pw1	0.53		cp_pw1	0.53
	cd_rcvry	-0.53		cd_rcvry	-0.52
	cd_hold	0.86		cd_hold	0.86
	sd_rcvry	-0.20		sd_rcvry	-0.20
	sd_hold	0.79		sd_hold	0.79

Name: fjk3s

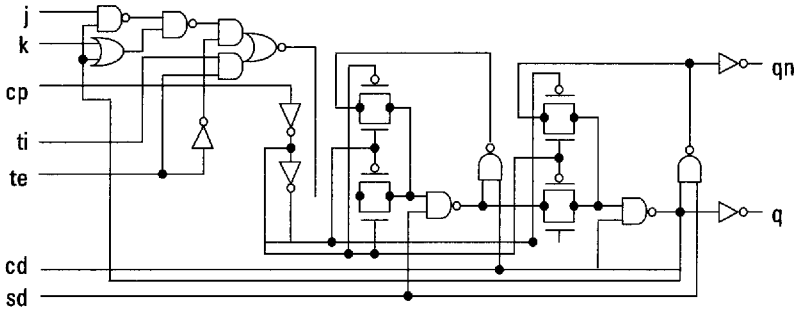
Description: JK Flip-Flop with Clear, Set, and Scan

Coding Syntax: u(q,qn)=fjk3s*(j,k,cp,cd,sd,ti,te)

Logic Symbol:



Schematics:



Truth Table:

j	*k*	*ti*	*te*	*cp*	*cd*	*sd*	*q*	*qn*
0	0	x	0	↑	1	1	q	qn
0	1	x	0	↑	1	1	0	1
1	0	x	0	↑	1	1	1	0
1	1	x	0	↑	1	1	qn	q
x	x	0	1	↑	1	1	0	1
x	x	1	1	↑	1	1	1	0
x	x	x	x	x	0	1	0	1
x	x	x	x	x	1	0	1	0
x	x	x	x	x	0	0	0	0

Loading Characteristics:

Values stated in standard loads.

Version	*j*	*k*	*cp*	*cd*	*sd*	*ti*	*te*
fjk3s	1.0	0.9	1.0	1.8	1.8	1.0	1.9
fjk3sp	1.0	0.9	1.0	1.8	1.8	1.0	1.9

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
fjk3s	13	cp_to_qn	tpLH	1.51	1.60	1.77	1.94	2.12
			tpHL	1.23	1.29	1.41	1.51	1.59
		cd_to_qn	tpLH	1.17	1.26	1.43	1.60	1.78
			tpHL	1.17	1.26	1.43	1.60	1.78
		sd_to_qn	tpLH	0.84	0.90	1.01	1.11	1.20
			tpHL	0.84	0.90	1.01	1.11	1.20
		cp_to_q	tpLH	1.18	1.27	1.44	1.61	1.79
			tpHL	1.12	1.18	1.27	1.36	1.45
		cd_to_q	tpLH	0.78	0.84	0.93	1.02	1.11
			tpHL	0.78	0.84	0.93	1.02	1.11
		sd_to_q	tpLH	1.27	1.35	1.52	1.69	1.87
			tpHL	1.27	1.35	1.52	1.69	1.87
fjk3sp	14	cp_to_qn	tpLH	1.56	1.61	1.70	1.79	1.87
			tpHL	1.29	1.32	1.39	1.45	1.51
		cd_to_qn	tpLH	1.24	1.29	1.39	1.48	1.56
			tpHL	1.24	1.29	1.39	1.48	1.56
		sd_to_qn	tpLH	0.86	0.89	0.96	1.02	1.08
			tpHL	0.86	0.89	0.96	1.02	1.08
		cp_to_q	tpLH	1.15	1.20	1.29	1.38	1.46
			tpHL	1.11	1.15	1.21	1.26	1.31
		cd_to_q	tpLH	0.79	0.83	0.90	0.95	1.00
			tpHL	0.79	0.83	0.90	0.95	1.00
		sd_to_q	tpLH	1.34	1.39	1.48	1.57	1.65
			tpHL	1.34	1.39	1.48	1.57	1.65

fjk3s
JK Flip-Flop with Clear, Set, and Scan

Timing Constraints:

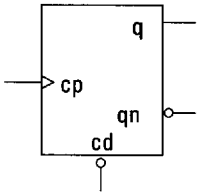
Version	*Parameters*	*Value*	*Version*	*Parameters*	*Value*
fjk3s	j_setup	0.93	fjk3sp	j_setup	0.93
	j_hold	-0.14		j_hold	-0.14
	k_setup	0.93		k_setup	0.93
	k_hold	-0.14		k_hold	-0.14
	ti_setup	0.67		ti_setup	0.67
	ti_hold	-0.05		ti_hold	-0.05
	te_setup	0.67		te_setup	0.67
	te_hold	-0.05		te_hold	-0.05
	cd_rcvry	-0.42		cd_rcvry	-0.42
	cd_hold	0.86		cd_hold	0.86
	sd_rcvry	-0.20		sd_rcvry	-0.20
	sd_hold	0.59		sd_hold	0.60
	cp_pw0	0.61		cp_pw0	0.62
	cp_pw1	0.53		cp_pw1	0.53

Name: ft2

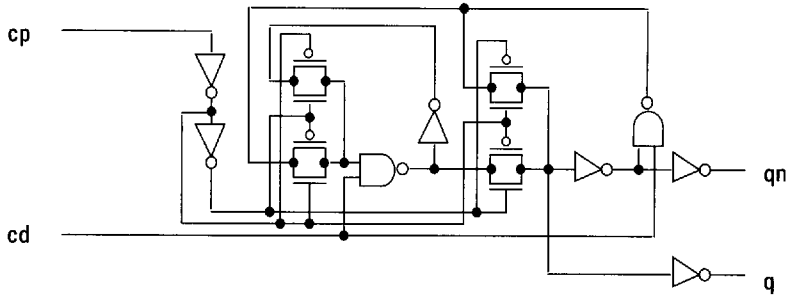
Description: Toggle Flip-Flop with Clear

Coding Syntax: u(q,qn)=ft2*(cp,cd)

Logic Symbol:



Schematics:



Truth Table:

cp	*cd*	*q*	*qn*
↑	1	qn	q
x	0	0	1

Loading Characteristics:

Values stated in standard loads.

Version	*cp*	*cd*
ft2	1.0	1.8
ft2p	1.0	1.8

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
ft2	7	cp_to_q	tpLH	1.00	1.09	1.27	1.44	1.63
			tpHL	0.92	0.98	1.10	1.20	1.29
		cp_to_qn	tpLH	1.07	1.14	1.31	1.48	1.66
			tpHL	1.12	1.17	1.26	1.34	1.42
		cd_to_q	tpLH	1.06	1.12	1.24	1.34	1.43
			tpHL	1.06	1.12	1.24	1.34	1.43
		cd_to_qn	tpLH	1.21	1.29	1.45	1.62	1.80
			tpHL	1.21	1.29	1.45	1.62	1.80

ft2

Toggle Flip-Flop with Clear

AC Characteristics: (Cont.)

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
ft2p	8	cp_to_q	tpLH	0.98	1.04	1.13	1.22	1.31
			tpHL	0.90	0.94	1.01	1.07	1.13
		cp_to_qn	tpLH	1.11	1.15	1.23	1.31	1.40
			tpHL	1.18	1.22	1.28	1.33	1.37
		cd_to_q	tpLH	1.08	1.12	1.19	1.25	1.31
			tpHL	1.08	1.12	1.19	1.25	1.31
		cd_to_qn	tpLH	1.29	1.33	1.41	1.49	1.57
			tpHL	1.29	1.33	1.41	1.49	1.57

Timing Constraints:

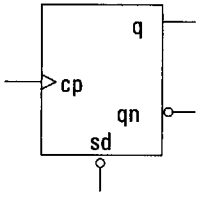
Version	*Parameters*	*Value*	*Version*	*Parameters*	*Value*
ft2	cd_rcvry	0.16	ft2p	cd_rcvry	0.20
	cd_hold	0.29		cd_hold	0.25
	cp_pw0	0.50		cp_pw0	0.50
	cp_pw1	0.49		cp_pw1	0.49

Name: ft4

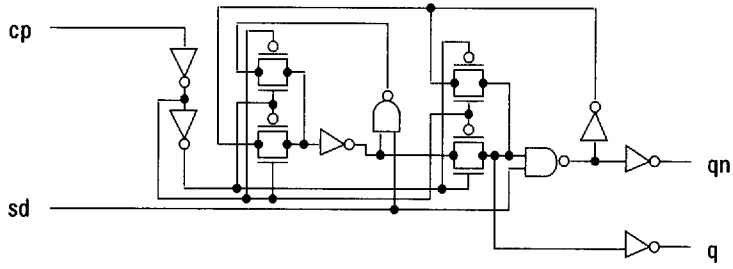
Description: Toggle Flip-Flop with Set

Coding Syntax: u(q,qn)=ft4*(cp,sd)

Logic Symbol:



Schematics:



Truth Table:

cp	*sd*	*q*	*qn*
↑	1	qn	q
x	0	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*cp*	*sd*
ft4	1.0	1.6
ft4p	1.0	1.6

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
ft4	8	cp_to_q	tpLH	0.95	1.04	1.21	1.38	1.56
			tpHL	0.91	0.97	1.08	1.17	1.26
		cp_to_qn	tpLH	1.11	1.20	1.36	1.54	1.72
			tpHL	1.11	1.16	1.25	1.33	1.42
		sd_to_q	tpLH	1.12	1.21	1.38	1.55	1.73
			tpHL	1.12	1.21	1.38	1.55	1.73
		sd_to_qn	tpLH	0.72	0.77	0.86	0.95	1.03
			tpHL	0.72	0.77	0.86	0.95	1.03

AC Characteristics: (Cont.)

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
ft4p	9	cp_to_q	tpLH	0.92	0.97	1.06	1.15	1.23
			tpHL	0.90	0.94	1.01	1.07	1.12
		cp_to_qn	tpLH	1.15	1.20	1.29	1.38	1.46
			tpHL	1.15	1.18	1.24	1.29	1.34
		sd_to_q	tpLH	1.23	1.27	1.36	1.45	1.54
			tpHL	1.23	1.27	1.36	1.45	1.54
		sd_to_qn	tpLH	0.78	0.81	0.87	0.92	0.96
			tpHL	0.78	0.81	0.87	0.92	0.96

Timing Constraints:

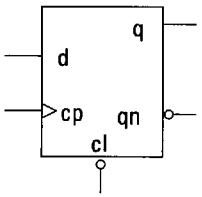
Version	*Parameters*	*Value*	*Version*	*Parameters*	*Value*
ft4	sd_rcvry	-0.81	ft4p	sd_rcvry	-0.77
	sd_hold	0.95		sd_hold	0.87
	cp_pw0	0.55		cp_pw0	0.68
	cp_pw1	0.51		cp_pw1	0.51

Name: sfd2

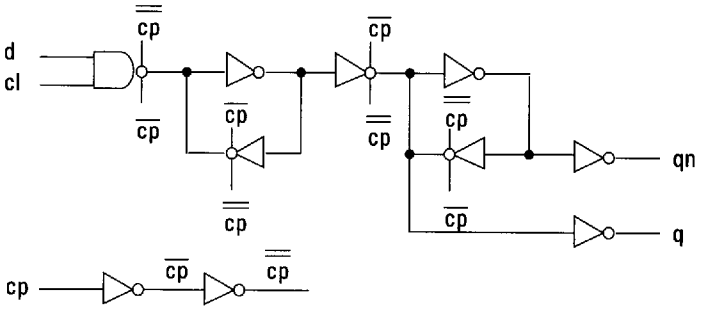
Description: D Flip-Flop with Synchronous Clear

Coding Syntax: u(q,qn)=sfd2*(d,cp,cl)

Logic Symbol:



Schematics:



Truth Table:

d	*cp*	*cl*	*q*	*qn*
x	↑	0	0	1
0	↑	x	0	1
1	↑	1	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*d*	*cp*	*cl*
sfd2	1.0	1.0	1.0
sfd2p	1.0	1.0	1.0

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
sfd2	8	cp_to_q	tpLH	1.00	1.08	1.25	1.42	1.60
			tpHL	0.96	1.02	1.14	1.23	1.32
		cp_to_qn	tpLH	1.12	1.20	1.36	1.53	1.71
			tpHL	1.11	1.16	1.25	1.34	1.42
sfd2p	9	cp_to_q	tpLH	0.98	1.02	1.11	1.19	1.28
			tpHL	0.97	1.01	1.09	1.15	1.21
		cp_to_qn	tpLH	1.20	1.24	1.32	1.40	1.48
			tpHL	1.17	1.20	1.26	1.30	1.35

sfd2
D Flip-Flop with Synchronous Clear

Timing Constraints:

Version	*Parameters*	*Value*	*Version*	*Parameters*	*Value*
sfd2	d_setup	0.40	sfd2p	d_setup	0.40
	d_hold	0.24		d_hold	0.24
	cl_setup	0.40		cl_setup	0.40
	cl_hold	0.24		cl_hold	0.24
	cp_pw0	0.64		cp_pw0	0.43
	cp_pw1	0.62		cp_pw1	0.62

2.4 Latches

This section contains data pages for LCA300K latches.

Naming Conventions

A latches root name is given at the top of each data page. Latch names with the suffix `p` have a high output drive strength. Latch names with no suffix have a standard output drive strength.

For example:

`ld1p` has high output drive strength.

`ld1` has standard output drive strength.

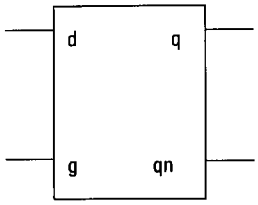
➤ ***Note:*** For the coding syntax, an asterisk following the cell name (for example, `ld1*`) is a wildcard symbol for the `p` option.

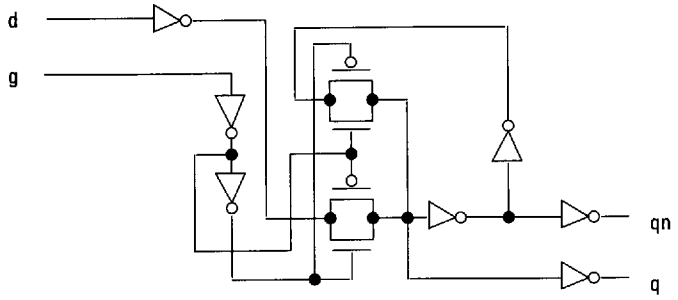
ld1
D Latch

Name: ld1 Description: D Latch

Coding Syntax: u(q,qn)=ld1*(d,g)

Logic Symbol: Schematics:





Truth Table:

d	*g*	*q*	*qn*
0	1	0	1
1	1	1	0
x	0	q	qn

Loading Characteristics:

Values stated in standard loads.

Version	*d*	*g*
ld1	1.0	1.0
ld1p	1.0	1.0

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
ld1	5	d_to_q	tpLH	0.89	0.97	1.15	1.32	1.50
			tpHL	0.90	0.96	1.07	1.16	1.25
		d_to_qn	tpLH	1.05	1.12	1.29	1.46	1.64
			tpHL	1.01	1.06	1.15	1.23	1.32
		g_to_q	tpLH	0.79	0.87	1.04	1.22	1.40
			tpHL	0.79	0.85	0.96	1.05	1.14
		g_to_qn	tpLH	0.93	1.01	1.17	1.35	1.53
			tpHL	0.91	0.96	1.05	1.13	1.21

AC Characteristics: (Cont.)

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
ld1p	6	d_to_q	tpLH	0.91	0.96	1.05	1.13	1.22
			tpHL	0.87	0.91	0.99	1.04	1.10
		d_to_qn	tpLH	1.07	1.12	1.20	1.28	1.37
			tpHL	1.11	1.14	1.20	1.25	1.29
		g_to_q	tpLH	0.76	0.81	0.89	0.98	1.06
			tpHL	0.77	0.81	0.88	0.94	1.00
		g_to_qn	tpLH	0.97	1.02	1.10	1.18	1.26
			tpHL	0.95	0.99	1.05	1.09	1.14

Timing Constraints:

Version	*Parameters*	*Value*	*Version*	*Parameters*	*Value*
ld1	d_setup	0.47	ld1p	d_setup	0.53
	d_hold	0.00		d_hold	0.05
	g_pw0	0.47		g_pw0	0.58
	g_pw1	0.47		g_pw1	0.58

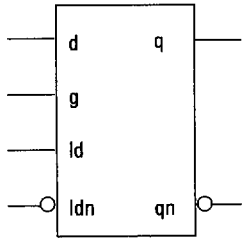
ld1lp
D Latch with Enable, Buffered, Double Drive

Name: ld1lp

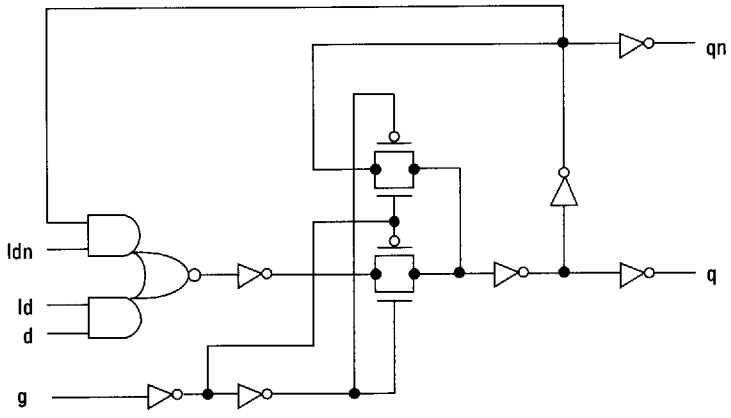
Description: D Latch with Enable, Buffered, Double Drive

Coding Syntax: u(q,qn)=ld1lp(d,g,ld,ldn)

Logic Symbol:



Schematics:



Truth Table:

g	*ld*	*ldn*	*d*	*q*	*qn*
0	x	x	x	q	qn
1	0	0	x	0	1
1	0	1	x	q	qn
1	1	0	0	0	1
1	1	0	1	1	0
1	1	1	0	q	qn
1	1	1	1	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*d*	*g*	*ld*	*ldn*
ld1lp	1.0	1.0	1.0	1.0

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
ld1lp	8	d_to_q	tpLH	1.31	1.35	1.43	1.51	1.60
			tpHL	1.34	1.38	1.43	1.48	1.52
		d_to_qn	tpLH	1.51	1.56	1.64	1.72	1.80
			tpHL	1.48	1.52	1.57	1.62	1.67
		ld_to_q	tpLH	1.31	1.35	1.43	1.51	1.60
			tpHL	1.34	1.38	1.43	1.48	1.52
		ld_to_qn	tpLH	1.51	1.56	1.64	1.72	1.80
			tpHL	1.48	1.52	1.57	1.62	1.67
		ldn_to_q	tpLH	1.31	1.35	1.43	1.51	1.60
			tpHL	1.34	1.38	1.43	1.48	1.52
		ldn_to_qn	tpLH	1.51	1.56	1.64	1.72	1.80
			tpHL	1.48	1.52	1.57	1.62	1.67
		g_to_q	tpLH	0.83	0.87	0.95	1.03	1.11
			tpHL	0.83	0.86	0.91	0.96	1.00
		g_to_qn	tpLH	1.00	1.04	1.12	1.20	1.28
			tpHL	1.00	1.04	1.09	1.14	1.18

Timing Constraints:

Version	*Parameters*	*Value*
ld1lp	d_setup	0.61
	d_hold	-0.09
	g_pw0	0.52
	g_pw1	0.52

ld1s2

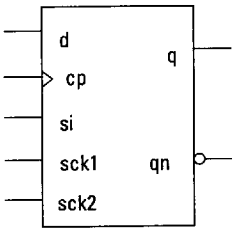
D Latch with 2 Scan Clock Control

Name: ld1s2

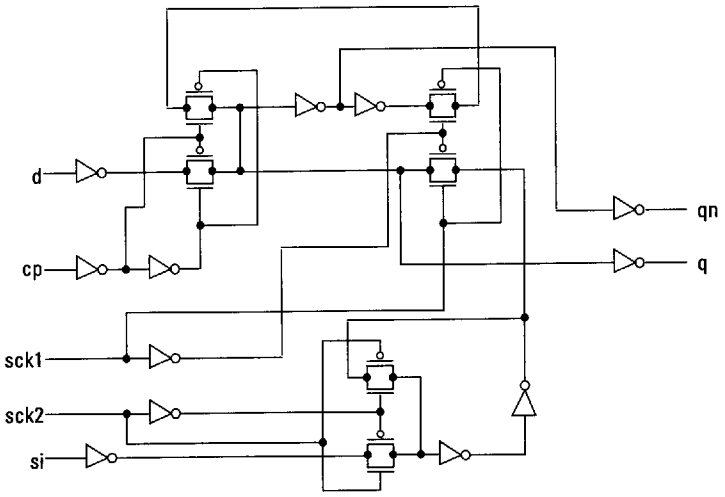
Description: D Latch with 2 Scan Clock Control

Coding Syntax: u(q,qn)=ld1s2*(d,cp,sck1,sck2,si)

Logic Symbol:



Schematics:



Truth Table:

cp	*sck1*	*sck2*	*q*	*qn*
1	0	x	d	$\overline{d}$
0	1	1	si	$\overline{si}$

Loading Characteristics:

Values stated in standard loads.

Version	*d*	*cp*	*sck1*	*sck2*	*si*
ld1s2	1.0	1.0	1.5	1.4	1.0
ld1s2p	1.0	1.0	1.5	1.4	1.0

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
ld1s2	9	d_to_q	tpLH	0.94	1.03	1.20	1.37	1.55
			tpHL	0.93	0.99	1.10	1.21	1.31
		d_to_qn	tpLH	1.08	1.16	1.32	1.49	1.68
			tpHL	1.05	1.11	1.19	1.27	1.36
		cp_to_q	tpLH	0.90	0.99	1.17	1.34	1.52
			tpHL	0.81	0.87	0.99	1.09	1.19
		cp_to_qn	tpLH	0.96	1.04	1.20	1.37	1.56
			tpHL	1.02	1.07	1.16	1.24	1.33
		sck1_to_q	tpLH	0.96	1.05	1.23	1.40	1.58
			tpHL	0.87	0.93	1.05	1.15	1.25
		sck1_to_qn	tpLH	1.02	1.10	1.26	1.43	1.62
			tpHL	1.08	1.13	1.22	1.30	1.39
		sck2_to_q	tpLH	1.02	1.11	1.28	1.45	1.64
			tpHL	1.14	1.20	1.31	1.42	1.52
		sck2_to_qn	tpLH	1.29	1.37	1.53	1.70	1.89
			tpHL	1.13	1.19	1.28	1.36	1.44
ld1s2p	10	d_to_q	tpLH	0.94	0.99	1.09	1.17	1.26
			tpHL	0.90	0.94	1.01	1.07	1.13
		d_to_qn	tpLH	1.11	1.15	1.23	1.31	1.40
			tpHL	1.14	1.18	1.24	1.29	1.33
		cp_to_q	tpLH	0.90	0.95	1.04	1.13	1.22
			tpHL	0.79	0.83	0.91	0.97	1.03
		cp_to_qn	tpLH	1.00	1.05	1.13	1.21	1.29
			tpHL	1.10	1.14	1.19	1.25	1.29
		sck1_to_q	tpLH	0.97	1.03	1.12	1.21	1.30
			tpHL	0.87	0.91	0.98	1.04	1.10
		sck1_to_qn	tpLH	1.08	1.12	1.20	1.28	1.37
			tpHL	1.18	1.21	1.27	1.32	1.36
		sck2_to_q	tpLH	0.99	1.04	1.13	1.22	1.31
			tpHL	1.11	1.15	1.22	1.29	1.34
		sck2_to_qn	tpLH	1.32	1.36	1.44	1.53	1.61
			tpHL	1.19	1.22	1.28	1.33	1.38

ld1s2

D Latch with 2 Scan Clock Control

Timing Constraints:

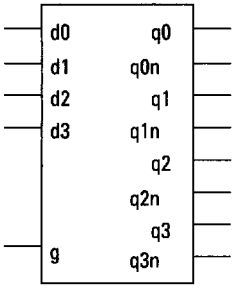
Version	*Parameters*	*Value*	*Version*	*Parameters*	*Value*
ld1s2	d_setup	0.46	ld1s2p	d_setup	0.57
	d_hold	0.12		d_hold	-0.02
	cp_pw0	0.50		cp_pw0	0.49
	cp_pw1	0.50		cp_pw1	0.49
	sck2_pw	1.44		sck2_pw	1.45
	si_setup	1.95		si_setup	1.96
	si_hold	-0.15		si_hold	-0.15

Name: ld1x4

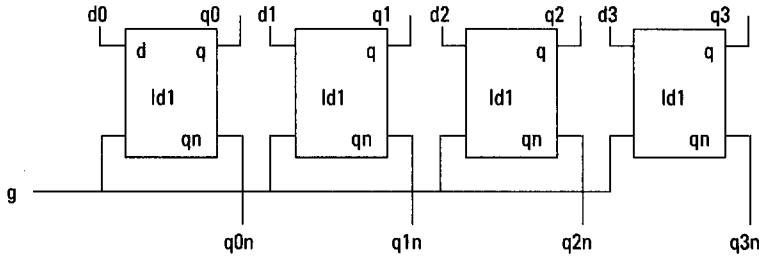
Description: 4 LD1 in Parallel with Common Gates

Coding Syntax: u(q0,q1,q2,q3,q0n,q1n,q2n,q3n)=ld1x4*(d0,d1,d2,d3,g)

Logic Symbol:



Schematics:



Truth Table:

g	*d0*	*q0*	*q0n*
1	0	0	1
1	1	1	0
0	x	q0	q0n

Loading Characteristics:

Values stated in standard loads.

Version	*d0*	*d1*	*d2*	*d3*	*g*
ld1x4	1.0	1.0	1.0	1.0	2.0
ld1x4p	1.0	1.0	1.0	1.0	2.0

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
ld1x4	16	Any d to any q	tpLH	0.90	0.98	1.15	1.32	1.50
			tpHL	0.84	0.91	1.03	1.14	1.24
		Any d to any qn	tpLH	0.99	1.07	1.24	1.41	1.59
			tpHL	1.02	1.07	1.16	1.24	1.32
		g to any q	tpLH	0.84	0.92	1.09	1.26	1.44
			tpHL	0.85	0.91	1.03	1.14	1.24
		g to any qn	tpLH	0.99	1.07	1.24	1.41	1.59
			tpHL	0.96	1.01	1.10	1.18	1.26

ld1x4
4 LD1 in Parallel with Common Gates

AC Characteristics: (Cont.)

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
ld1x4p	20	Any d to any q	tpLH	0.91	0.96	1.05	1.13	1.22
			tpHL	0.87	0.92	0.99	1.05	1.10
		Any d to any qn	tpLH	1.08	1.12	1.20	1.28	1.37
			tpHL	1.11	1.14	1.20	1.25	1.29
		g to any q	tpLH	0.81	0.86	0.94	1.03	1.11
			tpHL	0.83	0.87	0.94	1.00	1.06
		g to any qn	tpLH	1.03	1.07	1.15	1.23	1.32
			tpHL	1.00	1.04	1.10	1.15	1.19

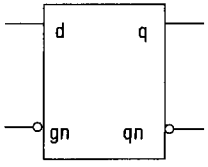
Timing Constraints:

Version	*Parameters*	*Value*	*Version*	*Parameters*	*Value*
ld1x4	Any d setup	0.37	ld1x4p	Any d setup	0.57
	Any d hold	0.34		Any d hold	-0.04
	Any g pw	0.71		Any g pw	0.47

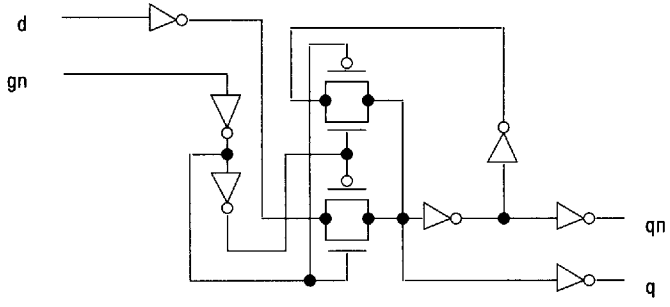
Name: ld2 Description: D Latch

Coding Syntax: u (q,qn)=ld2*(d,gn)

Logic Symbol:



Schematics:



Truth Table:

d	*gn*	*q0*	*q0n*
0	0	0	1
1	0	1	0
x	1	q0	q0n

Loading Characteristics:

Values stated in standard loads.

Version	*d*	*gn*
ld2	1.0	0.5
ld2p	1.0	0.5

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
ld2	5	d_to_q	tpLH	0.90	0.98	1.15	1.32	1.50
			tpHL	0.84	0.90	1.03	1.14	1.24
		d_to_qn	tpLH	0.99	1.07	1.23	1.40	1.58
			tpHL	1.02	1.07	1.16	1.24	1.32
		gn_to_q	tpLH	0.82	0.90	1.07	1.24	1.42
			tpHL	0.81	0.87	1.00	1.11	1.21
		gn_to_qn	tpLH	0.96	1.04	1.20	1.37	1.55
			tpHL	0.94	0.99	1.08	1.16	1.24

AC Characteristics: (Cont.)

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
ld2p	6	d_to_q	tpLH	0.92	0.97	1.05	1.13	1.22
			tpHL	0.87	0.91	0.98	1.04	1.10
		d_to_qn	tpLH	1.08	1.12	1.20	1.28	1.37
			tpHL	1.12	1.15	1.20	1.25	1.30
		gn_to_q	tpLH	0.80	0.85	0.93	1.02	1.10
			tpHL	0.80	0.84	0.91	0.97	1.03
		gn_to_qn	tpLH	1.00	1.05	1.13	1.21	1.29
			tpHL	1.00	1.03	1.09	1.14	1.18

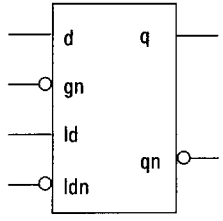
Timing Constraints:

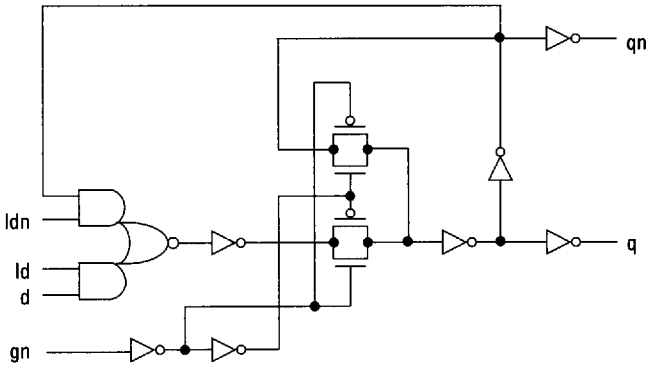
Version	*Parameters*	*Value*	*Version*	*Parameters*	*Value*
ld2	d_setup	0.50	ld2p	d_setup	0.59
	d_hold	0.00		d_hold	0.00
	gn_pw0	0.45		gn_pw0	0.55
	gn_pw1	0.45		gn_pw1	0.55

Name: ld2lp Description: D Latch, Active Low with Enable, Buffered, Double Drive

Coding Syntax: u(q,qn)=ld2lp(d,gn,ld,ldn)

Logic Symbol: Schematics:





Truth Table:

gn	*ld*	*ldn*	*d*	*q*	*qn*
1	x	x	x	q	qn
0	0	0	x	0	1
0	0	1	x	q	qn
0	1	0	0	0	1
0	1	0	1	1	0
0	1	1	0	q	qn
0	1	1	1	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*d*	*gn*	*ld*	*ldn*
ld2lp	1.0	0.5	1.0	1.0

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
ld2lp	8	d_to_q	tpLH	1.03	1.07	1.15	1.23	1.32
			tpHL	1.34	1.38	1.43	1.48	1.52
		d_to_qn	tpLH	1.51	1.56	1.64	1.72	1.80
			tpHL	1.21	1.24	1.30	1.35	1.39
		ld_to_q	tpLH	1.03	1.07	1.15	1.23	1.32
			tpHL	1.34	1.38	1.43	1.48	1.52
		ld_to_qn	tpLH	1.51	1.56	1.64	1.72	1.80
			tpHL	1.21	1.24	1.30	1.35	1.39
		ldn_to_q	tpLH	1.03	1.07	1.15	1.23	1.32
			tpHL	1.34	1.38	1.43	1.48	1.52
		ldn_to_qn	tpLH	1.51	1.56	1.64	1.72	1.80
			tpHL	1.21	1.24	1.30	1.35	1.39
		gn_to_q	tpLH	1.02	1.06	1.14	1.22	1.31
			tpHL	1.05	1.09	1.14	1.19	1.23
		gn_to_qn	tpLH	1.22	1.27	1.35	1.43	1.51
			tpHL	1.20	1.23	1.29	1.33	1.37

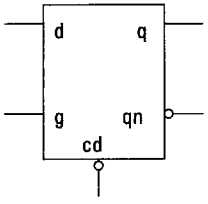
Timing Constraints:

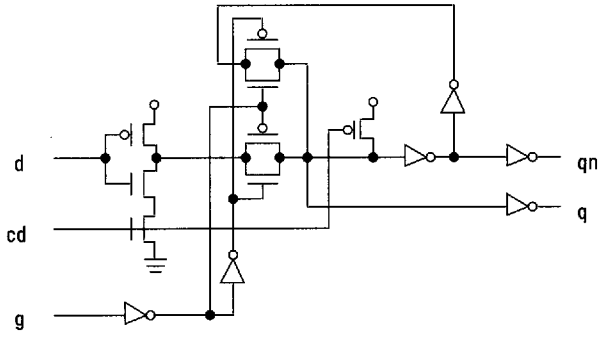
Version	*Parameters*	*Value*
ld2lp	d_setup	0.72
	d_hold	-0.01
	gn_pw0	0.43
	gn_pw1	0.43

Name: ld3 Description: D Latch with Clear Direct/Gate Active High

Coding Syntax: u(q,qn)=ld3*(d,g,cd)

Logic Symbol:l Schematics:





Truth Table:

d	*g*	*cd*	*q*	*qn*
0	1	1	0	1
1	1	1	1	0
x	0	1	q	qn
x	x	0	0	1

Loading Characteristics:

Values stated in standard loads.

Version	*d*	*g*	*cd*
ld3	1.0	1.0	0.9
ld3p	1.0	1.0	0.9

ld3
D Latch with Clear Direct/Gate Active High

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
ld3	5	d_to_q	tpLH	0.88	0.98	1.17	1.36	1.54
			tpHL	1.22	1.28	1.40	1.49	1.58
		d_to_qn	tpLH	1.38	1.46	1.62	1.79	1.97
			tpHL	1.07	1.12	1.21	1.30	1.38
		g_to_q	tpLH	0.86	0.95	1.15	1.33	1.52
			tpHL	0.80	0.86	0.98	1.07	1.16
		g_to_qn	tpLH	0.96	1.03	1.20	1.37	1.55
			tpHL	1.04	1.09	1.18	1.27	1.35
		cd_to_qn	tpLH	1.05	1.13	1.29	1.46	1.64
			tpHL	1.05	1.13	1.29	1.46	1.64
		cd_to_q	tpLH	0.89	0.96	1.07	1.17	1.26
			tpHL	0.89	0.96	1.07	1.17	1.26
ld3p	6	d_to_q	tpLH	0.90	0.95	1.04	1.14	1.24
			tpHL	1.22	1.26	1.33	1.39	1.45
		d_to_qn	tpLH	1.43	1.48	1.56	1.63	1.72
			tpHL	1.18	1.21	1.27	1.32	1.37
		g_to_q	tpLH	0.84	0.89	0.99	1.08	1.18
			tpHL	0.78	0.82	0.90	0.96	1.01
		g_to_qn	tpLH	1.00	1.04	1.12	1.20	1.28
			tpHL	1.12	1.16	1.21	1.26	1.31
		cd_to_qn	tpLH	1.12	1.17	1.25	1.33	1.41
			tpHL	1.12	1.17	1.25	1.33	1.41
		cd_to_q	tpLH	0.91	0.95	1.02	1.08	1.14
			tpHL	0.91	0.95	1.02	1.08	1.14

Timing Constraints:

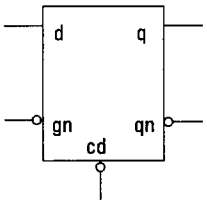
Version	*Parameters*	*Value*	*Version*	*Parameters*	*Value*
ld3	d_setup	0.66	ld3p	d_setup	0.77
	d_hold	0.17		d_hold	0.03
	g_pw	0.47		g_pw	0.54
	cd_rcvry	0.27		cd_rcvry	0.34
	cd_hold	0.20		cd_hold	0.20

Name: ld4

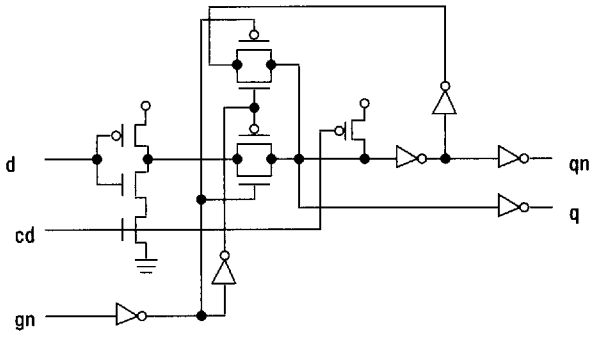
Description: D Latch with Clear Direct/Gate Active Low

Coding Syntax: u(q,qn)=ld4*(d,gn,cd)

Logic Symbol:



Schematics:



Truth Table:

d	*gn*	*cd*	*q*	*qn*
0	0	1	0	1
1	0	1	1	0
x	1	1	q	qn
x	x	0	0	1

Loading Characteristics:

Values stated in standard loads.

Version	*d*	*gn*	*cd*
ld4	1.0	0.5	0.9
ld4p	1.0	0.5	0.9

ld4

D Latch with Clear Direct/Gate Active Low

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
ld4	5	d_to_q	tpLH	0.89	0.98	1.18	1.36	1.55
			tpHL	1.22	1.28	1.39	1.49	1.58
		d_to_qn	tpLH	1.39	1.46	1.62	1.79	1.97
			tpHL	1.07	1.12	1.21	1.30	1.38
		gn_to_q	tpLH	0.89	0.98	1.18	1.36	1.55
			tpHL	0.80	0.87	0.98	1.07	1.17
		gn_to_qn	tpLH	0.97	1.05	1.21	1.38	1.56
			tpHL	1.07	1.12	1.21	1.30	1.38
		cd_to_qn	tpLH	1.05	1.13	1.29	1.46	1.64
			tpHL	1.05	1.13	1.29	1.46	1.64
		cd_to_q	tpLH	0.89	0.95	1.06	1.16	1.25
			tpHL	0.89	0.95	1.06	1.16	1.25
ld4p	6	d_to_q	tpLH	0.90	0.95	1.05	1.14	1.24
			tpHL	1.21	1.26	1.33	1.39	1.44
		d_to_qn	tpLH	1.44	1.48	1.56	1.64	1.72
			tpHL	1.18	1.21	1.27	1.32	1.37
		gn_to_q	tpLH	0.87	0.93	1.02	1.12	1.22
			tpHL	0.79	0.84	0.91	0.97	1.02
		gn_to_qn	tpLH	1.01	1.06	1.14	1.22	1.30
			tpHL	1.15	1.19	1.24	1.29	1.34
		cd_to_qn	tpLH	1.13	1.17	1.25	1.33	1.41
			tpHL	1.13	1.17	1.25	1.33	1.41
		cd_to_q	tpLH	0.90	0.95	1.02	1.08	1.13
			tpHL	0.90	0.95	1.02	1.08	1.13

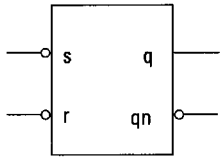
Timing Constraints:

Version	*Parameters*	*Value*	*Version*	*Parameters*	*Value*
ld4	d_setup	0.84	ld4p	d_setup	0.94
	d_hold	-0.00		d_hold	-0.13
	gn_pw0	0.75		gn_pw0	0.78
	gn_pw1	0.75		gn_pw1	0.78
	cd_rcvry	0.55		cd_rcvry	0.58
	cd_hold	0.20		cd_hold	0.20

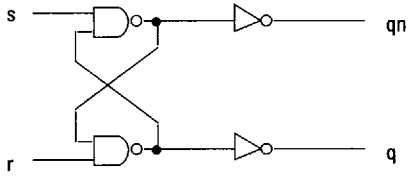
Name: lsr0 Description: SR Latch

Coding Syntax: u(q,qn)=lsr0*(s,r)

Logic Symbol:



Schematics:



Truth Table:

s	*r*	*q*	*qn*
0	0	0	0
0	1	1	0
1	0	0	1
1	1	q	qn

Loading Characteristics:

Values stated in standard loads.

Version	*s*	*r*
lsr0	0.9	0.9
lsr0p	0.9	0.9

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
lsr0	3	s_to_q	tpLH	0.93	1.01	1.18	1.35	1.53
			tpHL	0.93	1.01	1.18	1.35	1.53
		r_to_qn	tpLH	0.93	1.01	1.18	1.35	1.53
			tpHL	0.93	1.01	1.18	1.35	1.53
		r_to_q	tpLH	0.77	0.85	1.01	1.18	1.36
			tpHL	0.62	0.69	0.79	0.88	0.97
		s_to_qn	tpLH	0.81	0.89	1.05	1.22	1.40
			tpHL	0.65	0.71	0.82	0.92	1.01

AC Characteristics: (Cont.)

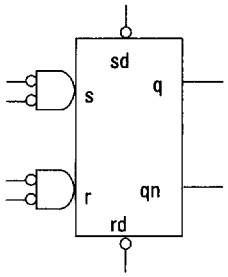
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

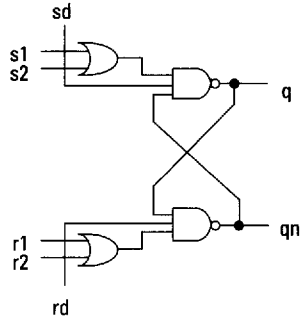
Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
lsr0p	4	s_to_q	tpLH	1.02	1.07	1.16	1.24	1.33
			tpHL	1.02	1.07	1.16	1.24	1.33
		r_to_qn	tpLH	1.02	1.07	1.16	1.24	1.33
			tpHL	1.02	1.07	1.16	1.24	1.33
		r_to_q	tpLH	0.77	0.82	0.90	0.98	1.07
			tpHL	0.65	0.69	0.76	0.82	0.87
		s_to_qn	tpLH	0.80	0.85	0.94	1.02	1.11
			tpHL	0.67	0.71	0.79	0.85	0.90

Name: lsr1 Description: SR Latch with Clear, Set, Separate Gated Inputs

Coding Syntax: u (q,qn) = lsr1 (s1,s2,sd,r1,r2,rd)

Logic Symbol: Schematics:





Truth Table:

s1,s2	*r1,r2*	*sd*	*rd*	*q*	*qn*
x	x	0	1	1	0
x	x	1	0	0	1
x	x	0	0	1	1
1	1	1	1	q	qn
1	0	1	1	0	1
0	1	1	1	1	0
0	0	1	1	1	1

Loading Characteristics:

Values stated in standard loads.

Version	*s1*	*s2*	*sd*	*r1*	*r2*	*rd*
lsr1	0.9	0.8	0.9	0.9	0.8	0.9

SR Latch with Clear, Set, Separate Gated Inputs

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

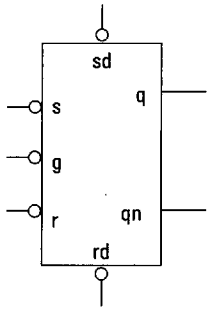
Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
lsr1	4	s1_to_q	tpLH	0.88	1.07	1.38	1.64	1.92
			tpHL	0.79	0.96	1.26	1.53	1.78
		s2_to_q	tpLH	0.88	1.07	1.38	1.64	1.92
			tpHL	0.79	0.96	1.26	1.53	1.78
		r1_to_qn	tpLH	0.88	1.07	1.38	1.64	1.92
			tpHL	0.79	0.96	1.26	1.53	1.78
		r2_to_qn	tpLH	0.88	1.07	1.38	1.64	1.92
			tpHL	0.79	0.96	1.26	1.53	1.78
		sd_to_q	tpLH	0.69	0.87	1.18	1.44	1.72
			tpHL	0.79	0.96	1.26	1.53	1.78
		rd_to_qn	tpLH	0.69	0.87	1.18	1.44	1.72
			tpHL	0.79	0.96	1.26	1.53	1.78

Name: lsr2

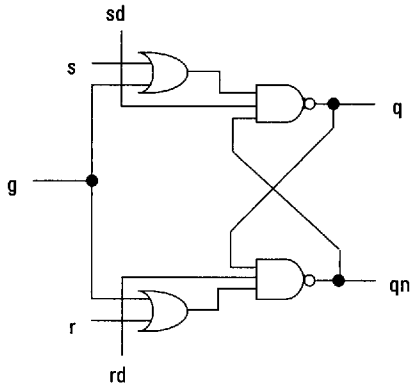
Description: SR Latch with Clear, Set, Common Gated Inputs

Coding Syntax: u(q,qn)=lsr2(s,r,g,sd,rd)

Logic Symbol:



Schematics:



Truth Table:

s	*r*	*g*	*sd*	*rd*	*q*	*qn*
x	x	x	0	1	1	0
x	x	x	1	0	0	1
x	x	x	0	0	1	1
x	x	1	1	1	q	qn
1	1	0	1	1	q	qn
1	0	0	1	1	0	1
0	1	0	1	1	1	0
0	0	0	1	1	1	1

Loading Characteristics:

Values stated in standard loads.

Version	*s*	*r*	*g*	*sd*	*rd*
lsr2	0.8	0.8	1.8	0.9	0.9

lsr2

SR Latch with Clear, Set, Common Gated Inputs

AC Characteristics:

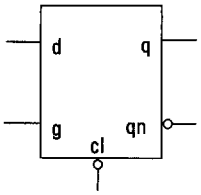
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

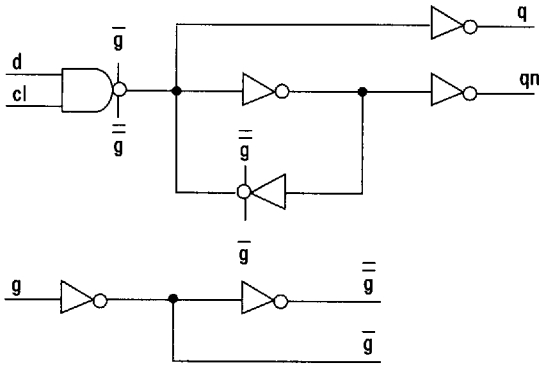
Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
lsr2	4	g_to_q	tpLH	1.42	1.61	1.91	2.17	2.41
			tpHL	0.81	0.98	1.29	1.56	1.80
		sd_to_q	tpLH	0.68	0.87	1.17	1.43	1.67
			tpHL	0.81	0.98	1.29	1.56	1.80
		rd_to_qn	tpLH	0.68	0.87	1.17	1.43	1.67
			tpHL	0.81	0.98	1.29	1.56	1.80
		s_to_q	tpLH	1.42	1.61	1.91	2.17	2.41
			tpHL	0.81	0.98	1.29	1.56	1.80
		r_to_qn	tpLH	1.35	1.53	1.84	2.10	2.33
			tpHL	0.81	0.98	1.29	1.56	1.80

Name: sld3 Description: D Latch with Synchronous Clear

Coding Syntax: u(q,qn)=sld3(d,g,cl)

Logic Symbol: Schematics:





Truth Table:

d	*g*	*cl*	*q*	*qn*
0	1	1	0	1
1	1	1	1	0
x	0	x	q	qn
x	1	0	0	1

Loading Characteristics:

Values stated in standard loads.

Version	*d*	*g*	*cl*
sld3	1.0	1.0	1.0

sld3
D Latch with Synchronous Clear

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
sld3	5	g_to_q	tpLH	0.96	1.05	1.24	1.42	1.61
			tpHL	0.88	0.95	1.07	1.18	1.29
		g_to_qn	tpLH	1.05	1.12	1.29	1.45	1.64
			tpHL	1.08	1.13	1.22	1.30	1.39
		d_to_q	tpLH	0.95	1.04	1.22	1.40	1.59
			tpHL	0.90	0.97	1.10	1.21	1.31
		d_to_qn	tpLH	1.07	1.15	1.31	1.48	1.66
			tpHL	1.07	1.12	1.21	1.29	1.37
		cl_to_q	tpLH	0.95	1.04	1.22	1.40	1.59
			tpHL	0.90	0.97	1.10	1.21	1.31
		cl_to_qn	tpLH	1.07	1.15	1.31	1.48	1.66
			tpHL	1.07	1.12	1.21	1.29	1.37

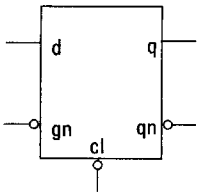
Timing Constraints:

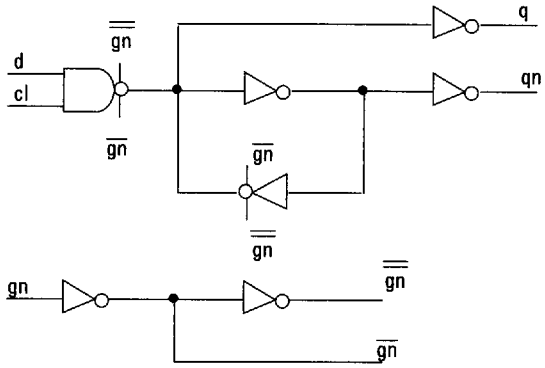
Version	*Parameters*	*Value*
sld3	d_setup	0.64
	d_hold	0.04
	cl_setup	0.64
	cl_hold	0.04
	g_pw0	0.64
	g_pw1	0.64

Name: sld4 Description: D Latch with Active Low Gate and Synchronous Clear

Coding Syntax: u(q,qn)=sld4(d,gn,cl)

Logic Symbol: Schematics:





Truth Table:

d	*g*	*cl*	*q*	*qn*
0	0	1	0	1
1	0	1	1	0
x	1	x	q	qn
x	0	0	0	1

Loading Characteristics:

Values stated in standard loads.

Version	*d*	*gn*	*cl*
sld4	1.0	0.5	1.0

sld4

D Latch with Active Low Gate and Synchronous Clear

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
sld4	5	gn_to_q	tpLH	0.93	1.02	1.21	1.39	1.58
			tpHL	0.93	1.00	1.13	1.24	1.34
		gn_to_qn	tpLH	1.10	1.18	1.34	1.51	1.69
			tpHL	1.05	1.11	1.19	1.28	1.36
		cl_to_q	tpLH	0.95	1.04	1.22	1.41	1.59
			tpHL	0.90	0.97	1.10	1.21	1.31
		cl_to_qn	tpLH	1.07	1.15	1.31	1.48	1.66
			tpHL	1.06	1.12	1.21	1.29	1.37
		d_to_q	tpLH	0.95	1.04	1.22	1.41	1.59
			tpHL	0.90	0.97	1.10	1.21	1.31
		d_to_qn	tpLH	1.07	1.15	1.31	1.48	1.66
			tpHL	1.06	1.12	1.21	1.29	1.37

Timing Constraints:

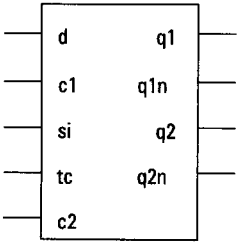
Version	*Parameters*	*Value*
sld4	d_setup	0.55
	d_hold	0.07
	cl_setup	0.55
	cl_hold	0.07
	gn_pw0	0.57
	gn_pw1	0.57

Name: srlc1

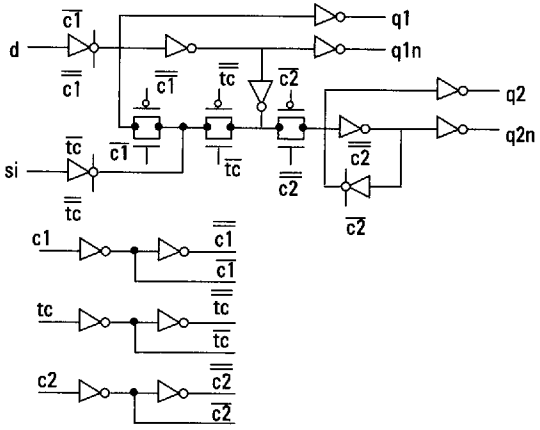
Description: D Latch into D Latch with Scan Input

Coding Syntax: U(q1,q1n,q2,q2n)=srlc1*(d,c1,si,tc,c2)

Logic Symbol:



Schematics:



Truth Table:

c1	*tc*	*c2*	*q1*	*q1n*	*q2*	*q2n*
1	0	0	d	$\overline{d}$	q2	q2n
0	1	0	si	$\overline{si}$	q2	q2n
0	0	1	q1	q1n	q1	q1n

Loading Characteristics:

Values stated in standard loads.

Version	*d*	*c1*	*si*	*tc*	*c2*
srlc1	1.0	1.0	1.0	1.0	1.0
srlc1p	1.0	1.0	1.0	1.0	1.0

srlc1
D Latch into D Latch with Scan Input

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
srlc1	11	c1_to_q1	tpLH	0.97	1.07	1.25	1.44	1.62
			tpHL	0.95	1.02	1.16	1.28	1.39
		c1_to_q1n	tpLH	1.10	1.18	1.35	1.52	1.69
			tpHL	1.09	1.14	1.23	1.31	1.39
		c1_to_q2	tpLH	1.47	1.55	1.72	1.90	2.08
			tpHL	1.50	1.56	1.68	1.78	1.88
		c1_to_q2n	tpLH	1.68	1.76	1.92	2.09	2.27
			tpHL	1.58	1.63	1.72	1.80	1.88
		d_to_q1	tpLH	0.82	0.92	1.11	1.29	1.48
			tpHL	0.89	0.96	1.10	1.22	1.33
		d_to_q1n	tpLH	1.05	1.13	1.29	1.46	1.64
			tpHL	0.95	0.99	1.08	1.17	1.25
		d_to_q2	tpLH	1.32	1.41	1.58	1.75	1.93
			tpHL	1.44	1.50	1.62	1.72	1.82
		d_to_q2n	tpLH	1.63	1.70	1.87	2.04	2.21
			tpHL	1.44	1.49	1.58	1.66	1.74
		si_to_q1	tpLH	1.08	1.18	1.37	1.55	1.74
			tpHL	1.14	1.21	1.35	1.47	1.58
		si_to_q1n	tpLH	1.30	1.38	1.54	1.71	1.89
			tpHL	1.21	1.25	1.34	1.42	1.51
		si_to_q2	tpLH	1.58	1.67	1.84	2.01	2.19
			tpHL	1.69	1.75	1.87	1.98	2.07
		si_to_q2n	tpLH	1.88	1.95	2.12	2.29	2.47
			tpHL	1.70	1.75	1.84	1.92	2.00
		tc_to_q1	tpLH	1.20	1.29	1.48	1.67	1.85
			tpHL	1.17	1.24	1.38	1.50	1.61
		tc_to_q1n	tpLH	1.33	1.41	1.57	1.74	1.92
			tpHL	1.32	1.36	1.45	1.54	1.62
		tc_to_q2	tpLH	1.69	1.78	1.95	2.12	2.30
			tpHL	1.72	1.78	1.90	2.01	2.10
		tc_to_q2n	tpLH	1.91	1.98	2.15	2.32	2.50
			tpHL	1.81	1.86	1.95	2.03	2.11
		c2_to_q2	tpLH	0.89	0.97	1.14	1.32	1.50
			tpHL	0.79	0.84	0.96	1.07	1.17
		c2_to_q2n	tpLH	0.97	1.05	1.21	1.38	1.56
			tpHL	1.01	1.06	1.14	1.23	1.31

AC Characteristics: (Cont.)

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*Gate Count*	*Delay Path*	*Output*	*Standard Loads*				
				2	*4*	*8*	*12*	*16*
srlc1p	13	c1_to_q1	tpLH	0.95	1.00	1.08	1.17	1.26
			tpHL	0.96	1.01	1.10	1.18	1.25
		c1_to_q1n	tpLH	1.21	1.25	1.34	1.42	1.50
			tpHL	1.14	1.18	1.23	1.28	1.33
		c1_to_q2	tpLH	1.56	1.60	1.70	1.78	1.87
			tpHL	1.67	1.71	1.78	1.84	1.90
		c1_to_q2n	tpLH	1.87	1.91	1.99	2.07	2.16
			tpHL	1.75	1.78	1.83	1.88	1.93
		d_to_q1	tpLH	0.89	0.94	1.03	1.11	1.20
			tpHL	0.89	0.94	1.04	1.11	1.19
		d_to_q1n	tpLH	1.14	1.19	1.27	1.35	1.43
			tpHL	1.08	1.12	1.18	1.22	1.27
		d_to_q2	tpLH	1.50	1.54	1.64	1.72	1.81
			tpHL	1.60	1.64	1.71	1.77	1.83
		d_to_q2n	tpLH	1.80	1.84	1.92	2.01	2.09
			tpHL	1.69	1.72	1.77	1.82	1.88
		si_to_q1	tpLH	1.16	1.21	1.30	1.38	1.47
			tpHL	1.14	1.19	1.28	1.36	1.43
		si_to_q1n	tpLH	1.39	1.43	1.51	1.60	1.68
			tpHL	1.35	1.39	1.45	1.49	1.54
		si_to_q2	tpLH	1.77	1.81	1.91	1.99	2.08
			tpHL	1.85	1.89	1.96	2.01	2.08
		si_to_q2n	tpLH	2.05	2.09	2.17	2.25	2.34
			tpHL	1.96	1.99	2.04	2.09	2.15
		tc_to_q1	tpLH	1.15	1.20	1.29	1.38	1.46
			tpHL	1.17	1.22	1.31	1.39	1.46
		tc_to_q1n	tpLH	1.41	1.46	1.54	1.62	1.70
			tpHL	1.35	1.38	1.44	1.49	1.53
		tc_to_q2	tpLH	1.77	1.81	1.90	1.99	2.07
			tpHL	1.87	1.92	1.98	2.04	2.10
		tc_to_q2n	tpLH	2.07	2.12	2.20	2.28	2.36
			tpHL	1.95	1.98	2.04	2.09	2.14
		c2_to_q2	tpLH	0.99	1.03	1.13	1.21	1.30
			tpHL	0.80	0.84	0.91	0.97	1.03
		c2_to_q2n	tpLH	1.00	1.04	1.12	1.20	1.29
			tpHL	1.18	1.21	1.27	1.31	1.37

srlc1

D Latch into D Latch with Scan Input

Timing Constraints:

Version	*Parameters*	*Value*	*Version*	*Parameters*	*Value*
srlc1	d_c1_setup	0.64	srlc1p	d_c1_setup	0.84
	d_c1_hold	0.10		d_c1_hold	-0.16
	d_c2_setup	1.07		d_c2_setup	1.07
	d_c2_hold	-0.20		d_c2_hold	-0.15
	si_setup	0.73		si_setup	0.86
	si_hold	0.00		si_hold	-0.17
	c1_pw	0.65		c1_pw	0.68
	tc_pw	0.65		tc_pw	0.68
	c2_pw	0.65		c2_pw	0.63

2.5 Internal Clock Buffers

This section contains data pages for the LCA300K internal clock buffers.

Naming Conventions

Internal clock buffer names have the following format:

root_name | ***input_voltage_level_option*** | ***drive_strength*** | ***internal_buffer_flag***

Table 2.1 shows the naming conventions used for internal clock buffers.

Table 2.1 Internal Clock Buffer Naming Conventions

Root Name	*Input Voltage Level Options*	*Drive Strength in mA*	*Internal Buffer Flag*
clk	t = TTL	2 (maximum loading $\leq$ 250)	i
	c = CMOS	4 (maximum loading $\leq$ 500)	
		8 (maximum loading $\leq$ 1,500)	
		16 (maximum loading $\leq$ 2,000)	

For example, `clkt2i` is a 2 mA internal clock buffer with TTL input.

➤ ***Note:*** For the coding syntax, an asterisk following the cell name is a wild-card symbol that replaces the drive strength values.

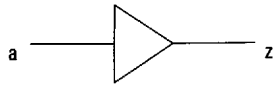
clkc
Internal Clock Buffer

Name: clkc

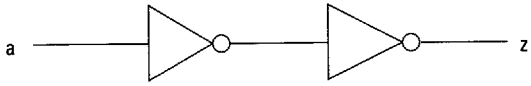
Description: Internal Clock Buffer

Coding Syntax: z=clkc*i(a)

Logic Symbol:



Schematics:



Truth Table:

a	*z*
0	0
1	1

Loading Characteristics:

Values stated in standard loads.

Version	*a*
clkc2i	2.1
clkc4i	2.1
clkc8i	2.1
clkc12i	2.1
clkc16i	2.1

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*I/O Slots*	*Delay Path*	*Output*	*Standard Loads*					
				100	*150*	*200*	*300*	*400*	*600*
clkc2i	2	a_to_z	tpLH	0.88	1.02	1.16	1.45	1.74	2.32
			tpHL	0.92	1.14	1.37	1.82	2.27	3.18
Version	*I/O Slots*	*Delay Path*	*Output*	*Standard Loads*					
				150	*200*	*300*	*400*	*600*	*800*
clkc4i	2	a_to_z	tpLH	0.82	0.92	1.03	1.24	1.45	1.88
			tpHL	0.81	0.98	1.15	1.49	1.82	2.50
Version	*I/O Slots*	*Delay Path*	*Output*	*Standard Loads*					
				200	*300*	*400*	*600*	*800*	*1000*
clkc8i	2	a_to_z	tpLH	0.87	1.21	1.56	1.80	2.16	2.52
			tpHL	0.85	1.36	1.87	2.21	2.72	3.22

AC Characteristics: (Cont.)

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*I/O Slots*	*Delay Path*	*Output*	*Standard Loads*					
				400	***600***	***800***	***1000***	***1200***	***1600***
clkc12i	2	a_to_z	tpLH	1.09	1.30	1.51	1.73	1.95	2.38
			tpHL	1.23	1.57	1.90	2.24	2.58	3.26
Version	*I/O Slots*	*Delay Path*	*Output*	*Standard Loads*					
				400	***600***	***800***	***1200***	***1600***	***2000***
clkc16i	2	a_to_z	tpLH	1.01	1.10	1.29	1.57	1.85	2.23
			tpHL	1.10	1.26	1.57	2.03	2.49	3.10

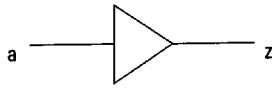
clkt
Internal Clock Buffer

Name: clkt

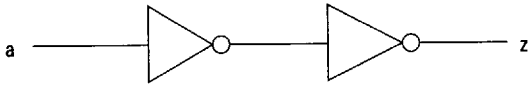
Description: Internal Clock Buffer

Coding Syntax: z=clkt*i(a)

Logic Symbol:



Schematics:



Truth Table:

a	*z*
0	0
1	1

Loading Characteristics:

Values stated in standard loads.

Version	*a*
clkt2i	2.0
clkt4i	2.0
clkt8i	2.0
clkt12i	2.0
clkt16i	2.0

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*I/O Slots*	*Delay Path*	*Output*	*Standard Loads*					
				100	*150*	*200*	*300*	*400*	*600*
clkt2i	2	a_to_z	tpLH	0.90	1.04	1.18	1.47	1.75	2.34
			tpHL	1.01	1.24	1.46	1.91	2.36	3.27
Version	*I/O Slots*	*Delay Path*	*Output*	*Standard Loads*					
				150	*200*	*300*	*400*	*600*	*800*
clkt4i	2	a_to_z	tpLH	0.86	0.97	1.07	1.28	1.49	1.93
			tpHL	0.90	1.07	1.25	1.58	1.92	2.59
Version	*I/O Slots*	*Delay Path*	*Output*	*Standard Loads*					
				200	*300*	*400*	*600*	*800*	*1000*
clkt8i	2	a_to_z	tpLH	0.92	1.26	1.61	1.85	2.21	2.57
			tpHL	0.95	1.46	1.97	2.30	2.81	3.32

AC Characteristics: (Cont.)

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal.
Values stated in nanoseconds. Ramp time=0.2 ns (measured from 10% to 90% VDD).

Version	*I/O Slots*	*Delay Path*	*Output*	*Standard Loads*					
				400	***600***	***800***	***1000***	***1200***	***1600***
clkt12i	2	a_to_z	tpLH	1.15	1.35	1.57	1.79	2.01	2.45
			tpHL	1.32	1.66	2.00	2.34	2.68	3.35
Version	***I/O Slots***	***Delay Path***	***Output***	***Standard Loads***					
				400	***600***	***800***	***1200***	***1600***	***2000***
clkt16i	2	a_to_z	tpLH	1.07	1.16	1.35	1.63	1.91	2.29
			tpHL	1.20	1.36	1.67	2.13	2.58	3.20

Chapter 3
5 V and 3.3 V I/O Macrocells

3.1 Introduction

The I/O 300K library, companion to the LCA300K technology library, contains:

- 5 V CMOS, TTL, and Schmitt trigger input macrocells
- 3.3 V I/Os (TTL-compatible buffers)

These I/O macrocells allow the designer to bridge the gap between current and future systems. Requirements for increasingly complex, bus-oriented system design have raised gate and pin counts and increased system clock rates. This trend increases switching noise in buses and increases the total power dissipation by the outputs of an ASIC. The IEEE has standardized a 3.3 V supply voltage, which results in lower power dissipation and less output noise than does a 5 V supply voltage. Designs can now accept and provide 3.3 V signals with fully characterized cells, in compliance with TTL specifications.

Delay data information given for 5 V TTL input buffers in this chapter may be used for 3.3 V applications. Special 3.3 V output and bidirectional buffers may be used to drive a 3.3 V signal.

Nomenclature and delays of 3.3 V output buffers are different from those of corresponding 5 V buffers. The names of 5 V buffers have no suffix; the names of corresponding 3.3 V I/Os are suffixed by a lowercase L (l), to indicate low voltage.

Although slew rate control with 5 V operation may be used to reduce noise levels, 3.3 V buffers provide this benefit with less propagation delay.

The 3.3 V cells are integrated into LSI Logic's C-MDE software.

3.2 Power Dissipation

Overall power dissipation of an ASIC may be reduced by using 3.3 V buffers.

The most important factor in calculating power dissipation is the charging and discharging of capacitance during circuit switching. The charging of capacitor C to a voltage V through a P-channel device builds up a charge CV and stores energy 1/2 CV^2. This energy is later discharged through an N-channel transistor in a CMOS P-N pair. When such switching takes place at a frequency f, the resulting power dissipated in the CMOS circuit is equivalent to $P = fCV^2(1/2)$. This AC power dissipation usually contributes more than 95% of the total power dissipated in CMOS circuits. For equivalent C and f, power dissipation of the outputs is decreased by 56.44% through the use of a 3.3 V instead of a 5 V buffer.

3.3 Power Ring Structures and Power Rules

In addition to the three ground buses (VSS, VSS2, and VSS3), and the two power buses (VDD and VDD2), designs using 3.3 V buffers need an additional 3.3 V power bus, VDD4, for external output drivers.

The power ring structures for 5 V and 3.3 V operation are shown in Figure 3.1 ("Internal Power and Ground Ring Structure Using 5 V Power Supply for 5 V Output Buffers") and Figure 3.2 ("Internal Power and Ground Ring Structure Using 3.3 V Power Supply for 3.3 V Output Buffers"), respectively.

If a 3.3 V buffer is used, the VDD4 power segment is created within the VDD power ring during the layout stage of the design. 3.3 V operation may be chosen for any or all outputs.

VDD4 uses the same power and ground rules described for VDD and VSS in Chapter 1. Every VDD4 pad supports up to 16 standard output buffers (a standard output buffer is a 4 mA buffer). In the case of simultaneous switching, each VDD4 pad supports up to 10 standard output buffers. Each VDD4 segment must have at least one VDD4 pad.

LSI Logic's 3.3 V design methodology maximizes the available I/O buffers for any design. Designs using VDD4 as a separate 3.3 V power bus for external 3.3 V output drivers are 25% to 30% smaller and 10% to15% faster than designs using a 5 V power bus.

Figure 3.1
Internal Power and Ground Ring Structure Using 5 V Power Supply for 5 V Outputs

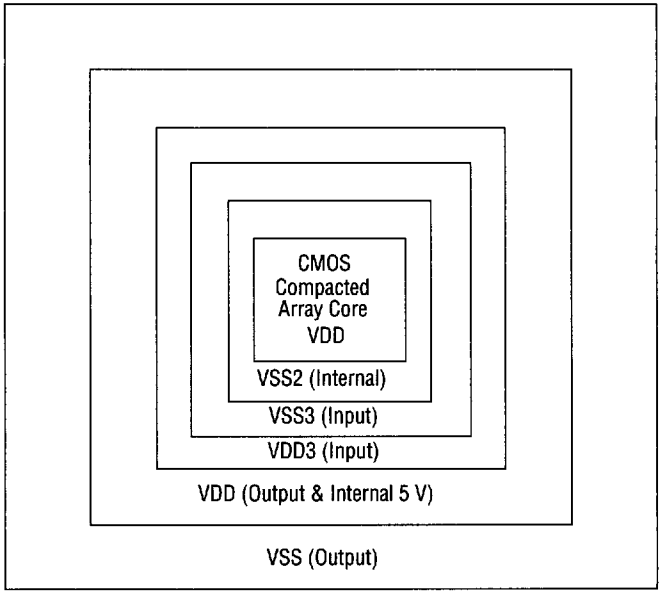
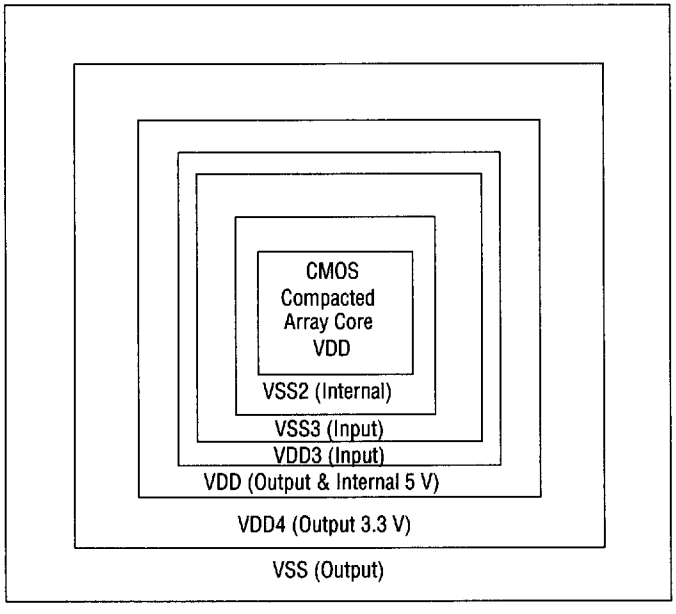


Figure 3.2
Internal Power and Ground Ring Structure Using 3.3 V Power Supply for 3.3 V Outputs



3.4 Organization

The remainder of this chapter is organized into the following sections:

- Input Clock Drivers
- Input Buffers
- Unidirect Output Buffers
- Bidirect Output Buffers
- 3-State Output Buffers
- Oscillators
- Commercial Output Buffers
- 3.3 V I/Os

Naming conventions for different macrocell types are given at the beginning of each section.

3.5 Input Clock Drivers

This section contains data pages for LCA300K input clock drivers.

Naming Conventions

Input clock driver names have the following format:

root_name | input_voltage_level_option | drive_strength | resistor (optional)

Table 3.1 shows the naming conventions used for input clock drivers.

Table 3.1 Input Clock Driver Naming Conventions

Root Name[1]	*Input Voltage Level Options*	*Drive Strength in mA*	*Optional Resistors*
drv	t = TTL	2 (maximum loading ≤ 250)	u = pull-up
	c = CMOS	4 (maximum loading ≤ 500)	d = pull-down
	sc = Schmitt trigger for CMOS	8 (maximum loading ≤ 1,000)	
		16 (maximum loading ≤ 2,000)	

1. The prefix d (direct) is used only for the direct input clock driver, `ddrv`.

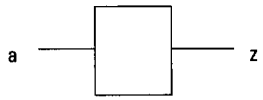
For example, `drvc2u` is an input clock driver with CMOS input, a 2 mA drive strength, and a pull-up resistor.

➤ ***Note:*** For the coding syntax, an asterisk following the cell name (for example, `drvc*`) is a wildcard symbol that replaces options' abbreviations and drive strength values.

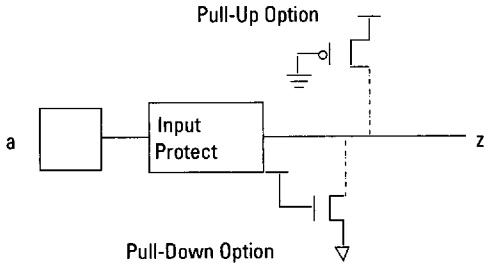
Name: ddrv Description: Direct Input Clock Driver

Coding Syntax: z=&ddrv*(a)

Logic Symbol:



Schematics:



Loading Characteristics: Not Applicable

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/O Slots*	*Pads*	*Delay Path*	*Output*	*Standard Loads*						*Slope*	*Incpt*
					50	*100*	*200*	*300*	*400*	*500*		
ddrv	1	1	a_to_z	tpLH	0.00	0.00	0.00	0.00	0.00	0.00	0.0000	0.0000
				tpHL	0.00	0.00	0.00	0.00	0.00	0.00	0.0000	0.0000

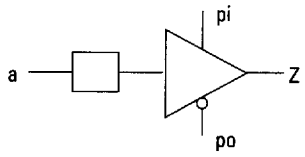
drvc
Clock Driver with CMOS Input

Name: drvc

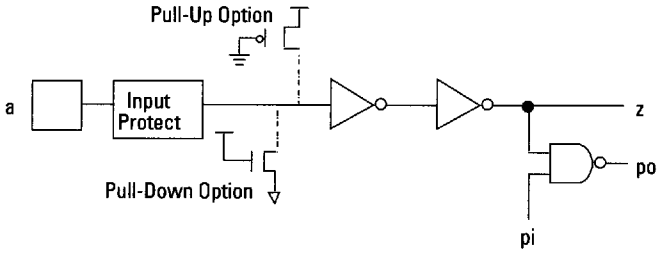
Description: Clock Driver with CMOS Input

Coding Syntax: u(z,po)=&drvc*(a,pi)

Logic Symbol:



Schematics:



Truth Table:

a	*pi*	*z*	*po*
0	x	0	1
1	0	1	1
1	1	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*pi*
drvc2	0.5
drvc4	0.5
drvc8	0.5
drvc12	0.5
drvc16	0.5

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*Slots*	*Pads*	*Delay Path*	*Output*	*Standard Loads*						*Slope*	*Incpt*
					50	*100*	*200*	*300*	*400*	*500*		
drvc2	2	1	a_to_z	tpLH	1.07	1.25	1.62	1.98	2.34	2.71	0.0036	0.8900
				tpHL	0.90	1.09	1.49	1.88	2.27	2.67	0.0039	0.7000
drvc4	2	1	a_to_z	tpLH	1.03	1.16	1.43	1.70	1.97	2.24	0.0027	0.8900
				tpHL	0.87	1.01	1.30	1.60	1.89	2.18	0.0029	0.7200
drvc8	2	1	a_to_z	tpLH	1.02	1.12	1.31	1.51	1.71	1.91	0.0020	0.9200
				tpHL	0.86	0.95	1.15	1.34	1.54	1.73	0.0019	0.7600
drvc12	2	1	a_to_z	tpLH	1.05	1.12	1.25	1.39	1.53	1.66	0.0014	0.9800
				tpHL	0.87	0.95	1.09	1.24	1.38	1.53	0.0015	0.8000
drvc16	2	1	a_to_z	tpLH	1.07	1.11	1.21	1.30	1.40	1.49	0.0009	1.0200
				tpHL	0.91	0.97	1.08	1.19	1.29	1.40	0.0011	0.8600

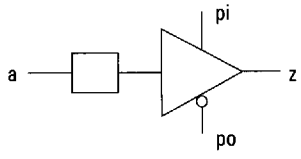
Name: drvsc

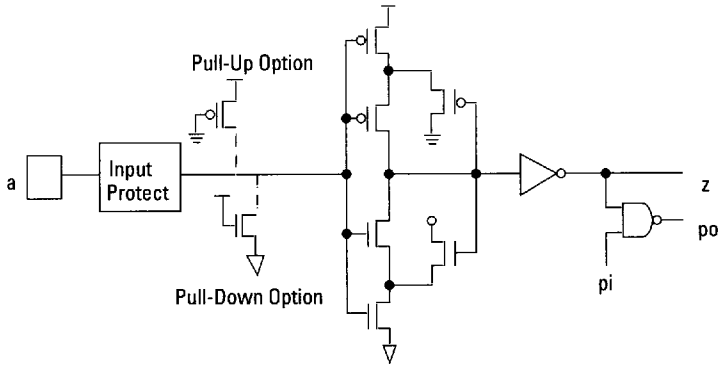
Description: Clock Driver with CMOS Schmitt Trigger Input

Coding Syntax: u(z,po)=&drvsc*(a,pi)

Logic Symbol:

Schematics:





Truth Table:

a	*pi*	*z*	*po*
0	x	0	1
1	0	1	1
1	1	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*pi*
drvsc2	0.5
drvsc4	0.5
drvsc8	0.5
drvsc12	0.5
drvsc16	0.5

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/O Slots*	*Pads*	*Delay Path*	*Output*	*Standard Loads*						*Slope*	*Incpt*
					50	*100*	*200*	*300*	*400*	*500*		
drvsc2	2	1	a_to_z	tpLH	1.67	1.85	2.22	2.58	2.94	3.31	0.0036	1.4900
				tpHL	1.83	2.02	2.42	2.81	3.20	3.60	0.0039	1.6300
drvsc4	2	1	a_to_z	tpLH	1.67	1.80	2.07	2.34	2.61	2.88	0.0027	1.5300
				tpHL	1.80	1.94	2.23	2.53	2.82	3.11	0.0029	1.6500
drvsc8	2	1	a_to_z	tpLH	1.67	1.77	1.96	2.16	2.36	2.56	0.0020	1.5700
				tpHL	1.80	1.89	2.09	2.28	2.48	2.67	0.0019	1.7000

drvsc

Clock Driver with CMOS Schmitt Trigger Input

AC Characteristics: (Cont.)

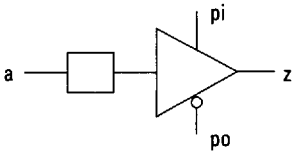
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

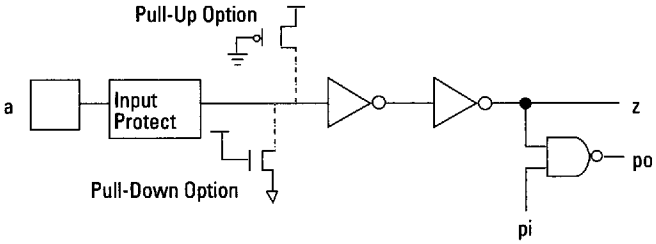
Version	*I/O Slots*	*Pads*	*Delay Path*	*Output*	*Standard Loads*						*Slope*	*Incpt*
					50	*100*	*200*	*300*	*400*	*500*		
drvsc12	2	1	a_to_z	tpLH	1.73	1.79	1.93	2.06	2.20	2.33	0.0013	1.6600
				tpHL	1.80	1.88	2.02	2.17	2.31	2.46	0.0015	1.7300
drvsc16	2	1	a_to_z	tpLH	1.72	1.76	1.86	1.95	2.05	2.14	0.0009	1.6700
				tpHL	1.90	1.95	2.06	2.16	2.27	2.37	0.0010	1.8500

Name: drvt Description: Clock Driver with TTL Input

Coding Syntax: u(z,po)=&drvt*(a,pi)

Logic Symbol: Schematics:





Truth Table:

a	*pi*	*z*	*po*
0	x	0	1
1	0	1	1
1	1	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*pi*
drvt2	0.5
drvt4	0.5
drvt8	0.5
drvt12	0.5
drvt16	0.5

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/O Slots*	*Pads*	*Delay Path*	*Output*	*Standard Loads*						*Slope*	*Incpt*
					50	*100*	*200*	*300*	*400*	*500*		
drvt2	2	1	a_to_z	tpLH	1.11	1.29	1.66	2.02	2.38	2.75	0.0036	0.9300
				tpHL	0.90	1.09	1.49	1.88	2.27	2.67	0.0039	0.7000
drvt4	2	1	a_to_z	tpLH	1.11	1.24	1.51	1.78	2.05	2.32	0.0027	0.9700
				tpHL	0.87	1.01	1.30	1.60	1.89	2.18	0.0029	0.7200
drvt8	2	1	a_to_z	tpLH	1.10	1.20	1.39	1.59	1.79	1.99	0.0020	1.0000
				tpHL	0.86	0.95	1.15	1.34	1.54	1.73	0.0019	0.7600
drvt12	2	1	a_to_z	tpLH	1.18	1.24	1.38	1.51	1.65	1.78	0.0013	1.1100
				tpHL	0.87	0.95	1.09	1.24	1.38	1.53	0.0015	0.8000
drvt16	2	1	a_to_z	tpLH	1.16	1.20	1.30	1.39	1.49	1.58	0.0009	1.1100
				tpHL	0.96	1.01	1.12	1.22	1.33	1.43	0.0010	0.9100

3.6 Input Buffers

This section contains data pages for the LCA300K input buffers.

Naming Conventions

Input buffer names have the following format:

root_name | ***input_voltage_level_option*** | ***resistor (optional)***

Table 3.2 shows the naming conventions used for input buffers.

Table 3.2 Input Buffer Naming Conventions

Root Name	*Input Voltage Level Options*	*Optional Resistors*
ibuf[1]	t = TTL	u = pull-up
schmit	tn = inverted TTL	d = pull-down
tlch[2]	c = CMOS	
	cn = inverted CMOS	

1. *CMOS voltage level option only. Macrocell names are* `ibuf` *for non-inverting,* `ibufn` *for inverting.*
2. *TTL voltage level option only. Macrocell names are* `tlcht` *for non-inverting,* `tlchn` *for inverting.*

For example, `schmitcnd` is an inverted Schmitt trigger with CMOS input and a pull-down resistor.

➤ ***Note:*** For the coding syntax, an asterisk following the cell name (for example, `ibuf*`) is a wildcard symbol that replaces options' abbreviations.

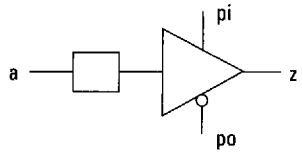
ibuf
CMOS Input Buffer

Name: ibuf

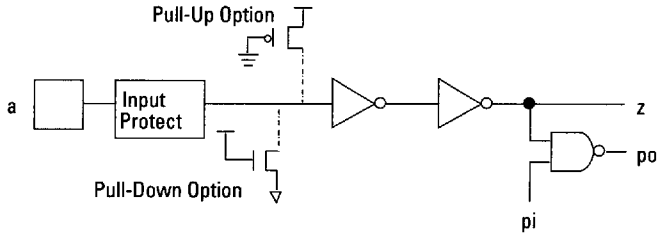
Description: CMOS Input Buffer

Coding Syntax: u(z,po)=&ibuf*(a,pi)

Logic Symbol:



Schematics:



Truth Table:

a	*pi*	*z*	*po*
0	x	0	1
1	0	1	1
1	1	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*pi*
ibuf	0.5

Pin A Input Capacitance: Device(1.7 pF) + pad(0.8 pF) = 2.5 pF

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

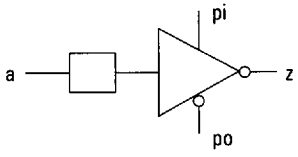
Version	*I/O Slots*	*Pads*	*Delay Path*	*Output*	*Standard Loads*					*Slope*	*Incpt*
					2	*4*	*8*	*12*	*16*		
ibuf	1	1	a_to_z	tpLH	0.49	0.53	0.59	0.66	0.72	0.0163	0.4600
				tpHL	0.36	0.38	0.43	0.47	0.52	0.0112	0.3400

Name: ibufn

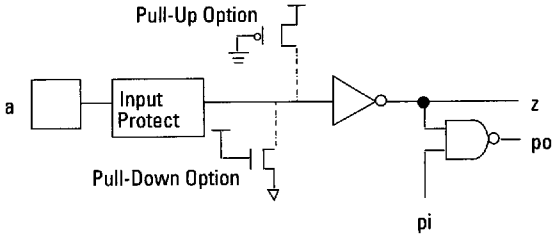
Description: Inverted CMOS Input Buffer

Coding Syntax: u(z,po)=&ibufn*(a,pi)

Logic Symbol:



Schematics:



Truth Table:

a	*pi*	*z*	*po*
0	1	1	0
1	x	0	1
0	0	1	1

Loading Characteristics:

Values stated in standard loads.

Version	*pi*
ibufn	0.5

Pin A Input Capacitance: Device(1.7 pF) + pad(0.8 pF) = 2.5 pF

AC Characteristics:

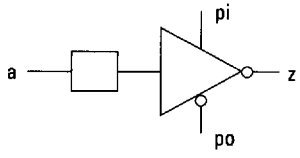
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

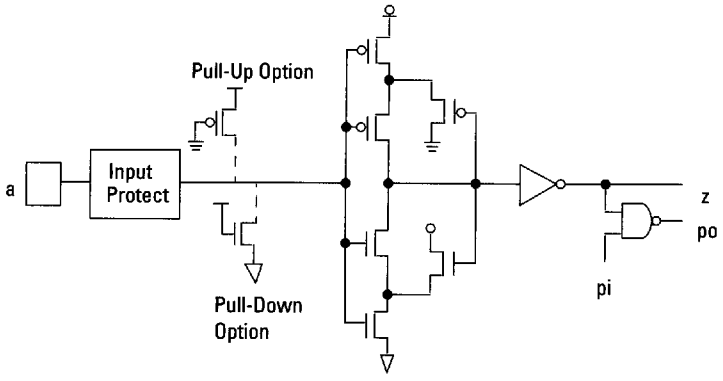
Version	*I/O Slots*	*Pads*	*Delay Path*	*Output*	*Standard Loads*					*Slope*	*Incpt*
					2	*4*	*8*	*12*	*16*		
ibufn	1	1	a_to_z	tpLH	0.26	0.30	0.37	0.45	0.53	0.0191	0.2200
				tpHL	0.34	0.38	0.44	0.51	0.57	0.0165	0.3100

Name: schmitc Description: Schmitt Trigger Input Buffer

Coding Syntax: u(z,po)=&schmitc*(a,pi)

Logic Symbol: Schematics:





Truth Table:

a	*pi*	*z*	*po*
0	x	0	1
1	0	1	1
1	1	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*pi*
schmitc	0.5

Pin A Input Capacitance: Device(1.7 pF) + pad(0.8 pF) = 2.5 pF

AC Characteristics:

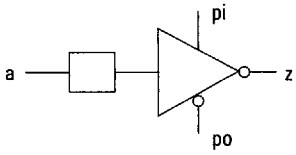
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

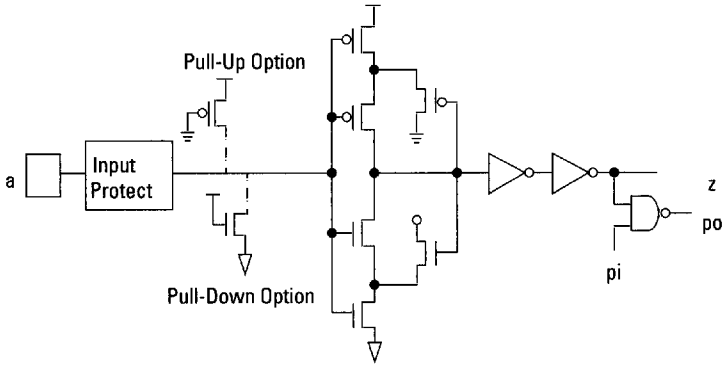
Version	*I/O Slots*	*Pads*	*Delay Path*	*Output*	*Standard Loads*					*Slope*	*Incpt*
					2	*4*	*8*	*12*	*16*		
schmitc	1	1	a_to_z	tpLH	1.07	1.17	1.37	1.57	1.77	0.0497	0.9700
				tpHL	1.36	1.41	1.50	1.60	1.70	0.0242	1.3100

Name: schmitcn Description: Inverted Schmitt Trigger Input Buffer

Coding Syntax: u(z,po)=&schmitcn*(a,pi)

Logic Symbol: Schematics:





Truth Table:

a	*pi*	*z*	*po*
0	0	1	1
0	1	1	0
1	x	0	1

Loading Characteristics:

Values stated in standard loads.

Version	*pi*
schmitcn	0.5

Pin A Input Capacitance: Device(1.7 pF) + pad(0.8 pF) = 2.5 pF

AC Characteristics:

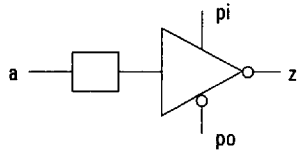
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

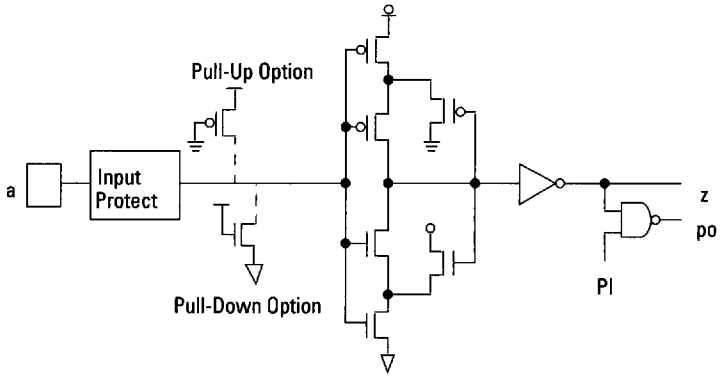
Version	*I/O Slots*	*Pads*	*Delay Path*	*Output*	*Standard Loads*					*Slope*	*Incpt*
					2	*4*	*8*	*12*	*16*		
schmitcn	1	1	a_to_z	tpLH	1.34	1.38	1.48	1.57	1.67	0.0236	1.2900
				tpHL	1.26	1.30	1.38	1.46	1.53	0.0196	1.2200

Name: schmitt Description: Input Pad with TTL-Level Schmitt Trigger

Coding Syntax: u(z,po)=&schmitt*(a,pi)

Logic Symbol: Schematics:





Truth Table:

a	*pi*	*z*	*po*
0	x	0	1
1	0	1	1
1	1	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*pi*
schmitt	0.5

Pin A Input Capacitance: Device(1.7 pF) + pad(0.8 pF) = 2.5 pF

AC Characteristics:

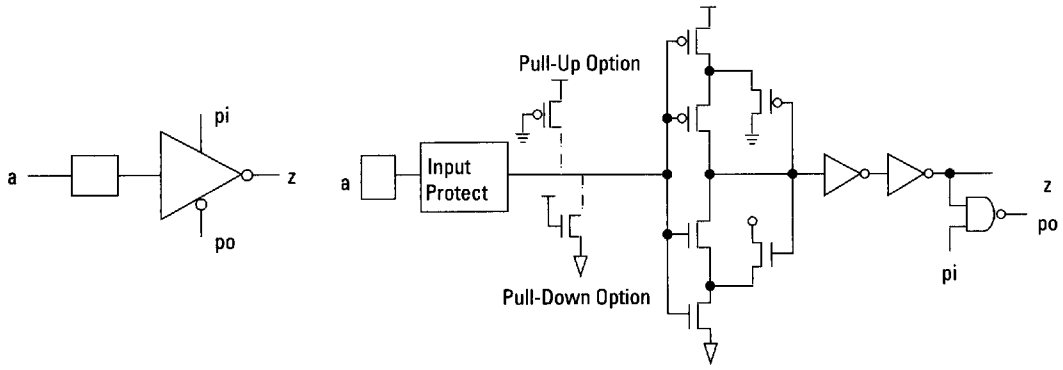
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/O Slots*	*Pads*	*Delay Path*	*Output*	*Standard Loads*					*Slope*	*Incpt*
					2	*4*	*8*	*12*	*16*		
schmitt	1	1	a_to_z	tpLH	1.11	1.20	1.40	1.59	1.79	0.0486	1.0100
				tpHL	1.18	1.23	1.34	1.44	1.55	0.0260	1.1300

Name: schmittn Description: Input Pad with Inverting TTL-Level Schmitt Trigger

Coding Syntax: u(z,po)=&schmittn*(a,pi)

Logic Symbol: Schematics:



Truth Table:

a	*pi*	*z*	*po*
0	0	1	1
0	1	1	0
1	x	0	1

Loading Characteristics:

Values stated in standard loads.

Version	*pi*
schmittn	0.5

Pin A Input Capacitance: Device(1.7 pF) + pad(0.8 pF) = 2.5 pF

AC Characteristics:

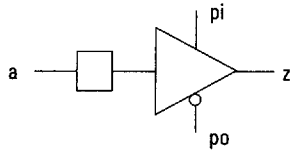
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

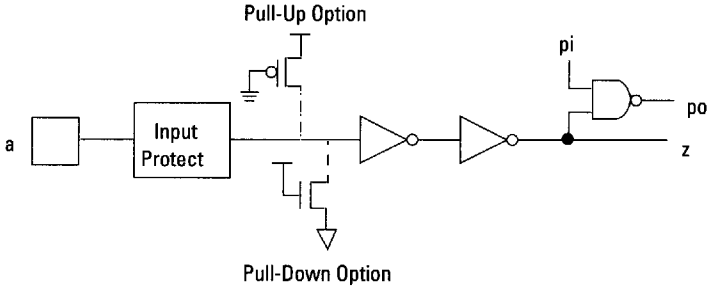
Version	*I/O Slots*	*Pads*	*Delay Path*	*Output*	*Standard Loads*					*Slope*	*Incpt*
					2	*4*	*8*	*12*	*16*		
schmittn	1	1	a_to_z	tpLH	1.13	1.17	1.24	1.31	1.37	0.0172	1.1000
				tpHL	1.46	1.51	1.61	1.70	1.80	0.0244	1.4100

Name: tlcht Description: TTL Input Buffer

Coding Syntax: u(z,po)=&tlcht*(a,pi)

Logic Symbol: Schematics:





Truth Table:

a	*pi*	*z*	*po*
0	x	0	1
1	0	1	1
1	1	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*pi*
tlcht	0.5

Pin A Input Capacitance: Device(1.7 pF) + pad(0.8 pF) = 2.5 pF

AC Characteristics:

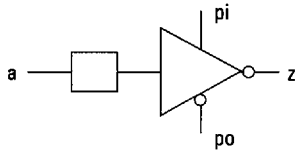
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

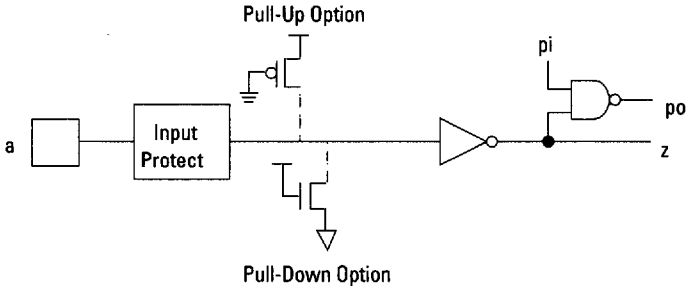
Version	*I/O Slots*	*Pads*	*Delay Path*	*Output*	*Standard Loads*					*Slope*	*Incpt*
					2	*4*	*8*	*12*	*16*		
tlcht	1	1	a_to_z	tpLH	0.51	0.54	0.60	0.66	0.72	0.0152	0.4800
				tpHL	0.37	0.39	0.42	0.46	0.50	0.0091	0.3500

Name: tlchn Description: Inverted TTL Input Buffer

Coding Syntax: u(z,po)=&tlchn*(a,pi)

Logic Symbol: Schematics:





Truth Table:

a	*pi*	*z*	*po*
0	0	1	1
1	x	0	1
0	1	1	0

Loading Characteristics:

Values stated in standard loads.

Version	*pi*
tlchn	0.5

Pin A Input Capacitance: Device(1.7 pF) + pad(0.8 pF) = 2.5 pF

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

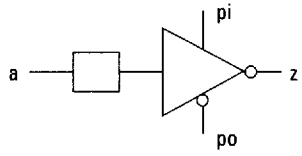
Version	*I/O Slots*	*Pads*	*Delay Path*	*Output*	*Standard Loads*					*Slope*	*Incpt*
					2	*4*	*8*	*12*	*16*		
tlchn	1	1	a_to_z	tpLH	0.29	0.39	0.59	0.79	1.00	0.0504	0.1900
				tpHL	0.36	0.40	0.49	0.58	0.67	0.0226	0.3100

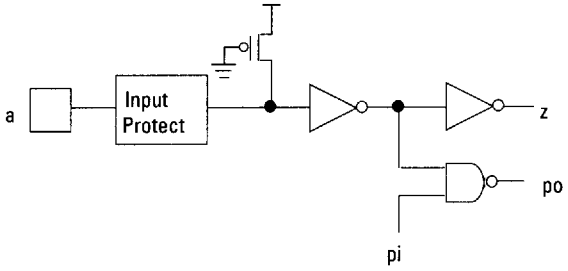
icptnu
Input Pad with Buffer for TN Input

Name: icptnu Description: Input Pad with Buffer for TN Input

Coding Syntax: u(z,po)=icptnu(a,pi)

Logic Symbol: Schematics:





Loading Characteristics:

Values stated in standard loads.

Version	*pi*
icptnu	0.3

Pin A Input Capacitance: Device(1.7 pF) + pad(0.8 pF) = 2.5 pF

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/O Slots*	*Pads*	*Delay Path*	*Output*	*Standard Loads*					*Slope*	*Incpt*
					2	*4*	*8*	*12*	*16*		
icptnu	1	1	a_to_z	tpLH	0.54	0.61	0.76	0.91	1.06	0.0376	0.4600
				tpHL	0.37	0.40	0.46	0.51	0.57	0.0146	0.3400
			a_to_po	tpLH	0.72	1.18	2.12	3.05	3.98	0.2332	0.2500
				tpHL	0.44	0.59	0.89	1.18	1.48	0.0745	0.2900

3.7 Unidirect Output Buffers

This section contains data pages for LCA300K unidirect output buffers.

Naming Conventions

Unidirect output buffer names have the following format:

root_name | ***drive_strength*** | ***slew_rate_control (optional)***

Table 3.3 shows the naming conventions used for unidirect output buffers.

Table 3.3 Unidirect Output Buffer Naming Conventions

Root Name	*Drive Strength in mA*	*Slew Rate Control Options*[1]
b	1	none = minimum
	2	rp = moderate
	4	r = maximum
	6	
	8	
	12	

1. Slew rate control is not available for `b1` *and* `b2` *buffers.*

For example, `b4rp` is a 4 mA unidirect output buffer with moderate slew rate control.

➤ ***Note:*** For the coding syntax, an asterisk following the cell name (for example, `b4*`) is a wildcard symbol that replaces options' abbreviations.

Converting Delays from CMOS to TTL

Buffer delays are given for CMOS levels. To convert the delay from a CMOS level (switching threshold = 2.5 V) to a TTL level (switching threshold = 1.4 V), use the following equations:

t_pHL = SLOPE x Cload x 1.5 + INCPT

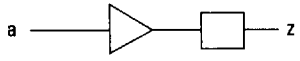
t_pLH = SLOPE x Cload x .55 + INCPT

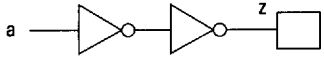
b1/b2
1 mA/2 mA Unidirect Output Buffer

Name: b1/b2 Description: 1 mA/2 mA Unidirect Output Buffer

Coding Syntax: z=&b1/b2(a)

Logic Symbol: Schematics:





Loading Characteristics:

Values stated in standard loads.

Version	*a*
b1	0.5
b2	0.5

Pin A Input Capacitance: Device(1.7 pF) + pad(0.8 pF) = 2.5 pF

AC Characteristics:

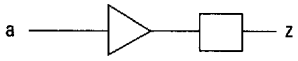
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

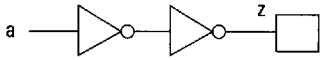
Version	*I/O Slots*	*Pads*	*Delay Path*	*Outputs*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
b1	1	1	a_to_z	tpLH	2.67	6.74	10.82	12.56	0.1164	0.9209
				tpHL	1.86	4.19	6.52	7.52	0.0665	0.8662
b2	1	1	a_to_z	tpLH	1.99	4.53	7.08	8.17	0.0728	0.8956
				tpHL	1.70	3.56	5.43	6.23	0.0534	0.8954

Name: b4 Description: 4 mA Unidirect Output Buffer

Coding Syntax: z=&b4*(a)

Logic Symbol: Schematics:





Loading Characteristics:

Values stated in standard loads.

Version	*a*
b4	0.5
b4r	0.5
b4rp	0.5

Pin A Input Capacitance: Device(1.7 pF) + pad(0.8 pF) = 2.5 pF

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

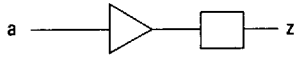
Version	*I/O Slots*	*Pads*	*Delay Path*	*Outputs*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
b4	1	1	a_to_z	tpLH	1.46	2.75	4.04	4.59	0.0367	0.9139
				tpHL	1.46	2.50	3.55	3.99	0.0298	1.0124
b4r	1	1	a_to_z	tpLH	1.84	3.47	5.09	5.79	0.0464	1.1439
				tpHL	1.85	3.14	4.43	4.98	0.0367	1.3039
b4rp	1	1	a_to_z	tpLH	1.83	3.23	4.64	5.24	0.0402	1.2246
				tpHL	1.96	3.15	4.34	4.85	0.0340	1.4553

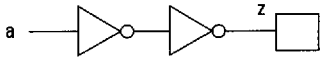
b6
6 mA Unidirect Output Buffer

Name: b6 Description: 6 mA Unidirect Output Buffer

Coding Syntax: z=&b6*(a)

Logic Symbol: Schematics:





Loading Characteristics:

Values stated in standard loads.

Version	*a*
b6	0.5
b6r	0.5
b6rp	0.5

Pin A Input Capacitance: Device(1.7 pF) + pad(0.8 pF) = 2.5 pF

AC Characteristics:

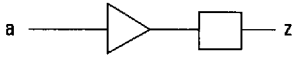
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

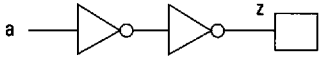
Version	*I/O Slots*	*Pads*	*Delay Path*	*Outputs*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
b6	1	1	a_to_z	tpLH	1.38	2.30	3.22	3.62	0.0263	0.9816
				tpHL	1.43	2.23	3.03	3.38	0.0229	1.0909
b6r	1	1	a_to_z	tpLH	1.74	2.98	4.21	4.74	0.0353	1.2096
				tpHL	1.86	2.93	4.00	4.45	0.0305	1.4045
b6rp	1	1	a_to_z	tpLH	1.80	2.87	3.94	4.39	0.0305	1.3445
				tpHL	2.06	3.01	3.95	4.36	0.0270	1.6538

Name: b8 Description: 8 mA Unidirect Output Buffer

Coding Syntax: z=&b8*(a)

Logic Symbol: Schematics:





Loading Characteristics:

Values stated in standard loads.

Version	*a*
b8	0.5
b8r	0.5
b8rp	0.5

Pin A Input Capacitance: Device(1.7 pF) + pad(0.8 pF) = 2.5 pF

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

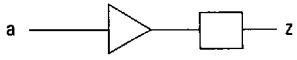
Version	*I/O Slots*	*Pads*	*Delay Path*	*Outputs*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
b8	1	1	a_to_z	tpLH	1.33	2.13	2.93	3.28	0.0229	0.9909
				tpHL	1.42	2.07	2.73	3.01	0.0187	1.1380
b8r	1	1	a_to_z	tpLH	1.70	2.72	3.73	4.17	0.0291	1.2602
				tpHL	1.81	2.68	3.56	3.93	0.0249	1.4373
b8rp	1	1	a_to_z	tpLH	1.74	2.64	3.54	3.92	0.0256	1.3595
				tpHL	1.98	2.83	3.68	4.04	0.0243	1.6152

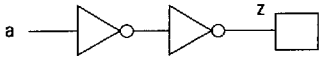
b12
12 mA Unidirect Output Buffer

Name: b12 Description: 12 mA Unidirect Output Buffer

Coding Syntax: z=&b12*(a)

Logic Symbol: Schematics:





Loading Characteristics:

Values stated in standard loads.

Version	*a*
b12	0.5
b12r	0.5
b12rp	0.5

Pin A Input Capacitance: Device(1.7 pF) + pad(0.8 pF) = 2.5 pF

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/O Slots*	*Pads*	*Delay Path*	*Outputs*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
b12	1	1	a_to_z	tpLH	1.34	2.02	2.70	2.99	0.0194	1.0502
				tpHL	1.45	2.01	2.56	2.80	0.0159	1.2094
b12r	1	1	a_to_z	tpLH	1.71	2.61	3.51	3.89	0.0256	1.3295
				tpHL	1.87	2.67	3.47	3.82	0.0229	1.5309
b12rp	1	1	a_to_z	tpLH	1.82	2.62	3.42	3.77	0.0229	1.4809
				tpHL	2.02	2.82	3.62	3.97	0.0229	1.6809

3.8 Bidirect Output Buffers

This section contains data pages for LCA300K bidirect output buffers.

Naming Conventions

Bidirect output buffer names have the following format:

root_name | ***drive_strength*** | ***input_voltage_level (optional)*** | ***slew_rate_control (optional)*** | ***resistors (optional)*** | ***other options***

Table 3.4 shows the naming conventions used for bidirect output buffers.

Table 3.4 Bidirect Output Buffer Naming Conventions

Root Name	*Drive Strength in mA*	*Input Voltage Level Options*	*Slew Rate Control Options*[1]	*Optional Resistors*[2]	*Other Options*[3]
bd	1	t = TTL	none = minimum	u = pull-up	od = Open drain
	2	tn = inverted TTL	rp = moderate	d = pull-down	
	4	c = CMOS	r = maximum		
	6	cn = inverted CMOS			
	8	sc = Schmitt trigger for CMOS			
	12	scn = Inverting CMOS Schmitt trigger			
		st = Schmitt trigger for TTL			
		stn = inverting TTL Schmitt trigger			

1. *Not available for 1 mA and 2 mA drive strengths.*
2. *Open drain option is not available for cells using these options.*
3. *Slew rate control and pull-up or pull-down resistors are not available for cells using this option.*

For example, `bd4tru` is a 4 mA bidirect output buffer with TTL input, maximum slew rate control, and a pull-up resistor.

➤ ***Note:*** In the coding syntax, an asterisk following the cell name (for example, `bd1*`) is a wildcard symbol that replaces options' abbreviations.

Converting Delays from CMOS to TTL

Buffer delays are given for CMOS levels. To convert the delay from a CMOS level (switching threshold = 2.5 V) to a TTL level (switching threshold = 1.4 V), use the following equations:

t_PHL = SLOPE x Cload x 1.5 + INCPT

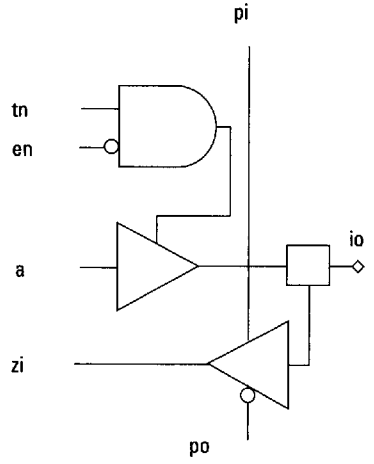
t_PLH = SLOPE x Cload x .55 + INCPT

Calculating Input Delays

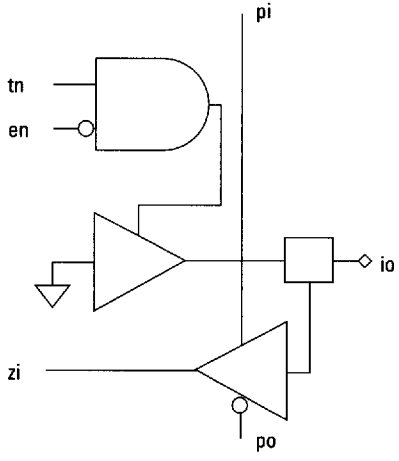
Bidirect output buffers have the features of both input and output buffers. The numbers listed in the tables show output delay times (a-io or en-io). To calculate input delays (a-z), refer to the Input Buffer section. For example, to calculate input delays for `bd4tru`, use the numbers listed for the input buffer `tlchtu` (a TTL input buffer with a pull-up resistor).

Bidirect Output Buffer Logic Symbols

Bidirect Buffer with Slew Rate Control and Optional Pull-up/Pull-down

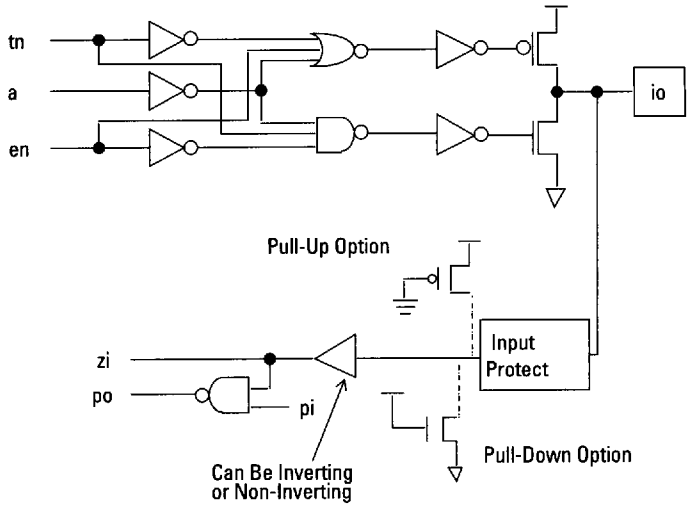


Bidirect Buffer with Open Drain

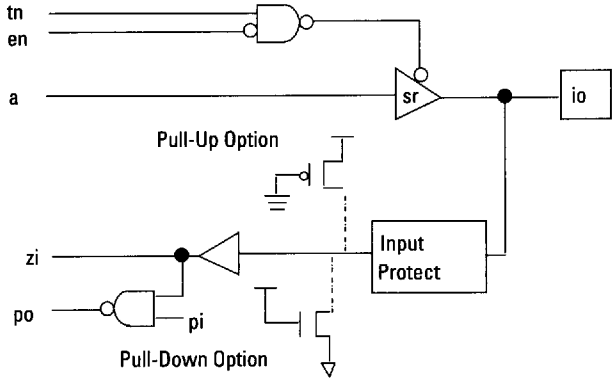


Bidirect Output Buffer Schematics

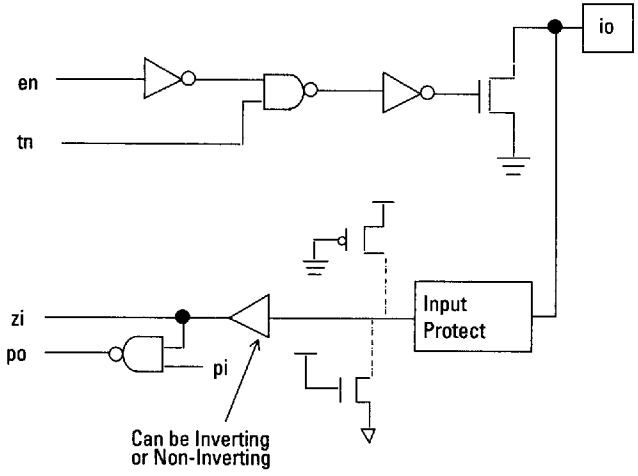
Bidirect Buffer with Optional Pull-up/Pull-down



Bidirect Buffer with Slew Rate Control and Optional Pull-up/Pull-down



Bidirect Buffer with Open Drain



bd1
1 mA Bidirect Output Buffer

Name: bd1 Description: 1 mA Bidirect Output Buffer

Coding Syntax: u(io,zi,po) = &bd1*(io,a,en,tn,pi)
u(io,zi,po) = &bd1*od(io,en,tn,pi)

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*en*	*tn*	*pi*
bd1*	0.5	1.0	0.5	0.5
bd1*od	-	1.0	0.5	0.5

Pin IO Input Capacitance: Device(1.7 pF) + pad(0.8 pF) = 2.5 pF

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/D Slots*	*Pads*	*Delay Path*	*Output*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
bd1*	1	1	a_to_io	tpLH	3.20	8.30	13.39	15.57	0.1455	1.0211
				tpHL	2.98	7.64	12.29	14.29	0.1331	0.9825
			en_to_io	tpZH	3.24	8.34	13.43	15.61	0.1455	1.0611
				tpZL	3.02	7.68	12.33	14.33	0.1331	1.0225
				tpLZ	2.59	7.25	11.90	13.90	0.1331	0.5925
				tpHZ	2.81	7.91	13.00	15.18	0.1455	0.6311
			tn_to_io	tpLZ	2.88	7.54	12.19	14.19	0.1331	0.8825
				tpHZ	3.10	8.20	13.29	15.47	0.1455	0.9211
				tpZH	3.42	8.52	13.61	15.79	0.1455	1.2411
				tpZL	3.20	7.86	12.51	14.51	0.1331	1.2025
bd1*od	1	1	en_to_io	tpLZ	0.19	0.19	0.19	0.19	0.0000	0.1900
				tpZL	1.36	3.69	6.02	7.02	0.0665	0.3662
			tn_to_io	tpLZ	0.47	0.47	0.47	0.47	0.0000	0.4700
				tpZL	1.64	3.97	6.30	7.30	0.0665	0.6462

Name: bd2 Description: 2 mA Bidirect Output Buffer

Coding Syntax: u(io,zi,po) = &bd2*(io,a,en,tn,pi)
u(io,zi,po) = &bd2*od(io,en,tn,pi)

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*en*	*tn*	*pi*
bd2*	0.5	1.0	0.5	0.5
bd2*od	-	1.0	0.5	0.5

Pin IO Input Capacitance: Device(1.7 pF) + pad(0.8 pF) = 2.5 pF

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/D Slots*	*Pads*	*Delay Path*	*Output*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
bd2*	1	1	a_to_io	tpLH	2.03	4.57	7.12	8.21	0.0728	0.9356
				tpHL	1.93	4.26	6.59	7.59	0.0665	0.9362
			en_to_io	tpZH	2.10	4.64	7.19	8.28	0.0728	1.0056
				tpZL	2.00	4.33	6.66	7.66	0.0665	1.0062
				tpLZ	1.64	3.97	6.30	7.30	0.0665	0.6462
				tpHZ	1.78	4.32	6.87	7.96	0.0728	0.6856
			tn_to_io	tpZH	2.28	4.82	7.37	8.46	0.0728	1.1856
				tpZL	2.18	4.51	6.84	7.84	0.0665	1.1862
				tpLZ	1.93	4.26	6.59	7.59	0.0665	0.9362
				tpHZ	2.07	4.61	7.16	8.25	0.0728	0.9756
bd2*od	1	1	en_to_io	tpLZ	0.22	0.22	0.22	0.22	0.0000	0.2200
				tpZL	1.17	3.03	4.90	5.70	0.0534	0.3654
			tn_to_io	tpLZ	0.50	0.50	0.50	0.50	0.0000	0.5000
				tpZL	1.45	3.31	5.18	5.98	0.0534	0.6454

bd4
4 mA Bidirect Output Buffer

Name: bd4 Description: 4 mA Bidirect Output Buffer

Coding Syntax: u(io,zi,po) = &bd4*(io,a,en,tn,pi)
u(io,zi,po) = &bd4*od(io,en,tn,pi)

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*en*	*tn*	*pi*
bd4*	0.5	1.0	0.5	0.5
bd4*od	-	1.0	0.5	0.5
bd4*r	0.5	1.0	0.5	0.5
bd4*rp	0.5	1.0	0.5	0.5

Pin IO Input Capacitance: Device(1.7 pF) + pad(0.8 pF) = 2.5 pF

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/D Slots*	*Pads*	*Delay Path*	*Output*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
bd4*	1	1	a_to_io	tpLH	1.49	2.78	4.07	4.62	0.0367	0.9439
				tpHL	1.42	2.46	3.51	3.95	0.0298	0.9724
			en_to_io	tpZH	1.76	3.05	4.34	4.89	0.0367	1.2139
				tpZL	1.69	2.73	3.78	4.22	0.0298	1.2424
				tpLZ	1.24	2.28	3.33	3.77	0.0298	0.7924
				tpHZ	1.41	2.70	3.99	4.54	0.0367	0.8639
			tn_to_io	tpZH	1.94	3.23	4.52	5.07	0.0367	1.3939
				tpZL	1.87	2.91	3.96	4.40	0.0298	1.4224
				tpLZ	1.53	2.57	3.62	4.06	0.0298	1.0824
				tpHZ	1.70	2.99	4.28	4.83	0.0367	1.1539
bd4*od	1	1	en_to_io	tpLZ	0.30	0.30	0.30	0.30	0.0000	0.3000
				tpZL	0.88	1.95	3.02	3.47	0.0305	0.4245
			tn_to_io	tpLZ	0.58	0.58	0.58	0.58	0.0000	0.5800
				tpZL	1.16	2.23	3.30	3.75	0.0305	0.7045

AC Characteristics: (Cont.)

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/D Slots*	*Pads*	*Delay Path*	*Output*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
bd4*r	1	1	a_to_io	tpLH	1.70	3.35	5.00	5.71	0.0471	0.9961
				tpHL	1.53	2.77	4.00	4.53	0.0353	0.9996
			en_to_io	tpZH	1.76	3.41	5.06	5.77	0.0471	1.0561
				tpZL	1.81	3.05	4.28	4.81	0.0353	1.2796
				tpLZ	1.25	2.49	3.72	4.25	0.0353	0.7196
				tpHZ	1.72	3.37	5.02	5.73	0.0471	1.0161
			tn_to_io	tpZH	1.90	3.55	5.20	5.91	0.0471	1.1961
				tpZL	1.95	3.19	4.42	4.95	0.0353	1.4196
				tpLZ	1.33	2.57	3.80	4.33	0.0353	0.7996
				tpHZ	1.80	3.45	5.10	5.81	0.0471	1.0961
bd4*rp	1	1	a_to_io	tpLH	1.61	3.04	4.47	5.09	0.0409	0.9967
				tpHL	1.48	2.59	3.71	4.19	0.0319	0.9988
			en_to_io	tpZH	1.57	3.00	4.43	5.05	0.0409	0.9567
				tpZL	1.58	2.69	3.81	4.29	0.0319	1.0988
				tpLZ	1.35	2.46	3.58	4.06	0.0319	0.8688
				tpHZ	1.68	3.11	4.54	5.16	0.0409	1.0667
			tn_to_io	tpZH	1.79	3.22	4.65	5.27	0.0409	1.1767
				tpZL	1.80	2.91	4.03	4.51	0.0319	1.3188
				tpLZ	1.42	2.53	3.65	4.13	0.0319	0.9388
				tpHZ	1.75	3.18	4.61	5.23	0.0409	1.1367

bd6
6 mA Bidirect Output Buffer

Name: bd6 Description: 6 mA Bidirect Output Buffer

Coding Syntax: u(io,zi,po) = &bd6*(io,a,en,tn,pi)
u(io,zi,po) = &bd6*od(io,en,tn,pi)

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*en*	*tn*	*pi*
bd6*	0.5	1.0	0.5	0.5
bd6*od	-	1.0	0.5	0.5
bd6*r	0.5	1.0	0.5	0.5
bd6*rp	0.5	1.0	0.5	0.5

Pin IO Input Capacitance: Device(1.7 pF) + pad(0.8 pF) = 2.5 pF

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/D Slots*	*Pads*	*Delay Path*	*Output*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
bd6*	1	1	a_to_io	tpLH	1.41	2.36	3.30	3.71	0.0270	1.0038
				tpHL	1.35	2.15	2.95	3.30	0.0229	1.0109
			en_to_io	tpZH	1.48	2.43	3.37	3.78	0.0270	1.0738
				tpZL	1.42	2.22	3.02	3.37	0.0229	1.0809
				tpLZ	1.32	2.12	2.92	3.27	0.0229	0.9809
				tpHZ	1.42	2.37	3.31	3.72	0.0270	1.0138
			tn_to_io	tpZH	1.66	2.61	3.55	3.96	0.0270	1.2538
				tpZL	1.60	2.40	3.20	3.55	0.0229	1.2609
				tpLZ	1.61	2.41	3.21	3.56	0.0229	1.2709
				tpHZ	1.71	2.66	3.60	4.01	0.0270	1.3038
bd6*od	1	1	en_to_io	tpLZ	0.35	0.35	0.35	0.35	0.0000	0.3500
				tpZL	0.79	1.59	2.39	2.74	0.0229	0.4509
			tn_to_io	tpLZ	0.63	0.63	0.63	0.63	0.0000	0.6300
				tpZL	1.07	1.87	2.67	3.02	0.0229	0.7309

AC Characteristics: (Cont.)

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/D Slots*	*Pads*	*Delay Path*	*Output*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
bd6*r	1	1	a_to_io	tpLH	1.56	2.82	4.08	4.63	0.0360	1.0217
				tpHL	1.44	2.41	3.38	3.80	0.0277	1.0259
			en_to_io	tpZH	1.67	2.93	4.19	4.74	0.0360	1.1317
				tpZL	1.77	2.74	3.71	4.13	0.0277	1.3559
				tpLZ	1.25	2.22	3.19	3.61	0.0277	0.8359
				tpHZ	1.65	2.91	4.17	4.72	0.0360	1.1117
			tn_to_io	tpZH	1.81	3.07	4.33	4.88	0.0360	1.2717
				tpZL	1.91	2.88	3.85	4.27	0.0277	1.4959
				tpLZ	1.33	2.30	3.27	3.69	0.0277	0.9159
				tpHZ	1.73	2.99	4.25	4.80	0.0360	1.1917
bd6*rp	1	1	a_to_io	tpLH	1.48	2.55	3.62	4.07	0.0305	1.0245
				tpHL	1.38	2.20	3.03	3.38	0.0236	1.0230
			en_to_io	tpZH	1.53	2.60	3.67	4.12	0.0305	1.0745
				tpZL	1.57	2.39	3.22	3.57	0.0236	1.2130
				tpLZ	1.31	2.13	2.96	3.31	0.0236	0.9530
				tpHZ	1.59	2.66	3.73	4.18	0.0305	1.1345
			tn_to_io	tpZH	1.75	2.82	3.89	4.34	0.0305	1.2945
				tpZL	1.79	2.61	3.44	3.79	0.0236	1.4330
				tpLZ	1.38	2.20	3.03	3.38	0.0236	1.0230
				tpHZ	1.66	2.73	3.80	4.25	0.0305	1.2045

bd8

8 mA Bidirect Output Buffer

Name: bd8 Description: 8 mA Bidirect Output Buffer

Coding Syntax: u(io,zi,po) = &bd8*(io,a,en,tn,pi)
u(io,zi,po) = &bd8*od(io,en,tn,pi)

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*en*	*tn*	*pi*
bd8*	0.5	1.0	0.5	0.5
bd8*od	-	1.0	0.5	0.5
bd8*r	0.5	1.0	0.5	0.5
bd8*rp	0.5	1.0	0.5	0.5

Pin IO Input Capacitance: Device(1.7 pF) + pad(0.8 pF) = 2.5 pF

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/D Slots*	*Pads*	*Delay Path*	*Output*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
bd8*	1	1	a_to_io	tpLH	1.36	2.16	2.96	3.31	0.0229	1.0209
				tpHL	1.33	1.96	2.59	2.86	0.0180	1.0559
			en_to_io	tpZH	1.45	2.25	3.05	3.40	0.0229	1.1109
				tpZL	1.42	2.05	2.68	2.95	0.0180	1.1459
				tpLZ	1.33	1.96	2.59	2.86	0.0180	1.0559
				tpHZ	1.46	2.26	3.06	3.41	0.0229	1.1209
			tn_to_io	tpZH	1.63	2.43	3.23	3.58	0.0229	1.2909
				tpZL	1.60	2.23	2.86	3.13	0.0180	1.3259
				tpLZ	1.62	2.25	2.88	3.15	0.0180	1.3459
				tpHZ	1.75	2.55	3.35	3.70	0.0229	1.4109
bd8*od	1	1	en_to_io	tpLZ	0.37	0.37	0.37	0.37	0.0000	0.3700
				tpZL	0.77	1.42	2.08	2.36	0.0187	0.4880
			tn_to_io	tpLZ	0.65	0.65	0.65	0.65	0.0000	0.6500
				tpZL	1.05	1.70	2.36	2.64	0.0187	0.7680

AC Characteristics: (Cont.)

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/D Slots*	*Pads*	*Delay Path*	*Output*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
bd8*r	1	1	a_to_io	tpLH	1.49	2.51	3.52	3.96	0.0291	1.0502
				tpHL	1.38	2.13	2.88	3.20	0.0215	1.0566
			en_to_io	tpZH	1.59	2.61	3.62	4.06	0.0291	1.1502
				tpZL	1.70	2.45	3.20	3.52	0.0215	1.3766
				tpLZ	1.22	1.97	2.72	3.04	0.0215	0.8966
				tpHZ	1.61	2.63	3.64	4.08	0.0291	1.1702
			tn_to_io	tpZH	1.73	2.75	3.76	4.20	0.0291	1.2902
				tpZL	1.84	2.59	3.34	3.66	0.0215	1.5166
				tpLZ	1.30	2.05	2.80	3.12	0.0215	0.9766
				tpHZ	1.69	2.71	3.72	4.16	0.0291	1.2502
bd8*rp	1	1	a_to_io	tpLH	1.42	2.32	3.22	3.60	0.0256	1.0395
				tpHL	1.35	2.06	2.76	3.06	0.0201	1.0523
			en_to_io	tpZH	1.48	2.38	3.28	3.66	0.0256	1.0995
				tpZL	1.55	2.26	2.96	3.26	0.0201	1.2523
				tpLZ	1.25	1.96	2.66	2.96	0.0201	0.9523
				tpHZ	1.52	2.42	3.32	3.70	0.0256	1.1395
			tn_to_io	tpZH	1.70	2.60	3.50	3.88	0.0256	1.3195
				tpZL	1.77	2.48	3.18	3.48	0.0201	1.4723
				tpLZ	1.32	2.03	2.73	3.03	0.0201	1.0223
				tpHZ	1.59	2.49	3.39	3.77	0.0256	1.2095

Name: bd12 Description: 12 mA Bidirect Output Buffer

Coding Syntax: u(io,zi,po) = &bd12*(io,a,en,tn,pi)
u(io,zi,po) = &bd12*od(io,en,tn,pi)

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*en*	*tn*	*pi*
bd12*	0.5	1.0	0.5	0.5
bd12*od	-	1.0	0.5	0.5
bd12*r	0.5	1.0	0.5	0.5
bd12*rp	0.5	1.0	0.5	0.5

Pin IO Input Capacitance: Device(1.7 pF) + pad(0.8 pF) = 2.5 pF

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/D Slots*	*Pads*	*Delay Path*	*Output*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
bd12*	1	1	a_to_io	tpLH	1.36	2.07	2.77	3.07	0.0201	1.0623
				tpHL	1.33	1.89	2.44	2.68	0.0159	1.0894
			en_to_io	tpZH	1.43	2.14	2.84	3.14	0.0201	1.1323
				tpZL	1.40	1.96	2.51	2.75	0.0159	1.1594
				tpLZ	1.39	1.95	2.50	2.74	0.0159	1.1494
				tpHZ	1.50	2.21	2.91	3.21	0.0201	1.2023
			tn_to_io	tpZH	1.61	2.32	3.02	3.32	0.0201	1.3123
				tpZL	1.58	2.14	2.69	2.93	0.0159	1.3394
				tpLZ	1.68	2.24	2.79	3.03	0.0159	1.4394
				tpHZ	1.79	2.50	3.20	3.50	0.0201	1.4923
bd12*od	1	1	en_to_io	tpLZ	0.41	0.41	0.41	0.41	0.0000	0.4100
				tpZL	0.77	1.35	1.94	2.18	0.0166	0.5216
			tn_to_io	tpLZ	0.69	0.69	0.69	0.69	0.0000	0.6900
				tpZL	1.05	1.63	2.22	2.46	0.0166	0.8016

AC Characteristics: (Cont.)

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/D Slots*	*Pads*	*Delay Path*	*Output*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
bd12*r	1	1	a_to_io	tpLH	1.42	2.32	3.22	3.60	0.0256	1.0395
				tpHL	1.37	2.02	2.68	2.96	0.0187	1.0880
			en_to_io	tpZH	1.55	2.45	3.35	3.73	0.0256	1.1695
				tpZL	1.72	2.37	3.03	3.31	0.0187	1.4380
				tpLZ	1.27	1.92	2.58	2.86	0.0187	0.9880
				tpHZ	1.68	2.58	3.48	3.86	0.0256	1.2995
			tn_to_io	tpZH	1.69	2.59	3.49	3.87	0.0256	1.3095
				tpZL	1.86	2.51	3.17	3.45	0.0187	1.5780
				tpLZ	1.35	2.00	2.66	2.94	0.0187	1.0680
				tpHZ	1.76	2.66	3.56	3.94	0.0256	1.3795
bd12*rp	1	1	a_to_io	tpLH	1.40	2.20	3.00	3.35	0.0229	1.0609
				tpHL	1.35	1.93	2.52	2.76	0.0166	1.1016
			en_to_io	tpZH	1.46	2.26	3.06	3.41	0.0229	1.1209
				tpZL	1.55	2.13	2.72	2.96	0.0166	1.3016
				tpLZ	1.25	1.83	2.42	2.66	0.0166	1.0016
				tpHZ	1.56	2.36	3.16	3.51	0.0229	1.2209
			tn_to_io	tpZH	1.68	2.48	3.28	3.63	0.0229	1.3409
				tpZL	1.77	2.35	2.94	3.18	0.0166	1.5216
				tpLZ	1.32	1.90	2.49	2.73	0.0166	1.0716
				tpHZ	1.63	2.43	3.23	3.58	0.0229	1.2909

3.9 3-State Output Buffers

This section contains data pages for LCA300K 3-state output buffers.

Naming Conventions

3-state output buffer names have the following format:

root_name | ***drive_strength*** | ***slew_rate_control (optional)*** | ***other option***

Table 3.5 shows the naming conventions used for 3-state output buffers.

Table 3.5 3-State Output Buffer Naming Conventions

Root Name	*Drive Strengths in mA*	*Slew Rate Control Options*[1]	*Other Option*[2]
bt	1	none = minimum	od = Open Drain
	2	rp = moderate	
	4	r = maximum	
	6		
	8		
	12		

1. *Not available for* `bt1` *and* `bt2`.
2. *Slew rate control is not available for cells using the open drain option.*

For example, `bt4rp` is a 4 mA 3-state output buffer with moderate slew rate control.

➤ ***Note:*** For the coding syntax, an asterisk following the cell name (for example, `bt1*`) is a wildcard symbol that replaces options' abbreviations.

Converting Delays from CMOS to TTL

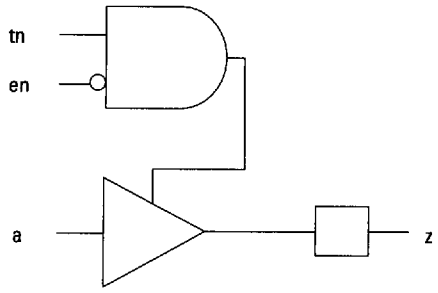
Buffer delays are given for CMOS levels. To convert the delay from a CMOS level (switching threshold = 2.5 V) to a TTL level (switching threshold = 1.4 V), use the following equations:

t_PHL = SLOPE x Cload x 1.5 + INCPT

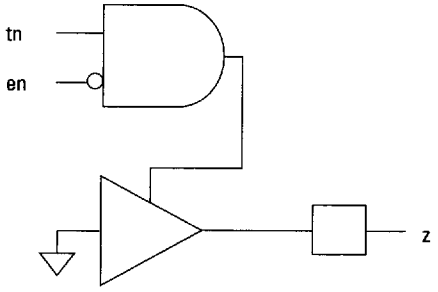
t_PLH = SLOPE x Cload x .55 + INCPT

3-State Output Buffer Logic Symbols

3-State Buffer with Slew Rate Control

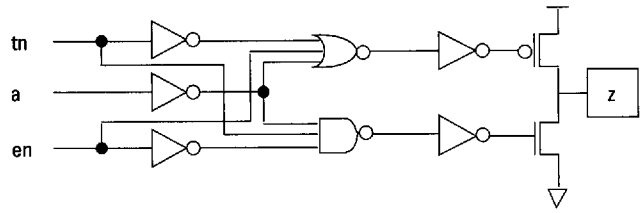


3-State Buffer with Open Drain

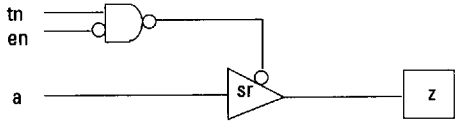


3-State Output Buffer Schematics

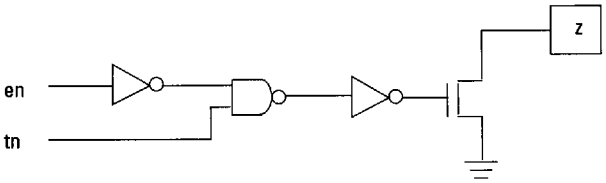
3-State Buffer



3-State Buffer with Slew Rate Control



3-State Buffer with Open Drain



Name: bt1 Description: 1 mA 3-State Output Buffer

Coding Syntax: z=&bt1(a,en,tn)
z=&bt1od(en,tn)

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*en*	*tn*
bt1	0.5	1.0	0.5
bt1od	–	1.0	0.5

Pin Z Input Capacitance: Device(1.7 pF) + pad(0.8 pF) = 2.5 pF

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/D Slots*	*Pads*	*Delay Path*	*Output*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
bt1	1	1	a_to_z	tpLH	3.20	8.30	13.39	15.57	0.1455	1.0211
				tpHL	2.98	7.64	12.29	14.29	0.1331	0.9825
			en_to_z	tpZH	3.24	8.34	13.43	15.61	0.1455	1.0611
				tpZL	3.02	7.68	12.33	14.33	0.1331	1.0225
				tpLZ	2.59	7.25	11.90	13.90	0.1331	0.5925
				tpHZ	2.81	7.91	13.00	15.18	0.1455	0.6311
			tn_to_z	tpLZ	2.88	7.54	12.19	14.19	0.1331	0.8825
				tpHZ	3.10	8.20	13.29	15.47	0.1455	0.9211
				tpZH	3.42	8.52	13.61	15.79	0.1455	1.2411
				tpZL	3.20	7.86	12.51	14.51	0.1331	1.2025
bt1od	1	1	en_to_z	tpLZ	0.19	0.19	0.19	0.19	0.0000	0.1900
				tpZL	1.36	3.69	6.02	7.02	0.0665	0.3662
			tn_to_z	tpLZ	0.59	0.59	0.59	0.59	0.0000	0.5900
				tpZL	1.64	3.97	6.30	7.30	0.0665	0.6462

Name: bt2 Description: 2 mA 3-State Output Buffer

Coding Syntax: z =&bt2(a,en,tn)
z=&bt2od(en,tn)

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*en*	*tn*
bt2	0.5	1.0	0.5
bt2od	–	1.0	0.5

Pin Z Input Capacitance: Device(1.7 pF) + pad(0.8 pF) = 2.5 pF

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/D Slots*	*Pads*	*Delay Path*	*Output*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
bt2	1	1	a_to_z	tpLH	2.03	4.57	7.12	8.21	0.0728	0.9356
				tpHL	1.93	4.26	6.59	7.59	0.0665	0.9362
			en_to_z	tpZH	2.10	4.64	7.19	8.28	0.0728	1.0056
				tpZL	2.00	4.33	6.66	7.66	0.0665	1.0062
				tpLZ	1.64	3.97	6.30	7.30	0.0665	0.6462
				tpHZ	1.78	4.32	6.87	7.96	0.0728	0.6856
			tn_to_z	tpLZ	1.93	4.26	6.59	7.59	0.0665	0.9362
				tpHZ	2.07	4.61	7.16	8.25	0.0728	0.9756
				tpZH	2.28	4.82	7.37	8.46	0.0728	1.1856
				tpZL	2.18	4.51	6.84	7.84	0.0665	1.1862
bt2od	1	1	en_to_z	tpLZ	0.22	0.22	0.22	0.22	0.0000	0.2200
				tpZL	1.17	3.03	4.90	5.70	0.0534	0.3654
			tn_to_z	tpLZ	0.62	0.62	0.62	0.62	0.0000	0.6200
				tpZL	1.45	3.31	5.18	5.98	0.0534	0.6454

bt4
4 mA 3-State Output Buffer

Name: bt4 Description: 4 mA 3-State Output Buffer

Coding Syntax: z=&bt4*(a,en,tn)
z=&bt4od(en,tn)

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*en*	*tn*
bt4	0.5	1.0	0.5
bt4od	-	1.0	0.5
bt4r	0.5	1.0	0.5
bt4rp	0.5	1.0	0.5

Pin Z Input Capacitance: Device(1.7 pF) + pad(0.8 pF) = 2.5 pF

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/D Slots*	*Pads*	*Delay Path*	*Output*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
bt4	1	1	a_to_z	tpLH	1.49	2.78	4.07	4.62	0.0367	0.9439
				tpHL	1.42	2.46	3.51	3.95	0.0298	0.9724
			en_to_z	tpZH	1.76	3.05	4.34	4.89	0.0367	1.2139
				tpZL	1.69	2.73	3.78	4.22	0.0298	1.2424
				tpLZ	1.24	2.28	3.33	3.77	0.0298	0.7924
				tpHZ	1.41	2.70	3.99	4.54	0.0367	0.8639
			tn_to_z	tpLZ	1.53	2.57	3.62	4.06	0.0298	1.0824
				tpHZ	1.70	2.99	4.28	4.83	0.0367	1.1539
				tpZH	1.94	3.23	4.52	5.07	0.0367	1.3939
				tpZL	1.87	2.91	3.96	4.40	0.0298	1.4224
bt4od	1	1	en_to_z	tpLZ	0.30	0.30	0.30	0.30	0.0000	0.3000
				tpZL	0.88	1.95	3.02	3.47	0.0305	0.4245
			tn_to_z	tpLZ	0.70	0.70	0.70	0.70	0.0000	0.7000
				tpZL	1.16	2.23	3.30	3.75	0.0305	0.7045

AC Characteristics: (Cont.)

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/D Slots*	*Pads*	*Delay Path*	*Output*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
bt4r	1	1	a_to_z	tpLH	1.70	3.35	5.00	5.71	0.0471	0.9961
				tpHL	1.53	2.77	4.00	4.53	0.0353	0.9996
			en_to_z	tpZH	1.76	3.41	5.06	5.77	0.0471	1.0561
				tpZL	1.81	3.05	4.28	4.81	0.0353	1.2796
				tpLZ	1.25	2.49	3.72	4.25	0.0353	0.7196
				tpHZ	1.72	3.37	5.02	5.73	0.0471	1.0161
			tn_to_z	tpLZ	1.33	2.57	3.80	4.33	0.0353	0.7996
				tpHZ	1.80	3.45	5.10	5.81	0.0471	1.0961
				tpZH	1.90	3.55	5.20	5.91	0.0471	1.1961
				tpZL	1.95	3.19	4.42	4.95	0.0353	1.4196
bt4rp	1	1	a_to_z	tpLH	1.61	3.04	4.47	5.09	0.0409	0.9967
				tpHL	1.48	2.59	3.71	4.19	0.0319	0.9988
			en_to_z	tpZH	1.57	3.00	4.43	5.05	0.0409	0.9567
				tpZL	1.58	2.69	3.81	4.29	0.0319	1.0988
				tpLZ	1.35	2.46	3.58	4.06	0.0319	0.8688
				tpHZ	1.68	3.11	4.54	5.16	0.0409	1.0667
			tn_to_z	tpLZ	1.42	2.53	3.65	4.13	0.0319	0.9388
				tpHZ	1.75	3.18	4.61	5.23	0.0409	1.1367
				tpZH	1.79	3.22	4.65	5.27	0.0409	1.1767
				tpZL	1.80	2.91	4.03	4.51	0.0319	1.3188

bt6
6 mA 3-State Output Buffer

Name: bt6 Description: 6 mA 3-State Output Buffer

Coding Syntax: z=&bt6*(a,en,tn)
z=&bt6od(en,tn)

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*en*	*tn*
bt6	0.5	1.0	0.5
bt6od	-	1.0	0.5
bt6r	0.5	1.0	0.5
bt6rp	0.5	1.0	0.5

Pin Z Input Capacitance: Device(1.7 pF) + pad(0.8 pF) = 2.5 pF

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/D Slots*	*Pads*	*Delay Path*	*Output*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
bt6	1	1	a_to_z	tpLH	1.41	2.36	3.30	3.71	0.0270	1.0038
				tpHL	1.35	2.15	2.95	3.30	0.0229	1.0109
			en_to_z	tpZH	1.48	2.43	3.37	3.78	0.0270	1.0738
				tpZL	1.42	2.22	3.02	3.37	0.0229	1.0809
				tpLZ	1.32	2.12	2.92	3.27	0.0229	0.9809
				tpHZ	1.42	2.37	3.31	3.72	0.0270	1.0138
			tn_to_z	tpLZ	1.61	2.41	3.21	3.56	0.0229	1.2709
				tpHZ	1.71	2.66	3.60	4.01	0.0270	1.3038
				tpZH	1.66	2.61	3.55	3.96	0.0270	1.2538
				tpZL	1.60	2.40	3.20	3.55	0.0229	1.2609
bt6od	1	1	en_to_z	tpLZ	0.35	0.35	0.35	0.35	0.0000	0.3500
				tpZL	0.79	1.59	2.39	2.74	0.0229	0.4509
			tn_to_z	tpLZ	0.75	0.75	0.75	0.75	0.0000	0.7500
				tpZL	1.07	1.87	2.67	3.02	0.0229	0.7309

AC Characteristics: (Cont.)

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/D Slots*	*Pads*	*Delay Path*	*Output*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
bt6r	1	1	a_to_z	tpLH	1.56	2.82	4.08	4.63	0.0360	1.0217
				tpHL	1.44	2.41	3.38	3.80	0.0277	1.0259
			en_to_z	tpZH	1.67	2.93	4.19	4.74	0.0360	1.1317
				tpZL	1.77	2.74	3.71	4.13	0.0277	1.3559
				tpLZ	1.25	2.22	3.19	3.61	0.0277	0.8359
				tpHZ	1.65	2.91	4.17	4.72	0.0360	1.1117
			tn_to_z	tpLZ	1.33	2.30	3.27	3.69	0.0277	0.9159
				tpHZ	1.73	2.99	4.25	4.80	0.0360	1.1917
				tpZH	1.81	3.07	4.33	4.88	0.0360	1.2717
				tpZL	1.91	2.88	3.85	4.27	0.0277	1.4959
bt6rp	1	1	a_to_z	tpLH	1.48	2.55	3.62	4.07	0.0305	1.0245
				tpHL	1.38	2.20	3.03	3.38	0.0236	1.0230
			en_to_z	tpZH	1.53	2.60	3.67	4.12	0.0305	1.0745
				tpZL	1.57	2.39	3.22	3.57	0.0236	1.2130
				tpLZ	1.31	2.13	2.96	3.31	0.0236	0.9530
				tpHZ	1.59	2.66	3.73	4.18	0.0305	1.1345
			tn_to_z	tpLZ	1.38	2.20	3.03	3.38	0.0236	1.0230
				tpHZ	1.66	2.73	3.80	4.25	0.0305	1.2045
				tpZH	1.75	2.82	3.89	4.34	0.0305	1.2945
				tpZL	1.79	2.61	3.44	3.79	0.0236	1.4330

bt8
8 mA 3-State Output Buffer

Name: bt8 Description: 8 mA 3-State Output Buffer

Coding Syntax: z=&bt8*(a,en,tn)
z=&bt8od(en,tn)

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*en*	*tn*
bt8	0.5	1.0	0.5
bt8od	–	1.0	0.5
bt8r	0.5	1.0	0.5
bt8rp	0.5	1.0	0.5

Pin Z Input Capacitance: Device(1.7 pF) + pad(0.8 pF) = 2.5 pF

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/D Slots*	*Pads*	*Delay Path*	*Output*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
bt8	1	1	a_to_z	tpLH	1.36	2.16	2.96	3.31	0.0229	1.0209
				tpHL	1.33	1.96	2.59	2.86	0.0180	1.0559
			en_to_z	tpZH	1.45	2.25	3.05	3.40	0.0229	1.1109
				tpZL	1.42	2.05	2.68	2.95	0.0180	1.1459
				tpLZ	1.33	1.96	2.59	2.86	0.0180	1.0559
				tpHZ	1.46	2.26	3.06	3.41	0.0229	1.1209
			tn_to_z	tpLZ	1.62	2.25	2.88	3.15	0.0180	1.3459
				tpHZ	1.75	2.55	3.35	3.70	0.0229	1.4109
				tpZH	1.63	2.43	3.23	3.58	0.0229	1.2909
				tpZL	1.60	2.23	2.86	3.13	0.0180	1.3259
bt8od	1	1	en_to_z	tpLZ	0.37	0.37	0.37	0.37	0.0000	0.3700
				tpZL	0.77	1.42	2.08	2.36	0.0187	0.4880
			tn_to_z	tpLZ	0.77	0.77	0.77	0.77	0.0000	0.7700
				tpZL	1.05	1.70	2.36	2.64	0.0187	0.7680

AC Characteristics: (Cont.)

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/D Slots*	*Pads*	*Delay Path*	*Output*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
bt8r	1	1	a_to_z	tpLH	1.49	2.51	3.52	3.96	0.0291	1.0502
				tpHL	1.38	2.13	2.88	3.20	0.0215	1.0566
			en_to_z	tpZH	1.59	2.61	3.62	4.06	0.0291	1.1502
				tpZL	1.70	2.45	3.20	3.52	0.0215	1.3766
				tpLZ	1.22	1.97	2.72	3.04	0.0215	0.8966
				tpHZ	1.61	2.63	3.64	4.08	0.0291	1.1702
			tn_to_z	tpLZ	1.30	2.05	2.80	3.12	0.0215	0.9766
				tpHZ	1.69	2.71	3.72	4.16	0.0291	1.2502
				tpZH	1.73	2.75	3.76	4.20	0.0291	1.2902
				tpZL	1.84	2.59	3.34	3.66	0.0215	1.5166
bt8rp	1	1	a_to_z	tpLH	1.42	2.32	3.22	3.60	0.0256	1.0395
				tpHL	1.35	2.06	2.76	3.06	0.0201	1.0523
			en_to_z	tpZH	1.48	2.38	3.28	3.66	0.0256	1.0995
				tpZL	1.55	2.26	2.96	3.26	0.0201	1.2523
				tpLZ	1.25	1.96	2.66	2.96	0.0201	0.9523
				tpHZ	1.52	2.42	3.32	3.70	0.0256	1.1395
			tn_to_z	tpLZ	1.32	2.03	2.73	3.03	0.0201	1.0223
				tpHZ	1.59	2.49	3.39	3.77	0.0256	1.2095
				tpZH	1.70	2.60	3.50	3.88	0.0256	1.3195
				tpZL	1.77	2.48	3.18	3.48	0.0201	1.4723

Name: bt12 Description: 12 mA 3-State Output Buffer

Coding Syntax: z=&bt12*(a,en,tn)
z=&bt12od(en,tn)

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*en*	*tn*
bt12	0.5	1.0	0.5
bt12od	–	1.0	0.5
bt12r	0.5	1.0	0.5
bt12rp	0.5	1.0	0.5

Pin Z Input Capacitance: Device(1.7 pF) + pad(0.8 pF) = 2.5 pF

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/D Slots*	*Pads*	*Delay Path*	*Output*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
bt12	1	1	a_to_z	tpLH	1.36	2.07	2.77	3.07	0.0201	1.0623
				tpHL	1.33	1.89	2.44	2.68	0.0159	1.0894
			en_to_z	tpZH	1.43	2.14	2.84	3.14	0.0201	1.1323
				tpZL	1.40	1.96	2.51	2.75	0.0159	1.1594
				tpLZ	1.39	1.95	2.50	2.74	0.0159	1.1494
				tpHZ	1.50	2.21	2.91	3.21	0.0201	1.2023
			tn_to_z	tpLZ	1.68	2.24	2.79	3.03	0.0159	1.4394
				tpHZ	1.79	2.50	3.20	3.50	0.0201	1.4923
				tpZH	1.61	2.32	3.02	3.32	0.0201	1.3123
				tpZL	1.58	2.14	2.69	2.93	0.0159	1.3394
bt12od	1	1	en_to_z	tpLZ	0.41	0.41	0.41	0.41	0.0000	0.4100
				tpZL	0.77	1.35	1.94	2.18	0.0166	0.5216
			tn_to_z	tpLZ	0.81	0.81	0.81	0.81	0.0000	0.8100
				tpZL	1.05	1.63	2.22	2.46	0.0166	0.8016

AC Characteristics: (Cont.)

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

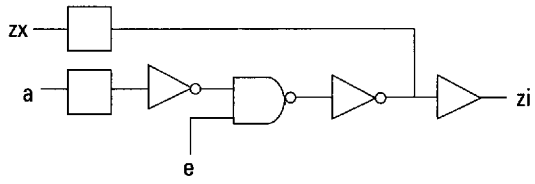
Version	*I/D Slots*	*Pads*	*Delay Path*	*Output*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
bt12r	1	1	a_to_z	tpLH	1.42	2.32	3.22	3.60	0.0256	1.0395
				tpHL	1.37	2.02	2.68	2.96	0.0187	1.0880
			en_to_z	tpZH	1.55	2.45	3.35	3.73	0.0256	1.1695
				tpZL	1.72	2.37	3.03	3.31	0.0187	1.4380
				tpLZ	1.27	1.92	2.58	2.86	0.0187	0.9880
				tpHZ	1.68	2.58	3.48	3.86	0.0256	1.2995
			tn_to_z	tpLZ	1.35	2.00	2.66	2.94	0.0187	1.0680
				tpHZ	1.76	2.66	3.56	3.94	0.0256	1.3795
				tpZH	1.69	2.59	3.49	3.87	0.0256	1.3095
				tpZL	1.86	2.51	3.17	3.45	0.0187	1.5780
bt12rp	1	1	a_to_z	tpLH	1.40	2.20	3.00	3.35	0.0229	1.0609
				tpHL	1.35	1.93	2.52	2.76	0.0166	1.1016
			en_to_z	tpZH	1.46	2.26	3.06	3.41	0.0229	1.1209
				tpZL	1.55	2.13	2.72	2.96	0.0166	1.3016
				tpLZ	1.25	1.83	2.42	2.66	0.0166	1.0016
				tpHZ	1.56	2.36	3.16	3.51	0.0229	1.2209
			tn_to_z	tpLZ	1.32	1.90	2.49	2.73	0.0166	1.0716
				tpHZ	1.63	2.43	3.23	3.58	0.0229	1.2909
				tpZH	1.68	2.48	3.28	3.63	0.0229	1.3409
				tpZL	1.77	2.35	2.94	3.18	0.0166	1.5216

oscim
Oscillator with Enable

Name: oscim Description: Oscillator with Enable
Recommended frequency range: 0.1 MHz to 55 MHz

Coding Syntax: u(zx,zi)=oscim(a,e)

Logic Symbol:



Truth Table:

e	*a*	*zx*	*zi*
1	0	1	0
1	1	0	1
0	x	0	1

Loading Characteristics:

Values stated in standard loads

Version	*e*
oscim	0.5

Pin A Input Capacitance: Device(1.7 pF) + pad(0.8 pF) = 2.5 pF
Pin ZX Output Capacitance: Device(1.7 pF) + pad(0.8 pF) = 2.5 pF

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/O Slots*	*Pads*	*Delay Path*	*Output*	*Standard Loads*						*Slope*	*Incpt*
					50	*100*	*200*	*300*	*400*	*500*		
oscim	1	2	e_to_zi	tpLH	1.37	2.45	4.61	6.76	8.92	11.08	0.0216	0.2962
				tpHL	1.43	2.18	3.67	5.17	6.67	8.17	0.0150	0.6782
			a_to_zi	tpLH	1.37	2.45	4.61	6.76	8.92	11.08	0.0216	0.2962
				tpHL	1.43	2.18	3.67	5.17	6.67	8.17	0.0150	0.6782

AC Characteristics: (Cont.)

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/O Slots*	*Pads*	*Delay Path*	*Output*	*Standard Loads*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
oscim	1	1	e_to_zx	tpLH	0.71	1.00	1.29	1.41	0.0083	0.5856
				tpHL	0.30	0.56	0.81	0.92	0.0073	0.1926
			a_to_zx	tpLH	0.71	1.00	1.29	1.41	0.0083	0.5856
				tpHL	0.30	0.56	0.81	0.92	0.0073	0.1926

3.11 Commercial Output Buffers

This section contains data pages for LCA300K commercial output buffers. These output buffers can be used under commercial conditions only:

WC commercial = 70 °C, 4.75 V

BC commercial = 0 °C, 5.25 V

Commercial output buffers have a voltage output LOW (VOL) of 0.5 V.

These buffers are not suitable for military applications.

Naming Conventions

Commercial output buffer names have the following format:

root_name | drive_strength | input_voltage_level_option | slew_rate_control (optional) | resistors (optional) | other option | a

The type of commercial output buffer being used designates the root name. (See Table 3.6.) The suffix "a" is appended to all commerical output buffer names.

Table 3.6 shows the naming conventions used for commercial output buffers.

Table 3.6 Commercial Output Buffer Naming Conventions

Root Name	*Drive Strength in mA*	*Input Voltage Level Option*[1]	*Slew Rate Control Options*	*Optional Resistors*[2]	*Other Option*[3]
b = Unidirect bd = Bidirect bt = 3-State	24	t = TTL tn = inverted TTL c = CMOS cn = inverted CMOS sc = Schmitt trigger for CMOS scn = Inverting CMOS Schmitt trigger st = Schmitt trigger for TTL stn = inverting TTL Schmitt trigger	none = minimum rp = moderate r = maximum	u = pull-up d = pull-down	od = Open Drain

1. Only bidirect buffers have these options.
2. These resistors are only available for bidirect buffers.
3. Slew rate control and pull-up and pull-down resistors are not available for cells using the open drain option.

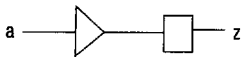
For example, `bd24trua` is a commercial bidirect output buffer with TTL input, maximum slew rate control, and a pull-up resistor.

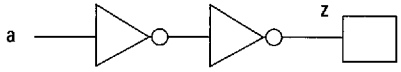
➤ ***Note:*** In the coding syntax, an asterisk following the cell name (for example, `bd24*a`) is a wildcard symbol that replaces options' abbreviations.

Name: b24a Description: 24 mA Unidirect Output Buffer

Coding Syntax: z=&b24*a(a)

Logic Symbol: Schematics:





Loading Characteristics:

Values stated in standard loads.

Version	*a*
b24a	0.5
b24ra	0.5
b24rpa	0.5

Pin Z Input Capacitance: Device(1.2 pF) + pad(0.8 pF) = 2.0 pF

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

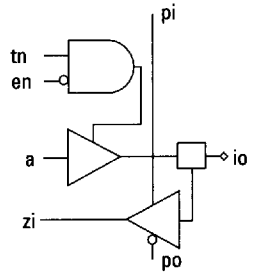
Version	*I/O Slots*	*Pads*	*Delay Path*	*Outputs*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
b24a	1	1	a_to_z	tpLH	1.35	2.03	2.71	3.00	0.0194	1.0602
				tpHL	1.45	2.01	2.56	2.80	0.0159	1.2094
b24ra	1	1	a_to_z	tpLH	1.71	2.61	3.51	3.89	0.0256	1.3295
				tpHL	1.87	2.67	3.47	3.82	0.0229	1.5309
b24rpa	1	1	a_to_z	tpLH	1.82	2.62	3.42	3.77	0.0229	1.4809
				tpHL	2.02	2.82	3.62	3.97	0.0229	1.6809

bd24a
24 mA Bidirect Output Buffer

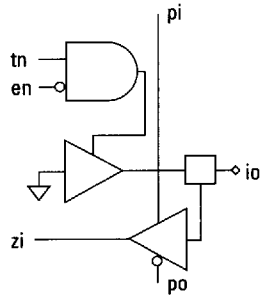
Name: bd24a Description: 24 mA Bidirect Output Buffer

Coding Syntax: u(io,zi,po) = &bd24*a(io,a,en,tn,pi)
u(io,zi,po) = &bd24*oda(io,en,tn,pi)

Logic Symbol: Bidirect Buffer with Slew Rate Control and Optional Pull-up/Pull-down



Bidirect Buffer with Open Drain



Loading Characteristics:

Values stated in standard loads.

Version	*a*	*en*	*tn*	*pi*
bd24*a	0.5	1.0	0.5	0.5
bd24*oda	-	1.0	0.5	0.5
bd24*ra	0.5	1.0	0.5	0.5
bd24*rpa	0.5	1.0	0.5	0.5

Pin IO Input Capacitance: Device(1.7 pF) + pad(0.8 pF) = 2.5 pF

AC Characteristics:

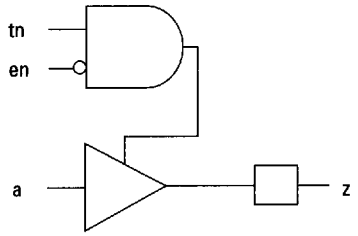
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/D Slots*	*Pads*	*Delay Path*	*Output*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
bd24*a	1	1	a_to_io	tpLH	1.36	2.07	2.77	3.07	0.0201	1.0623
				tpHL	1.33	1.89	2.44	2.68	0.0159	1.0894
			en_to_io	tpZH	1.42	2.13	2.83	3.13	0.0201	1.1223
				tpZL	1.40	1.96	2.51	2.75	0.0159	1.1594
				tpLZ	1.38	1.94	2.49	2.73	0.0159	1.1394
				tpHZ	1.50	2.21	2.91	3.21	0.0201	1.2023
			tn_to_io	tpZH	1.60	2.31	3.01	3.31	0.0201	1.3023
				tpZL	1.58	2.14	2.69	2.93	0.0159	1.3394
				tpLZ	1.63	2.19	2.74	2.98	0.0159	1.3894
				tpHZ	1.75	2.46	3.16	3.46	0.0201	1.4523
bd24*oda	1	1	en_to_io	tpLZ	0.45	0.45	0.45	0.45	0.0000	0.4500
				tpZL	0.75	1.33	1.92	2.16	0.0166	0.5016
			tn_to_io	tpLZ	0.74	0.74	0.74	0.74	0.0000	0.7400
				tpZL	1.04	1.62	2.21	2.45	0.0166	0.7916
bd24*ra	1	1	a_to_io	tpLH	1.42	2.32	3.22	3.60	0.0256	1.0395
				tpHL	1.37	2.02	2.68	2.96	0.0187	1.0880
			en_to_io	tpZH	1.50	2.40	3.30	3.68	0.0256	1.1195
				tpZL	1.52	2.17	2.83	3.11	0.0187	1.2380
				tpLZ	1.27	1.92	2.58	2.86	0.0187	0.9880
				tpHZ	1.53	2.43	3.33	3.71	0.0256	1.1495
			tn_to_io	tpZH	1.69	2.59	3.49	3.87	0.0256	1.3095
				tpZL	1.71	2.36	3.02	3.30	0.0187	1.4280
				tpLZ	1.35	2.00	2.66	2.94	0.0187	1.0680
				tpHZ	1.61	2.51	3.41	3.79	0.0256	1.2295
bd24*rpa	1	1	a_to_io	tpLH	1.40	2.20	3.00	3.35	0.0229	1.0609
				tpHL	1.35	1.93	2.52	2.76	0.0166	1.1016
			en_to_io	tpZH	1.47	2.27	3.07	3.42	0.0229	1.1309
				tpZL	1.49	2.07	2.66	2.90	0.0166	1.2416
				tpLZ	1.39	1.97	2.56	2.80	0.0166	1.1416
				tpHZ	1.63	2.43	3.23	3.58	0.0229	1.2909
			tn_to_io	tpZH	1.65	2.45	3.25	3.60	0.0229	1.3109
				tpZL	1.67	2.25	2.84	3.08	0.0166	1.4216
				tpLZ	1.42	2.00	2.59	2.83	0.0166	1.1716
				tpHZ	1.66	2.46	3.26	3.61	0.0229	1.3209

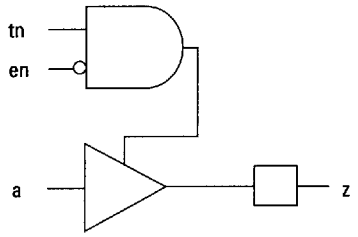
Name: bt24a Description: 24 mA 3-State Output Buffer

Coding Syntax: z=&bt24*a(a,en,tn)
z=&bt24oda(en,tn)

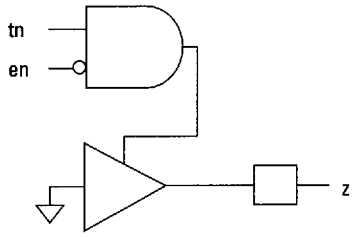
Logic Symbol: 3-State Buffer with Slew Rate Control



3-State Buffer with Slew Rate Control and Optional Pull-up/Pull-down



3-State Buffer with Open Drain



Loading Characteristics:

Values stated in standard loads.

Version	*a*	*en*	*tn*
bt24a	0.5	1.0	0.5
bt24oda	-	1.0	0.5
bt24ra	0.5	1.0	0.5
bt24rpa	0.5	1.0	0.5

Pin Z Input Capacitance: Device(1.2 pF) + pad(0.8 pF) = 20 pF

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/D Slots*	*Pads*	*Delay Path*	*Output*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
bt24a	1	1	a_to_z	tpLH	1.36	2.07	2.77	3.07	0.0201	1.0623
				tpHL	1.33	1.89	2.44	2.68	0.0159	1.0894
			en_to_z	tpZH	1.42	2.13	2.83	3.13	0.0201	1.1223
				tpZL	1.40	1.96	2.51	2.75	0.0159	1.1594
				tpLZ	1.38	1.94	2.49	2.73	0.0159	1.1394
				tpHZ	1.50	2.21	2.91	3.21	0.0201	1.2023
			tn_to_z	tpLZ	1.63	2.19	2.74	2.98	0.0159	1.3894
				tpHZ	1.75	2.46	3.16	3.46	0.0201	1.4523
				tpZH	1.60	2.31	3.01	3.31	0.0201	1.3023
				tpZL	1.58	2.14	2.69	2.93	0.0159	1.3394
bt24oda	1	1	en_to_z	tpLZ	0.41	0.41	0.41	0.41	0.0000	0.4100
				tpZL	0.75	1.33	1.92	2.16	0.0166	0.5016
			tn_to_z	tpLZ	0.79	0.79	0.79	0.79	0.0000	0.7900
				tpZL	1.04	1.62	2.21	2.45	0.0166	0.7916
bt24ra	1	1	a_to_z	tpLH	1.42	2.32	3.22	3.60	0.0256	1.0395
				tpHL	1.37	2.02	2.68	2.96	0.0187	1.0880
			en_to_z	tpZH	1.50	2.40	3.30	3.68	0.0256	1.1195
				tpZL	1.52	2.17	2.83	3.11	0.0187	1.2380
				tpLZ	1.27	1.92	2.58	2.86	0.0187	0.9880
				tpHZ	1.53	2.43	3.33	3.71	0.0256	1.1495
			tn_to_z	tpLZ	1.35	2.00	2.66	2.94	0.0187	1.0680
				tpHZ	1.61	2.51	3.41	3.79	0.0256	1.2295
				tpZH	1.69	2.59	3.49	3.87	0.0256	1.3095
				tpZL	1.71	2.36	3.02	3.30	0.0187	1.4280
bt24rpa	1	1	a_to_z	tpLH	1.40	2.20	3.00	3.35	0.0229	1.0609
				tpHL	1.35	1.93	2.52	2.76	0.0166	1.1016
			en_to_z	tpZH	1.47	2.27	3.07	3.42	0.0229	1.1309
				tpZL	1.49	2.07	2.66	2.90	0.0166	1.2416
				tpLZ	1.39	1.97	2.56	2.80	0.0166	1.1416
				tpHZ	1.63	2.43	3.23	3.58	0.0229	1.2909
			tn_to_z	tpLZ	1.42	2.00	2.59	2.83	0.0166	1.1716
				tpHZ	1.66	2.46	3.26	3.61	0.0229	1.3209
				tpZH	1.65	2.45	3.25	3.60	0.0229	1.3109
				tpZL	1.67	2.25	2.84	3.08	0.0166	1.4216

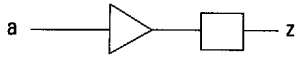
b1l/b2l

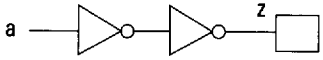
1 mA/2 mA 3.3 V Unidirect Output Buffer

Name: b1l/b2l Description: 1 mA/2 mA 3.3 V Unidirect Output Buffer

Coding Syntax: z=&b1/b2l(a)

Logic Symbol: Schematics:





Loading Characteristics:

Values stated in standard loads.

Version	*a*
b1l	0.5
b2l	0.5

Pin Z Output Capacitance: Device(1.2 pF) + pad(0.8 pF) = 2.0 pF

AC Characteristics:

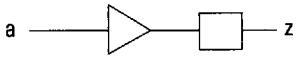
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

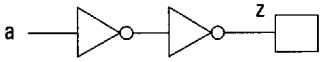
Version	*I/O Slots*	*Pads*	*Delay Path*	*Outputs*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
b1l	1	1	a_to_z	tpLH	2.81	7.17	11.54	13.41	0.1247	0.9367
				tpHL	1.30	2.66	4.02	4.60	0.0388	0.7203
b2l	1	1	a_to_z	tpLH	2.32	5.60	8.87	10.28	0.0936	0.9200
				tpHL	1.21	2.31	3.40	3.87	0.0312	0.7467

Name: b4l Description: 4 mA 3.3 V Unidirect Output Buffer

Coding Syntax: z=&b4*l(a)

Logic Symbol: Schematics:





Loading Characteristics:

Values stated in standard loads.

Version	*a*
b4l	0.5
b4rl	0.5
b4rpl	0.5

Pin Z Output Capacitance: Device(1.2 pF) + pad(0.8 pF) = 2.0 pF

AC Characteristics:

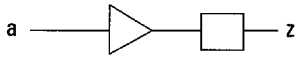
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/O Slots*	*Pads*	*Delay Path*	*Outputs*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
b4l	1	1	a_to_z	tpLH	1.71	3.48	5.25	6.01	0.0506	0.9468
				tpHL	1.14	1.77	2.40	2.67	0.0180	0.8659
b4rl	1	1	a_to_z	tpLH	2.24	4.57	6.90	7.90	0.0665	1.2462
				tpHL	1.49	2.27	3.04	3.38	0.0222	1.1587
b4rpl	1	1	a_to_z	tpLH	2.24	4.35	6.46	7.37	0.0603	1.3369
				tpHL	1.59	2.31	3.04	3.35	0.0208	1.2744

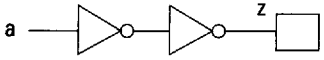
Name: b6l Description: 6 mA 3.3 V Unidirect Output Buffer

Coding Syntax: z=&b6*l(a)

Logic Symbol:



Schematics:



Loading Characteristics:

Values stated in standard loads.

Version	*a*
b6l	1.0
b6rl	1.0
b6rpl	1.0

Pin Z Output Capacitance: Device(2.2 pF) + pad(0.8 pF) = 3.0 pF

AC Characteristics:

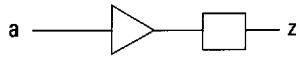
VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

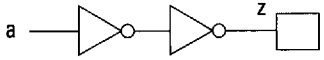
Version	*I/O Slots*	*Pads*	*Delay Path*	*Outputs*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
b6l	2	1	a_to_z	tpLH	1.38	2.55	3.71	4.21	0.0333	0.8831
				tpHL	1.00	1.42	1.83	2.00	0.0118	0.8265
b6rl	2	1	a_to_z	tpLH	1.79	3.35	4.90	5.56	0.0444	1.1275
				tpHL	1.30	1.86	2.41	2.65	0.0159	1.0594
b6rpl	2	1	a_to_z	tpLH	1.81	3.17	4.53	5.11	0.0388	1.2303
				tpHL	1.37	1.88	2.39	2.61	0.0146	1.1551

Name: b8l Description: 8 mA 3.3 V Unidirect Output Buffer

Coding Syntax: z=&b8*l(a)

Logic Symbol: Schematics:





Loading Characteristics:

Values stated in standard loads.

Version	*a*
b8l	1.0
b8rl	1.0
b8rpl	1.0

Pin Z Output Capacitance: Device(2.2 pF) + pad(0.8 pF) = 3.0 pF

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

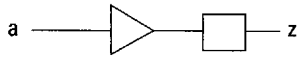
Version	*I/O Slots*	*Pads*	*Delay Path*	*Outputs*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
b8l	2	1	a_to_z	tpLH	1.29	2.19	3.09	3.47	0.0256	0.9095
				tpHL	1.02	1.34	1.65	1.79	0.0090	0.8879
b8rl	2	1	a_to_z	tpLH	1.70	2.91	4.12	4.64	0.0346	1.1774
				tpHL	1.29	1.72	2.16	2.35	0.0125	1.0987
b8rpl	2	1	a_to_z	tpLH	1.75	2.86	3.98	4.46	0.0319	1.2688
				tpHL	1.37	1.79	2.20	2.37	0.0118	1.1965

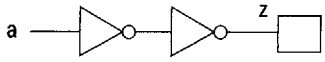
b12l
12 mA 3.3 V Unidirect Output Buffer

Name: b12l Description: 12 mA 3.3 V Unidirect Output Buffer

Coding Syntax: z=&b12*l(a)

Logic Symbol: Schematics:





Loading Characteristics:

Values stated in standard loads.

Version	*a*
b12l	1.5
b12rl	1.5
b12rpl	1.5

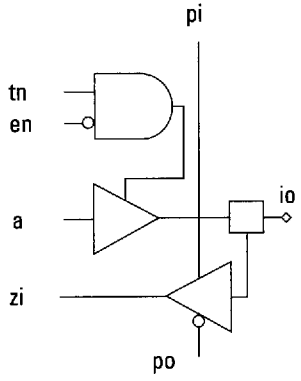
Pin Z Output Capacitance: Device(3.2 pF) + pad(0.8 pF) = 4.0 pF

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

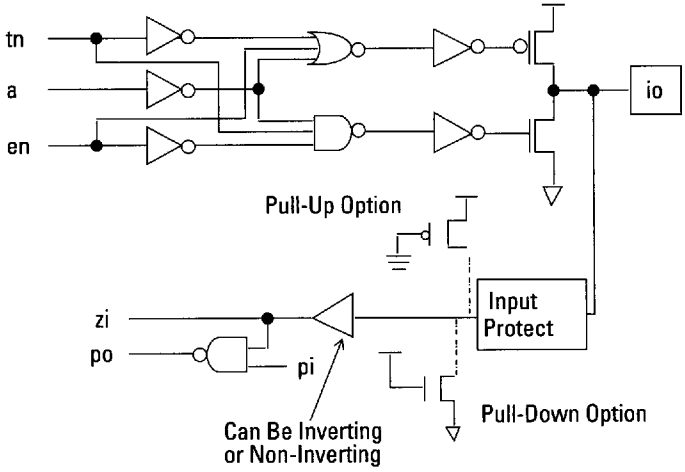
Version	*I/O Slots*	*Pads*	*Delay Path*	*Outputs*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
b12l	3	1	a_to_z	tpLH	1.16	1.77	2.38	2.64	0.0173	0.9037
				tpHL	0.98	1.20	1.42	1.51	0.0062	0.8893
b12rl	3	1	a_to_z	tpLH	1.50	2.35	3.20	3.56	0.0243	1.1352
				tpHL	1.19	1.51	1.82	1.96	0.0090	1.0579
b12rpl	3	1	a_to_z	tpLH	1.56	2.36	3.16	3.51	0.0229	1.2209
				tpHL	1.26	1.58	1.89	2.03	0.0090	1.1279

Bidirect Output Buffer Logic Symbol

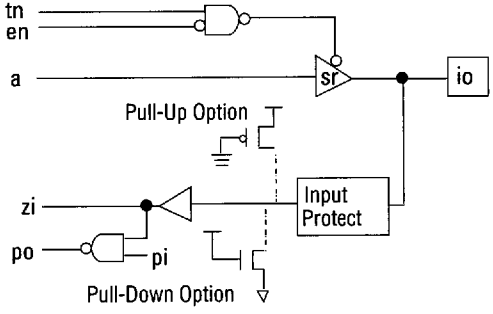


Bidirect Output Buffer Schematics

Bidirect Buffer with Optional Pull-up/Pull-down resistors



Bidirect Buffer with Slew Rate Control and Optional Pull-up/Pull-down



1 mA 3.3 V Bidirect Output Buffer

Name: bd1l Description: 1 mA 3.3 V Bidirect Output Buffer

Coding Syntax: u(io,zi,po) = &bd1*l(io,a,en,tn,pi)

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*en*	*tn*	*pi*
bd1*l	0.5	1.0	0.5	0.5

Pin IO Input Capacitance: Device(1.7 pF) + pad(0.8 pF) = 2.5 pF

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/D Slots*	*Pads*	*Delay Path*	*Output*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
bd1*l	1	1	a_to_io	tpLH	2.89	7.25	11.62	13.49	0.1247	1.0167
				tpHL	1.31	2.67	4.03	4.61	0.0388	0.7303
			en_to_io	tpZH	3.07	7.43	11.80	13.67	0.1247	1.1967
				tpZL	1.51	2.87	4.23	4.81	0.0388	0.9303
				tpLZ	1.22	2.58	3.94	4.52	0.0388	0.6403
				tpHZ	2.78	7.14	11.51	13.38	0.1247	0.9067
			tn_to_io	tpZH	3.15	7.51	11.88	13.75	0.1247	1.2767
				tpZL	1.59	2.95	4.31	4.89	0.0388	1.0103
				tpLZ	1.27	2.63	3.99	4.57	0.0388	0.6903
				tpHZ	2.83	7.19	11.56	13.43	0.1247	0.9567

Name: bd2l Description: 2 mA 3.3 V Bidirect Output Buffer

Coding Syntax: u(io,zi,po) = &bd2*l(io,a,en,tn,pi)

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*en*	*tn*	*pi*
bd2*l	0.5	1.0	0.5	0.5

Pin IO Input Capacitance: Device(1.7 pF) + pad(0.8 pF) = 2.5 pF

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/D Slots*	*Pads*	*Delay Path*	*Output*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
bd2*l	1	1	a_to_io	tpLH	2.40	5.68	8.95	10.36	0.0936	1.0000
				tpHL	1.34	2.70	4.06	4.64	0.0388	0.7603
			en_to_io	tpZH	2.57	5.85	9.12	10.53	0.0936	1.1700
				tpZL	1.53	2.89	4.25	4.83	0.0388	0.9503
				tpLZ	1.32	2.68	4.04	4.62	0.0388	0.7403
				tpHZ	2.26	5.54	8.81	10.22	0.0936	0.8600
			tn_to_io	tpZH	2.65	5.93	9.20	10.61	0.0936	1.2500
				tpZL	1.61	2.97	4.33	4.91	0.0388	1.0303
				tpLZ	1.37	2.73	4.09	4.67	0.0388	0.7903
				tpHZ	2.31	5.59	8.86	10.27	0.0936	0.9100

Name: bd4l Description: 4 mA 3.3 V Bidirect Output Buffer

Coding Syntax: u(io,zi,po) = &bd4*l(io,a,en,tn,pi)

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*en*	*tn*	*pi*
bd4*l	0.5	1.0	0.5	0.5

Pin IO Input Capacitance: Device(1.7 pF) + pad(0.8 pF) = 2.5 pF

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/D Slots*	*Pads*	*Delay Path*	*Output*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
bd4*l	1	1	a_to_io	tpLH	1.81	3.60	5.40	6.17	0.0513	1.0390
				tpHL	1.07	1.70	2.33	2.60	0.0180	0.7959
			en_to_io	tpZH	1.99	3.78	5.58	6.35	0.0513	1.2190
				tpZL	1.27	1.90	2.53	2.80	0.0180	0.9959
				tpLZ	1.16	1.79	2.42	2.69	0.0180	0.8859
				tpHZ	1.64	3.43	5.23	6.00	0.0513	0.8690
			tn_to_io	tpZH	2.07	3.86	5.66	6.43	0.0513	1.2990
				tpZL	1.35	1.98	2.61	2.88	0.0180	1.0759
				tpLZ	1.21	1.84	2.47	2.74	0.0180	0.9359
				tpHZ	1.69	3.48	5.28	6.05	0.0513	0.9190
bd4*rl	1	1	a_to_io	tpLH	2.10	4.43	6.76	7.76	0.0665	1.1062
				tpHL	1.16	1.87	2.57	2.87	0.0201	0.8623
			en_to_io	tpZH	2.26	4.59	6.92	7.92	0.0665	1.2662
				tpZL	1.45	2.16	2.86	3.16	0.0201	1.1523
				tpLZ	1.08	1.79	2.49	2.79	0.0201	0.7823
				tpHZ	1.95	4.28	6.61	7.61	0.0665	0.9562
			tn_to_io	tpZH	2.36	4.69	7.02	8.02	0.0665	1.3662
				tpZL	1.55	2.26	2.96	3.26	0.0201	1.2523
				tpLZ	1.13	1.84	2.54	2.84	0.0201	0.8323
				tpHZ	2.00	4.33	6.66	7.66	0.0665	1.0062

AC Characteristics: (Cont.)

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/D Slots*	*Pads*	*Delay Path*	*Output*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
bd4*rpl	1	1	a_to_io	tpLH	2.05	4.13	6.22	7.11	0.0596	1.1548
				tpHL	1.13	1.78	2.44	2.72	0.0187	0.8480
			en_to_io	tpZH	2.19	4.27	6.36	7.25	0.0596	1.2948
				tpZL	1.31	1.96	2.62	2.90	0.0187	1.0280
				tpLZ	1.33	1.98	2.64	2.92	0.0187	1.0480
				tpHZ	1.93	4.01	6.10	6.99	0.0596	1.0348
			tn_to_io	tpZH	2.30	4.38	6.47	7.36	0.0596	1.4048
				tpZL	1.42	2.07	2.73	3.01	0.0187	1.1380
				tpLZ	1.39	2.04	2.70	2.98	0.0187	1.1080
				tpHZ	1.99	4.07	6.16	7.05	0.0596	1.0948

Name: bd6l Description: 6 mA 3.3 V Bidirect Output Buffer

Coding Syntax: u(io,zi,po) = &bd6*l(io,a,en,tn,pi)

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*en*	*tn*	*pi*
bd6*l	1.0	1.9	1.0	0.5

Pin IO Input Capacitance: Device(2.7 pF) + pad(0.8 pF) = 3.5 pF

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/D Slots*	*Pads*	*Delay Path*	*Output*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
bd6*l	2	1	a_to_io	tpLH	1.48	2.65	3.81	4.31	0.0333	0.9831
				tpHL	0.98	1.41	1.85	2.04	0.0125	0.7887
			en_to_io	tpZH	1.65	2.82	3.98	4.48	0.0333	1.1531
				tpZL	1.16	1.59	2.03	2.22	0.0125	0.9687
				tpLZ	1.08	1.51	1.95	2.14	0.0125	0.8887
				tpHZ	1.33	2.50	3.66	4.16	0.0333	0.8331
			tn_to_io	tpZH	1.74	2.91	4.07	4.57	0.0333	1.2431
				tpZL	1.25	1.68	2.12	2.31	0.0125	1.0587
				tpLZ	1.12	1.55	1.99	2.18	0.0125	0.9287
				tpHZ	1.37	2.54	3.70	4.20	0.0333	0.8731
bd6*rl	2	1	a_to_io	tpLH	1.69	3.22	4.75	5.40	0.0437	1.0353
				tpHL	1.04	1.53	2.01	2.22	0.0139	0.8330
			en_to_io	tpZH	1.85	3.38	4.91	5.56	0.0437	1.1953
				tpZL	1.35	1.84	2.32	2.53	0.0139	1.1430
				tpLZ	1.01	1.50	1.98	2.19	0.0139	0.8030
				tpHZ	1.59	3.12	4.65	5.30	0.0437	0.9353
			tn_to_io	tpZH	1.95	3.48	5.01	5.66	0.0437	1.2953
				tpZL	1.45	1.94	2.42	2.63	0.0139	1.2430
				tpLZ	1.03	1.52	2.00	2.21	0.0139	0.8230
				tpHZ	1.61	3.14	4.67	5.32	0.0437	0.9553

AC Characteristics: (Cont.)

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/D Slots*	*Pads*	*Delay Path*	*Output*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
bd6*rpl	2	1	a_to_io	tpLH	1.65	2.98	4.32	4.89	0.0381	1.0782
				tpHL	1.02	1.45	1.89	2.08	0.0125	0.8287
			en_to_io	tpZH	1.79	3.12	4.46	5.03	0.0381	1.2182
				tpZL	1.20	1.63	2.07	2.26	0.0125	1.0087
				tpLZ	1.24	1.67	2.11	2.30	0.0125	1.0487
				tpHZ	1.57	2.90	4.24	4.81	0.0381	0.9982
			tn_to_io	tpZH	1.89	3.22	4.56	5.13	0.0381	1.3182
				tpZL	1.30	1.73	2.17	2.36	0.0125	1.1087
				tpLZ	1.30	1.73	2.17	2.36	0.0125	1.1087
				tpHZ	1.63	2.96	4.30	4.87	0.0381	1.0582

bd8l
8 mA 3.3 V Bidirect Output Buffer

Name: bd8l Description: 8 mA 3.3 V Bidirect Output Buffer

Coding Syntax: u(io,zi,po) = &bd8*l(io,a,en,tn,pi)

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*en*	*tn*	*pi*
bd8*l	1.0	1.9	1.0	0.5

Pin IO Input Capacitance: Device(2.7 pF) + pad(0.8 pF) = 3.5 pF

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/D Slots*	*Pads*	*Delay Path*	*Output*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
bd8*l	2	1	a_to_io	tpLH	1.39	2.31	3.23	3.63	0.0263	0.9916
				tpHL	0.94	1.26	1.57	1.71	0.0090	0.8079
			en_to_io	tpZH	1.57	2.49	3.41	3.81	0.0263	1.1716
				tpZL	1.13	1.45	1.76	1.90	0.0090	0.9979
				tpLZ	1.03	1.35	1.66	1.80	0.0090	0.8979
				tpHZ	1.23	2.15	3.07	3.47	0.0263	0.8316
			tn_to_io	tpZH	1.66	2.58	3.50	3.90	0.0263	1.2616
				tpZL	1.22	1.54	1.85	1.99	0.0090	1.0879
				tpLZ	1.07	1.39	1.70	1.84	0.0090	0.9379
				tpHZ	1.27	2.19	3.11	3.51	0.0263	0.8716
bd8*rl	2	1	a_to_io	tpLH	1.57	2.76	3.95	4.46	0.0340	1.0653
				tpHL	1.00	1.36	1.73	1.88	0.0104	0.8422
			en_to_io	tpZH	1.73	2.92	4.11	4.62	0.0340	1.2253
				tpZL	1.31	1.67	2.04	2.19	0.0104	1.1522
				tpLZ	1.01	1.37	1.74	1.89	0.0104	0.8522
				tpHZ	1.43	2.62	3.81	4.32	0.0340	0.9253
			tn_to_io	tpZH	1.83	3.02	4.21	4.72	0.0340	1.3253
				tpZL	1.41	1.77	2.14	2.29	0.0104	1.2522
				tpLZ	1.03	1.39	1.76	1.91	0.0104	0.8722
				tpHZ	1.45	2.64	3.83	4.34	0.0340	0.9453

AC Characteristics: (Cont.)

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/D Slots*	*Pads*	*Delay Path*	*Output*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
bd8*rpl	2	1	a_to_io	tpLH	1.55	2.65	3.74	4.21	0.0312	1.0867
				tpHL	1.00	1.34	1.67	1.82	0.0097	0.8501
			en_to_io	tpZH	1.70	2.80	3.89	4.36	0.0312	1.2367
				tpZL	1.19	1.53	1.86	2.01	0.0097	1.0401
				tpLZ	1.21	1.55	1.88	2.03	0.0097	1.0601
				tpHZ	1.46	2.56	3.65	4.12	0.0312	0.9967
			tn_to_io	tpZH	1.80	2.90	3.99	4.46	0.0312	1.3367
				tpZL	1.29	1.63	1.96	2.11	0.0097	1.1401
				tpLZ	1.27	1.61	1.94	2.09	0.0097	1.1201
				tpHZ	1.52	2.62	3.71	4.18	0.0312	1.0567

Name: bd12l Description: 12 mA 3.3 V Bidirect Output Buffer

Coding Syntax: u(io,zi,po) = &bd12*l(io,a,en,tn,pi)

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*en*	*tn*	*pi*
bd12*l	1.5	2.7	1.5	0.5

Pin IO Input Capacitance: Device(3.7 pF) + pad(0.8 pF) = 4.5 pF

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

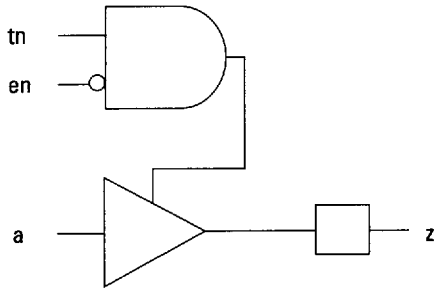
Version	*I/D Slots*	*Pads*	*Delay Path*	*Output*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
bd12*l	3	1	a_to_io	tpLH	1.25	1.88	2.51	2.78	0.0180	0.9759
				tpHL	0.89	1.11	1.33	1.42	0.0062	0.7993
			en_to_io	tpZH	1.43	2.06	2.69	2.96	0.0180	1.1559
				tpZL	1.08	1.30	1.52	1.61	0.0062	0.9893
				tpLZ	1.00	1.22	1.44	1.53	0.0062	0.9093
				tpHZ	1.09	1.72	2.35	2.62	0.0180	0.8159
			tn_to_io	tpZH	1.52	2.15	2.78	3.05	0.0180	1.2459
				tpZL	1.17	1.39	1.61	1.70	0.0062	1.0793
				tpLZ	1.04	1.26	1.48	1.57	0.0062	0.9493
				tpHZ	1.13	1.76	2.39	2.66	0.0180	0.8559
bd12*rl	3	1	a_to_io	tpLH	1.36	2.18	3.01	3.36	0.0236	1.0030
				tpHL	0.99	1.23	1.47	1.57	0.0069	0.8815
			en_to_io	tpZH	1.55	2.37	3.20	3.55	0.0236	1.1930
				tpZL	1.19	1.43	1.67	1.77	0.0069	1.0815
				tpLZ	1.04	1.28	1.52	1.62	0.0069	0.9315
				tpHZ	1.28	2.10	2.93	3.28	0.0236	0.9230
			tn_to_io	tpZH	1.66	2.48	3.31	3.66	0.0236	1.3030
				tpZL	1.30	1.54	1.78	1.88	0.0069	1.1915
				tpLZ	1.08	1.32	1.56	1.66	0.0069	0.9715
				tpHZ	1.32	2.14	2.97	3.32	0.0236	0.9630

AC Characteristics: (Cont.)

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

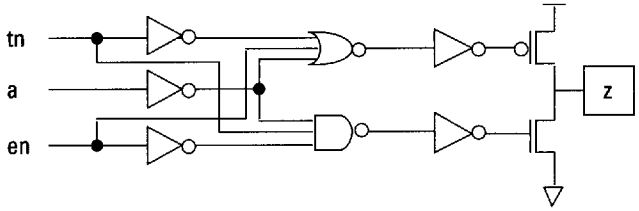
Version	*I/D Slots*	*Pads*	*Delay Path*	*Output*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
bd12*rpl	3	1	a_to_io	tpLH	1.38	2.16	2.93	3.27	0.0222	1.0487
				tpHL	0.94	1.18	1.42	1.52	0.0069	0.8315
			en_to_io	tpZH	1.54	2.32	3.09	3.43	0.0222	1.2087
				tpZL	1.11	1.35	1.59	1.69	0.0069	1.0015
				tpLZ	1.19	1.43	1.67	1.77	0.0069	1.0815
				tpHZ	1.30	2.08	2.85	3.19	0.0222	0.9687
			tn_to_io	tpZH	1.65	2.43	3.20	3.54	0.0222	1.3187
				tpZL	1.22	1.46	1.70	1.80	0.0069	1.1115
				tpLZ	1.25	1.49	1.73	1.83	0.0069	1.1415
				tpHZ	1.36	2.14	2.91	3.25	0.0222	1.0287

3-State Output Buffer Logic Symbol

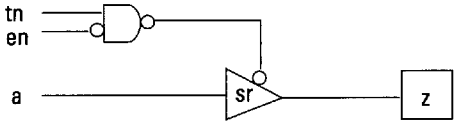


3-State Output Buffer Schematics

3-State Buffer



3-State Buffer with Slew Rate Control



Name: bt1l Description: 1 mA 3.3 V 3-State Output Buffer

Coding Syntax: z=&bt1l(a,en,tn)

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*en*	*tn*
bt1l	0.5	1.0	0.5

Pin Z Output Capacitance: Device(1.2 pF) + pad(0.8 pF) = 2.0 pF

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/D Slots*	*Pads*	*Delay Path*	*Output*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
bt1l	1	1	a_to_z	tpLH	2.89	7.25	11.62	13.49	0.1247	1.0167
				tpHL	1.31	2.67	4.03	4.61	0.0388	0.7303
			en_to_z	tpZH	3.07	7.43	11.80	13.67	0.1247	1.1967
				tpZL	1.51	2.87	4.23	4.81	0.0388	0.9303
				tpLZ	1.22	2.58	3.94	4.52	0.0388	0.6403
				tpHZ	2.78	7.14	11.51	13.38	0.1247	0.9067
			tn_to_z	tpLZ	1.27	2.63	3.99	4.57	0.0388	0.6903
				tpHZ	2.83	7.19	11.56	13.43	0.1247	0.9567
				tpZH	3.15	7.51	11.88	13.75	0.1247	1.2767
				tpZL	1.59	2.95	4.31	4.89	0.0388	1.0103

bt2l
2 mA 3.3 V 3-State Output Buffer

Name: bt2l Description: 2 mA 3.3 V 3-State Output Buffer

Coding Syntax: z =&bt2l(a,en,tn)

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*en*	*tn*
bt2l	0.5	1.0	0.5

Pin Z Output Capacitance: Device(1.2 pF) + pad(0.8 pF) = 2.0 pF

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/D Slots*	*Pads*	*Delay Path*	*Output*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
bt2l	1	1	a_to_z	tpLH	2.40	5.68	8.95	10.36	0.0936	1.0000
				tpHL	1.34	2.70	4.06	4.64	0.0388	0.7603
			en_to_z	tpZH	2.57	5.85	9.12	10.53	0.0936	1.1700
				tpZL	1.53	2.89	4.25	4.83	0.0388	0.9503
				tpLZ	1.32	2.68	4.04	4.62	0.0388	0.7403
				tpHZ	2.26	5.54	8.81	10.22	0.0936	0.8600
			tn_to_z	tpLZ	1.37	2.73	4.09	4.67	0.0388	0.7903
				tpHZ	2.31	5.59	8.86	10.27	0.0936	0.9100
				tpZH	2.65	5.93	9.20	10.61	0.0936	1.2500
				tpZL	1.61	2.97	4.33	4.91	0.0388	1.0303

Name: bt4l Description: 4 mA 3.3 V 3-State Output Buffer

Coding Syntax: z=&bt4*l(a,en,tn)

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*en*	*tn*
bt4l	0.5	1.0	0.5

Pin Z Output Capacitance: Device(1.2 pF) + pad(0.8 pF) = 2.0 pF

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/D Slots*	*Pads*	*Delay Path*	*Output*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
bt4l	1	1	a_to_z	tpLH	1.81	3.60	5.40	6.17	0.0513	1.0390
				tpHL	1.07	1.70	2.33	2.60	0.0180	0.7959
			en_to_z	tpZH	1.99	3.78	5.58	6.35	0.0513	1.2190
				tpZL	1.27	1.90	2.53	2.80	0.0180	0.9959
				tpLZ	1.16	1.79	2.42	2.69	0.0180	0.8859
				tpHZ	1.64	3.43	5.23	6.00	0.0513	0.8690
			tn_to_z	tpLZ	1.21	1.84	2.47	2.74	0.0180	0.9359
				tpHZ	1.69	3.48	5.28	6.05	0.0513	0.9190
				tpZH	2.07	3.86	5.66	6.43	0.0513	1.2990
				tpZL	1.35	1.98	2.61	2.88	0.0180	1.0759
bt4rl	1	1	a_to_z	tpLH	2.10	4.43	6.76	7.76	0.0665	1.1062
				tpHL	1.16	1.87	2.57	2.87	0.0201	0.8623
			en_to_z	tpZH	2.26	4.59	6.92	7.92	0.0665	1.2662
				tpZL	1.45	2.16	2.86	3.16	0.0201	1.1523
				tpLZ	1.08	1.79	2.49	2.79	0.0201	0.7823
				tpHZ	1.95	4.28	6.61	7.61	0.0665	0.9562
			tn_to_z	tpLZ	1.13	1.84	2.54	2.84	0.0201	0.8323
				tpHZ	2.00	4.33	6.66	7.66	0.0665	1.0062
				tpZH	2.36	4.69	7.02	8.02	0.0665	1.3662
				tpZL	1.55	2.26	2.96	3.26	0.0201	1.2523

AC Characteristics: (Cont.)

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/D Slots*	*Pads*	*Delay Path*	*Output*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
bt4rpl	1	1	a_to_z	tpLH	2.05	4.13	6.22	7.11	0.0596	1.1548
				tpHL	1.13	1.78	2.44	2.72	0.0187	0.8480
			en_to_z	tpZH	2.19	4.27	6.36	7.25	0.0596	1.2948
				tpZL	1.31	1.96	2.62	2.90	0.0187	1.0280
				tpLZ	1.33	1.98	2.64	2.92	0.0187	1.0480
				tpHZ	1.93	4.01	6.10	6.99	0.0596	1.0348
			tn_to_z	tpLZ	1.39	2.04	2.70	2.98	0.0187	1.1080
				tpHZ	1.99	4.07	6.16	7.05	0.0596	1.0948
				tpZH	2.30	4.38	6.47	7.36	0.0596	1.4048
				tpZL	1.42	2.07	2.73	3.01	0.0187	1.1380

Name: bt6l Description: 6 mA 3.3 V 3-State Output Buffer

Coding Syntax: z=&bt6*l(a,en,tn)

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*en*	*tn*
bt6l	1.0	1.9	1.0

Pin Z Output Capacitance: Device(2.2 pF) + pad(0.8 pF) = 3.0 pF

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/O Slots*	*Pads*	*Delay Path*	*Output*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
bt6l	2	1	a_to_z	tpLH	1.48	2.65	3.81	4.31	0.0333	0.9831
				tpHL	0.98	1.41	1.85	2.04	0.0125	0.7887
			en_to_z	tpZH	1.65	2.82	3.98	4.48	0.0333	1.1531
				tpZL	1.16	1.59	2.03	2.22	0.0125	0.9687
				tpLZ	1.08	1.51	1.95	2.14	0.0125	0.8887
				tpHZ	1.33	2.50	3.66	4.16	0.0333	0.8331
			tn_to_z	tpLZ	1.12	1.55	1.99	2.18	0.0125	0.9287
				tpHZ	1.37	2.54	3.70	4.20	0.0333	0.8731
				tpZH	1.74	2.91	4.07	4.57	0.0333	1.2431
				tpZL	1.25	1.68	2.12	2.31	0.0125	1.0587
bt6rl	2	1	a_to_z	tpLH	1.69	3.22	4.75	5.40	0.0437	1.0353
				tpHL	1.04	1.53	2.01	2.22	0.0139	0.8330
			en_to_z	tpZH	1.85	3.38	4.91	5.56	0.0437	1.1953
				tpZL	1.35	1.84	2.32	2.53	0.0139	1.1430
				tpLZ	1.01	1.50	1.98	2.19	0.0139	0.8030
				tpHZ	1.59	3.12	4.65	5.30	0.0437	0.9353
			tn_to_z	tpLZ	1.03	1.52	2.00	2.21	0.0139	0.8230
				tpHZ	1.61	3.14	4.67	5.32	0.0437	0.9553
				tpZH	1.95	3.48	5.01	5.66	0.0437	1.2953
				tpZL	1.45	1.94	2.42	2.63	0.0139	1.2430

AC Characteristics: (Cont.)

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/D Slots*	*Pads*	*Delay Path*	*Output*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
bt6rpl	2	1	a_to_z	tpLH	1.65	2.98	4.32	4.89	0.0381	1.0782
				tpHL	1.02	1.45	1.89	2.08	0.0125	0.8287
			en_to_z	tpZH	1.79	3.12	4.46	5.03	0.0381	1.2182
				tpZL	1.20	1.63	2.07	2.26	0.0125	1.0087
				tpLZ	1.24	1.67	2.11	2.30	0.0125	1.0487
				tpHZ	1.57	2.90	4.24	4.81	0.0381	0.9982
			tn_to_z	tpLZ	1.30	1.73	2.17	2.36	0.0125	1.1087
				tpHZ	1.63	2.96	4.30	4.87	0.0381	1.0582
				tpZH	1.89	3.22	4.56	5.13	0.0381	1.3182
				tpZL	1.30	1.73	2.17	2.36	0.0125	1.1087

Name: bt8l Description: 8 mA 3.3 V 3-State Output Buffer

Coding Syntax: z=&bt8*l(a,en,tn)

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*en*	*tn*
bt8l	1.0	1.9	1.0

Pin Z Output Capacitance: Device(2.2 pF) + pad(0.8 pF) = 3.0 pF

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/D Slots*	*Pads*	*Delay Path*	*Output*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
bt8l	2	1	a_to_z	tpLH	1.39	2.31	3.23	3.63	0.0263	0.9916
				tpHL	0.94	1.26	1.57	1.71	0.0090	0.8079
			en_to_z	tpZH	1.57	2.49	3.41	3.81	0.0263	1.1716
				tpZL	1.13	1.45	1.76	1.90	0.0090	0.9979
				tpLZ	1.03	1.35	1.66	1.80	0.0090	0.8979
				tpHZ	1.23	2.15	3.07	3.47	0.0263	0.8316
			tn_to_z	tpLZ	1.07	1.39	1.70	1.84	0.0090	0.9379
				tpHZ	1.27	2.19	3.11	3.51	0.0263	0.8716
				tpZH	1.66	2.58	3.50	3.90	0.0263	1.2616
				tpZL	1.22	1.54	1.85	1.99	0.0090	1.0879
bt8rl	2	1	a_to_z	tpLH	1.57	2.76	3.95	4.46	0.0340	1.0653
				tpHL	1.00	1.36	1.73	1.88	0.0104	0.8422
			en_to_z	tpZH	1.73	2.92	4.11	4.62	0.0340	1.2253
				tpZL	1.31	1.67	2.04	2.19	0.0104	1.1522
				tpLZ	1.01	1.37	1.74	1.89	0.0104	0.8522
				tpHZ	1.43	2.62	3.81	4.32	0.0340	0.9253
			tn_to_z	tpLZ	1.03	1.39	1.76	1.91	0.0104	0.8722
				tpHZ	1.45	2.64	3.83	4.34	0.0340	0.9453
				tpZH	1.83	3.02	4.21	4.72	0.0340	1.3253
				tpZL	1.41	1.77	2.14	2.29	0.0104	1.2522

AC Characteristics: (Cont.)

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/D Slots*	*Pads*	*Delay Path*	*Output*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
bt8rpl	2	1	a_to_z	tpLH	1.55	2.65	3.74	4.21	0.0312	1.0867
				tpHL	1.00	1.34	1.67	1.82	0.0097	0.8501
			en_to_z	tpZH	1.70	2.80	3.89	4.36	0.0312	1.2367
				tpZL	1.19	1.53	1.86	2.01	0.0097	1.0401
				tpLZ	1.21	1.55	1.88	2.03	0.0097	1.0601
				tpHZ	1.46	2.56	3.65	4.12	0.0312	0.9967
			tn_to_z	tpLZ	1.27	1.61	1.94	2.09	0.0097	1.1201
				tpHZ	1.52	2.62	3.71	4.18	0.0312	1.0567
				tpZH	1.80	2.90	3.99	4.46	0.0312	1.3367
				tpZL	1.29	1.63	1.96	2.11	0.0097	1.1401

Name: bt12l Description: 12 mA 3.3 V 3-State Output Buffer

Coding Syntax: z=&bt12*l(a,en,tn)

Loading Characteristics:

Values stated in standard loads.

Version	*a*	*en*	*tn*
bt12l	1.5	2.7	1.5

Pin Z Output Capacitance: Device(3.2 pF) + pad(0.8 pF) = 4.0 pF

AC Characteristics:

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/D Slots*	*Pads*	*Delay Path*	*Output*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
bt12l	3	1	a_to_z	tpLH	1.25	1.88	2.51	2.78	0.0180	0.9759
				tpHL	0.89	1.11	1.33	1.42	0.0062	0.7993
			en_to_z	tpZH	1.42	2.05	2.68	2.95	0.0180	1.1459
				tpZL	1.07	1.29	1.51	1.60	0.0062	0.9793
				tpLZ	1.00	1.22	1.44	1.53	0.0062	0.9093
				tpHZ	1.09	1.72	2.35	2.62	0.0180	0.8159
			tn_to_z	tpLZ	1.04	1.26	1.48	1.57	0.0062	0.9493
				tpHZ	1.13	1.76	2.39	2.66	0.0180	0.8559
				tpZH	1.51	2.14	2.77	3.04	0.0180	1.2359
				tpZL	1.16	1.38	1.60	1.69	0.0062	1.0693
bt12rl	3	1	a_to_z	tpLH	1.36	2.18	3.01	3.36	0.0236	1.0030
				tpHL	0.99	1.23	1.47	1.57	0.0069	0.8815
			en_to_z	tpZH	1.55	2.37	3.20	3.55	0.0236	1.1930
				tpZL	1.19	1.43	1.67	1.77	0.0069	1.0815
				tpLZ	1.04	1.28	1.52	1.62	0.0069	0.9315
				tpHZ	1.28	2.10	2.93	3.28	0.0236	0.9230
			tn_to_z	tpLZ	1.08	1.32	1.56	1.66	0.0069	0.9715
				tpHZ	1.32	2.14	2.97	3.32	0.0236	0.9630
				tpZH	1.66	2.48	3.31	3.66	0.0236	1.3030
				tpZL	1.30	1.54	1.78	1.88	0.0069	1.1915

AC Characteristics: (Cont.)

VDD=5 V, Ambient Temperature=25 degrees C, Estimated Wire Length=0, Process=Nominal. Values stated in nanoseconds.

Version	*I/D Slots*	*Pads*	*Delay Path*	*Output*	*Capacitance Loads (pF)*				*Slope*	*Incpt*
					15	*50*	*85*	*100*		
bt12rpl	3	1	a_to_z	tpLH	1.38	2.16	2.93	3.27	0.0222	1.0487
				tpHL	0.94	1.18	1.42	1.52	0.0069	0.8315
			en_to_z	tpZH	1.53	2.31	3.08	3.42	0.0222	1.1987
				tpZL	1.10	1.34	1.58	1.68	0.0069	0.9915
				tpLZ	1.20	1.44	1.68	1.78	0.0069	1.0915
				tpHZ	1.31	2.09	2.86	3.20	0.0222	0.9787
			tn_to_z	tpLZ	1.26	1.50	1.74	1.84	0.0069	1.1515
				tpHZ	1.37	2.15	2.92	3.26	0.0222	1.0387
				tpZH	1.64	2.42	3.19	3.53	0.0222	1.3087
				tpZL	1.21	1.45	1.69	1.79	0.0069	1.1015

Chapter 4
Logic Functions (Block Synthesis) and Memories (Memory Compiler)

This chapter lists logic functions available through the C-MDE Block Synthesis program and memories available through the C-MDE Memory Compiler program.

4.1 Logic Functions Available Through Block Synthesis

Block Synthesis is a design tool that automates the design, verification, and documentation of common logic functions.

Counters, registers, and multiplexers are examples of functions that are part of almost every digital system design. With Block Synthesis, optimized logic functions that are "right by construction" are automatically generated from user specifications. Table 4.1 lists Block Synthesis-generated logic functions: the variety of logic function, the bit width, and the available options.

Table 4.1 Block Synthesis-Generated Logic Functions

Logic Function	*Variety*	*Width (Bits)*	*Available Options*
Adders	Carry Select	1-64	
	Carry Look-Ahead	1-64	
	Carry-Skip	1-64	
	Ripple Carry	1-64	
	Advanced Parallel	1-512	Optimized for Speed/Gates Carry-in/Carry-out High-drive Output Pipelined with Choice of Flip-Flop

(Sheet 1 of 3)

Table 4.1 (Cont.) Block Synthesis-Generated Logic Functions

Logic Function	*Variety*	*Width (Bits)*	*Available Options*
Counters	Ripple Binary	2-64	Clear Direct Set Direct Clear Direct, Count Enable Set Direct, Count Enable
	Johnson	2-64	Asynchronous Clear Asynchronous Set Synchronous Clear Count Enable
	Binary Up Binary Down Binary Up/Down	2-64	Asynchronous Clear Asynchronous Set Asynchronous Load Synchronous Clear Synchronous Set Synchronous Load Count Enable
	Shift	3-12	Asynchronous Clear Asynchronous Set Asynchronous Load Synchronous Clear Synchronous Set Synchronous Load Count Enable
	Gray Up Gray Down Gray Up/Down	4-32	Asynchronous Clear Asynchronous Set Synchronous Clear
Multiplexers	2-16	1-64	Invert/Normal Outputs Gated/Non-Gated Outputs Encoded/Decoded Selects Optimized for Speed/Gates
Incrementers Decrementers	Incrementer Decrementer Incrementer/Decrementer	1-64	Invert/Normal Outputs Gated/Non-Gated Outputs Optimized for Speed/Gates
Decoders	2-to-4 through 7-to-128		Invert/Normal Outputs Gated/Non-Gated Outputs High Drive Outputs

(Sheet 2 of 3)

Table 4.1 (Cont.) Block Synthesis-Generated Logic Functions

Logic Function	*Variety*	*Width (Bits)*	*Available Options*
Shift Register		2-128	Asynchronous Clear Asynchronous Set Asynchronous Parallel Load Synchronous Clear Synchronous Set Synchronous Parallel Load Shift Enable Shift Left/Right
FT/FIFO	2-1024 Words	1-128	Block Layout or Not
Comparator		1-128	Invert/Normal Outputs Optimized for Speed/Gate High Drive Outputs Buffered/Unbuffered Inputs
BUFGEN	2-2048 Input UL	2-256 Fan-Outs	Invert/Normal Outputs
Multipliers	16 Multipliers 32 Addends for Sum-of-Product	128 x 128	Delay of Multiplicands Delay of Multipliers Delay of Addends Signed/Unsigned/Mixed-mode of any I/O 1 Pipeline with choice of Flip-Flop
JTAG	TAP Controller Instruction Register Device ID Registers		
Barrel Shifters	Logical Arithmetic Circular Logical/Arithmetic/Circular	128	Invert/Normal Outputs Left/Right - Left/Right Maximum Shift Positions
RAM-BIST	For all 1-Port RAMs		Number of Words Word Length Sub-word Length
ALU	74181	1-256	Optimized for Speed/Gates Buffered/Unbuffered Inputs/Outputs Optimized for Speed/Gates
	ALU within the 2901	1-256	Buffered/Unbuffered Inputs/Outputs Carry-out Options Optimized for Speed/Gates RAM size (8-1024)
	2901	4-128	Carry-out Options

(Sheet 3 of 3)

4.2 Memories Available Through Memory Compiler

Memory Compiler is a design tool that automatically generates application-specific single- or multi-port megacells—such as static RAMs, ROMs, FIFOs, and CAMs—for cell- and array-based designs. With Memory Compiler, the user can quickly and efficiently generate memories optimized for both speed and area. For example, RAM and ROM can be configured so as to eliminate unnecessary memory, require fewer buffers, and avoid inter-chip skew problems. Memory Compiler also creates data sheets for each megacell generated and logic and layout design files used for simulation, testing, and layout.

Table 4.2 shows the array-based megacells generated by Memory Compiler; Table 4.3 shows the cell-based megacells.

For more information contact your LSI Logic applications engineer.

Table 4.2 Memory Compiler-Generated Array-Based Megacells

Type	*Description*	*Max. Configuration*	*Min. Configuration*	*Max Configuration Taa (ns)*
DM023	2 Port RAM - 1r1w	54x32	8x4	5.4
DM024	2 Port RAM - 1r1w	128x32	65x4	6.31
DS023	3 Port RAM - 2r1w	64x32	8x4	TBD
GA023	1 Port RAM - 1rw	64x32	8x4	5.43
GA024	1 Port RAM - 1rw	128x32	65x32	6.33
GA031	ROM	256x32	16x8	7.0
GA032	ROM	1Kx32	512x8	10.0
FDTRAM31	2 Port RAM - 1r1rw	64x32	8x4	5.1
FDTRAM32	2 Port RAM - 1r1rw	128x32	65x4	TBD

Table 4.3
Memory Compiler-Generated Cell-Based Megacells

Type	*Description*	*Max Configuration*	*Min Configuration*	*Max Configuration Taa (ns)*
MG702	Low-Power 2 Port RAM with bit or byte write option - 1r1w	1Kx72	8x1	9.56
MG704	Low-Power 3 Port RAM with bit or byte write option - 2r1w	1Kx72	8x1	9.7
MG705	High-Density 2 Port RAM - 2rw	2Kx24	16x2	6.8
MG709	CAM - Content Addressable Memory	TBD	TBD	TBD
MG712	Low-Power 1 Port RAM with bit or byte write option - 1rw	1Kx72	16x2	6.3
MG714	High-Density 1 Port RAM with bit or byte write option - 1rw	2Kx36	32x8	7.1
MG716	ROM	2Kx72	32x2	10.2
MG722	Synchronous 1 Port RAM with bit or byte write option - 1rw	2Kx36	16x2	6.0
MG724	Delay Line Memory	2Kx36	16x4	2.0 ns[1]
MG732	RAM Based FIFO	2Kx24	32x2	TBD

1.TACK = 2.0 ns (The falling edge of 2047 clock cycle to data output)

Chapter 5
Macrofunctions

This chapter contains a table of any available macrofunctions. The table shows the macrofunction names, industry standard names, short functional descriptions, gate counts, and cell unit counts (where applicable).

The table is divided into the following categories:

- Adders
- Buffers
- Clock Prescalers
- Comparators
- Counters
- Decoders
- JTAG
- Latches
- Multiplexers
- Parity Decoders
- Registers
- Synchronizers

Name	*Industry Standard Name*	*Description*	*Array-Based Gate Count*	*Cell-Based Gate Count*	*Cell-Based Cell Units*
Adders					
CLA1		Carry Look-Ahead for 4-Bit Adder	24	23	67
CLA2		Carry Look-Ahead for 4-Bit Adder	21	20	67
CLA2B		Carry Look-Ahead for 2 Blocks of Adders	7	5	16
CLA2BGP		CLA for 2 Blocks of Adders with Group G, P Outputs	14	10	36
CLA4B		Carry Look-Ahead for 4 Blocks of Adders	24	19	75
CLA4BGP		CLA for 4 Blocks of Adders with Group G, P Outputs	38	30	125
FA2	7482	2-Bit Binary Full Adder	20	18	52
FA4		4-Bit Binary Full Adder	50	41	146
FA4C		4-Bit CLA Adder with Carry Out	51	49	167
FA4GP		4-Bit CLA Adder with Group Generate/Propagate	63	61	210
FA8		8-Bit Carry Look-Ahead Adder	121	115	393
FA16		16-Bit Carry Look-Ahead Adder	277	251	872

(Sheet 1 of 8)

Name	*Industry Standard Name*	*Description*	*Array-Based Gate Count*	*Cell-Based Gate Count*	*Cell-Based Cell Units*
FA32		32-Bit Carry Look-Ahead Adder	588	550	1908
FAS2		2-Bit Binary 25 Complement Full Adder, Subtractor	26	20	62
M82C	7482	2-Bit Binary Full Adder	20	20	48
Buffers					
M244C	74244	Dual 4-Bit 3-State Internal Buffer	36	26	88
Clock Prescalers					
PS2		Divide by 2 External Clock Prescaler	17	16	41
PS3		Divide by 3 External Clock Prescaler	25	24	61
PS4		Divide by 4 External Clock Prescaler	33	32	82
Comparators					
CMP4		4-Bit Equality Comparator	15	14	46
CMP8		8-Bit Equality Comparator	30	29	97
MAG2	1/2SN7485	2-Bit Expandable Magnitude Comparator	27	22	73
MAG2H		2-Bit Magnitude Comparator	22	17	59
MAG4		4-Bit Expandable Magnitude Comparator	50	44	151
M85C		4-Bit Expandable Magnitude Comparator	50	44	151
M85S	7485/74S85 74LS85	4-Bit Magnitude Comparator	42	40	156
M85L	74L85	4-Bit Magnitude Comparator	40	38	150
Counters - Binary					
CB4C		4-Bit Binary Up Counter with Synchronous Clear	50	44	131
CB5C		5-Bit Binary Up Counter with Synchronous Clear	64	57	173
CB6C		6-Bit Binary Up Counter with Synchronous Clear	78	70	212
CB7C		7-Bit Binary Up Counter with Synchronous Clear	96	84	256
CB8C		8-Bit Binary Up Counter with Synchronous Clear	113	98	298
CB9C		9-Bit Binary Up Counter with Synchronous Clear	131	112	347
CB10C		10-Bit Binary Up Counter with Synchronous Clear	147	127	393
CB4F		4-Bit Binary Up Counter with CD and SD	53	49	138
CB5F		5-Bit Binary Up Counter with CD and SD	72	63	180
CB6F		6-Bit Binary Up Counter with CD and SD	90	77	221
CB7F		7-Bit Binary Up Counter with CD and SD	108	92	266

(Sheet 2 of 8)

Name	*Industry Standard Name*	*Description*	*Array-Based Gate Count*	*Cell-Based Gate Count*	*Cell-Based Cell Units*
CB8F		8-Bit Binary Up Counter with CD and SD	127	107	309
CB9F		9-Bit Binary Up Counter with CD and SD	145	122	354
CB10F		10-Bit Binary Up Counter with CD and SD	163	138	401
CB41		4-Bit Binary Up Counter, Expandable with CD	62	54	150
CB42		4-Bit Binary Up Counter, Expandable, Synchronous Clear	62	58	166
CM3B		Mod-3 Binary Counter with CD	19	17	46
CM4B		Mod-4 Binary Counter with CD	19	18	46
CM5B		Mod-5 Binary Counter with CD	34	31	79
CM6B		Mod-6 Binary Counter with CD	33	31	81
CM7B		Mod-7 Binary Counter with CD	37	34	89
CM8B		Mod-8 Binary Counter with CD	29	29	75
CM9B		Mod-9 Binary Counter with CD	47	43	109
CM10B		Mod-10 Binary Counter with CD	45	42	109
CM11B		Mod-11 Binary Counter with CD	49	45	117
CM12B		Mod-12 Binary Counter with CD	46	42	107
CM13B		Mod-13 Binary Counter with CD	50	46	119
CM14B		Mod-14 Binary Counter with CD	49	45	114
CM15B		Mod-15 Binary Counter with CD	52	48	128
CM16B		Mod-16 Binary Counter with CD	44	41	105
CM17B		Mod-17 Binary Counter with CD	61	56	141
M160C	74160	4-Bit Binary Counter, Synchronous Load, Asynch. Clear	80	66	197
M160D	74160	4-Bit Binary Counter, Synchronous Load, Asynch. Clear	76	72	219
M161C	74161	4-Bit Binary Counter, Synchronous Load, Asynch. Clear	70	63	186
M161D	74161	4-Bit Binary Counter, Synchronous Load, Asynch. Clear	70	68	210
M162C	74162	4-Bit Binary Counter, Synchronous Load, Synch. Clear	78	64	200
M162D	74162	4-Bit Binary Counter, Synchronous Load, Synch. Clear	74	71	222
M163C	74163	4-Bit Counter, Expandable, Synch. Load, Synch. Clear	78	63	190
M163D	74163	4-Bit Counter, Expandable, Synch. Load, Synch. Clear	72	69	215
M163F	74163	4-Bit Fast Binary Counter, Expandable, Synch. Load/Clear	115	104	296
M169C	74169	4-Bit Up/Down Counter, Expandable, Synch. Load	77	71	209

(Sheet 3 of 8)

Name	*Industry Standard Name*	*Description*	*Array-Based Gate Count*	*Cell-Based Gate Count*	*Cell-Based Cell Units*
Counters - Gray Code					
C2G		Mod-4 Gray Code Counter with CD	20	16	42
C3G		Mod-8 Gray Code Counter with CD	34	31	84
C4G		Mod-16 Gray Code Counter with CD	56	52	140
C5G		Mod-32 Gray Code Counter with CD	70	67	186
C6G		Mod-64 Gray Code Counter with CD	84	79	212
C7G		Mod-28 Gray Code Counter with CD	100	91	241
C8G		Mod-256 Gray Code Counter with CD	115	104	275
Counters - Johnson					
CM4J		Mod-4 Johnson Counter with CD	18	16	42
CM6J		Mod-6 Johnson Counter with CD	27	24	63
CM8J		Mod-8 Johnson Counter with CD	36	32	84
CM10J		Mod-10 Johnson Counter with CD	45	40	105
CM12J		Mod-12 Johnson Counter with CD	54	48	126
CM14J		Mod-14 Johnson Counter with CD	63	56	147
CM16J		Mod-16 Johnson Counter with CD	72	64	168
Counters - Shift					
CM5SR		Mod-5 Shift Counter with CD	28	25	67
CM8SR		Mod-8 Shift Counter with CD	31	28	76
CM9SR		Mod-9 Shift Counter with CD	40	36	98
CM10SR		Mod-10 Shift Counter with CD	42	38	103
CM12SR		Mod-12 Shift Counter with CD	41	37	97
Counters - Up/Down					
CUD41		4-Bit Up/Down Counter with CD	72	65	191
CUD42		4-Bit Up/Down Counter with Asynch. Load Clear	92	83	258
Decoders					
D24GH		Gated 2-to-4 Decoder, Outputs High	15	10	34
D24GL		Gated 2-to-4 Decoder, Outputs Low	16	10	34
D24H		2-to-4 Decoder, Outputs High	10	6	26
D24L		2-to-4 Decoder, Outputs Low	10	6	26
D38GH		Gated 3-to-8 Decoder, Outputs High	32	19	89

(Sheet 4 of 8)

Name	*Industry Standard Name*	*Description*	*Array-Based Gate Count*	*Cell-Based Gate Count*	*Cell-Based Cell Units*
D38GL		Gated 3-to-8 Decoder, Outputs Low	38	19	89
D38H		3-to-8 Decoder, Outputs High	27	19	65
D38L		3-to-8 Decoder, Outputs Low	30	19	65
D410H		4-to-10 Decoder, Outputs High	38	24	112
D410L		4-to-10 Decoder, Outputs Low	49	24	113
M42	7442	4-to-10 Decoder, Outputs Low	44	27	98
M138D	74138	Gated 3-to-8 Decoder, Outputs Low	42	24	106
DM6JH		Decoder for Mod-6 Johnson Counter, Outputs High	12	6	30
DM6JL		Decoder for Mod-6 Johnson Counter, Outputs Low	12	6	30
DM8JH		Decoder for Mod-8 Johnson Counter, Outputs High	16	8	40
DM8JL		Decoder for Mod-8 Johnson Counter, Outputs Low	16	8	40
DM10JH		Decoder for Mod-10 Johnson Counter, Outputs High	20	10	50
DM10JL		Decoder for Mod-10 Johnson Counter, Outputs Low	20	10	50
DM12JH		Decoder for Mod-12 Johnson Counter, Outputs High	24	12	60
DM12JL		Decoder for Mod-12 Johnson Counter, Outputs Low	24	12	60
DM14JH		Decoder for Mod-14 Johnson Counter, Outputs High	28	14	70
DM14JL		Decoder for Mod-14 Johnson Counter, Outputs Low	28	14	70
DM16JH		Decoder for Mod-16 Johnson Counter, Outputs High	32	16	80
DM16JL		Decoder for Mod-16 Johnson Counter, Outputs Low	32	16	80
JTAG					
TAPC_D6		JTAG TAP Controller	210	181	462
TAPDC1		JTAG TAP Instruction Decoder 1	15	7	22
Latches					
L3X8		8-Bit Gated Latch with CD	48	40	128
L4		4-Bit Gated Latch	24	20	52
L8		8-Bit Gated Latch	48	40	104
Multiplexers					
M150C	74150	16-to-1 Inverting MUX with Gated Outputs	31	36	132
M151C	74151	8-to-1 MUX with Gated Outputs	16	19	69
M152C	74152	8-to-1 Inverting MUX	13	17	60
M153C	74L5152	Gate Dual 4-Input MUX	18	14	44

(Sheet 5 of 8)

Name	*Industry Standard Name*	*Description*	*Array-Based Gate Count*	*Cell-Based Gate Count*	*Cell-Based Cell Units*
M157C	74157	Quad 2-to-1 Non-Inverting MUX, Gated Outputs	18	13	47
M158C	74158	Quad 2-to-1 Inverting MUX, Gated Outputs	22	11	49
MUX41GH		4-Bit Non-Inverting MUX, Gate	9	8	23
MUX41H		4-Bit Non-Inverting MUX	7	6	17
MUX41L		4-Bit Inverting MUX	7	7	19
MUX52H		Dual 5-Bit Non-Inverting MUX	20	19	50
MUX54H		Quad 5-Bit Non-Inverting MUX	44	35	94
MUX61H		Quad 6-Bit Non-Inverting MUX	14	12	31
MUX62H		Dual 6-Bit Non-Inverting MUX	28	21	56
MUX64H		Quad 6-Bit Non-Inverting MUX	56	39	107
MUX71H		7-Bit Non-Inverting MUX	15	14	38
MUX72H		Dual 7-Bit Non-Inverting MUX	30	25	70
MUX74H		Quad 7-Bit Non-Inverting MUX	48	47	135
MUX81H		8-Bit Non-Inverting MUX	15	14	48
MUX22H		Dual 2-to-1 Non-Inverting MUX	8	7	27
MUX24H		Quad 2-to-1 Non-Inverting MUX	16	13	51
MUX24L		Quad 2-to-1 Inverting MUX	9	9	39
MUX31H		3-to-1 Non-Inverting MUX	8	7	20
MUX31L		3-to-1 Inverting MUX	8	8	23
MUX32H		Dual 3-to-1 Non-Inverting MUX	12	13	37
MUX34H		Quad 3-to-1 Non-Inverting MUX	22	26	74
MUX42H		Dual 4-to-1 Non-Inverting MUX	14	12	32
MUX44H		Quad 4-to-1 Non-Inverting MUX	24	24	64
MUX51H		5-to-1 Non-Inverting MUX	10	11	27
MUX51L		5-to-1 Inverting MUX	10	9	28
MUX61L		6-to-1 Inverting MUX	14	14	48
MUX71L		7-to-1 Inverting MUX	6	16	57
MUX82H		Dual 8-to-1 Non-Inverting MUX	30	28	80
MUX84H		Quad 8-to-1 Non-Inverting MUX	60	56	160
Parity Detectors					
PAR8		8-Bit Odd Parity Detector	24	21	64
PAR9		9-Bit Odd Parity Detector	28	24	80

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Name	*Industry Standard Name*	*Description*	*Array-Based Gate Count*	*Cell-Based Gate Count*	*Cell-Based Cell Units*
Registers					
C3LSR		Mod-7 Linear Feedback Shift Register	29	26	67
C4LSR		Mod-15 Linear Feedback Shift Register	38	34	88
C5LSR		Mod-31 Linear Feedback Shift Register	48	43	114
C6LSR		Mod-63 Linear Feedback Shift Register	56	50	130
C7LSR		Mod-127 Linear Feedback Shift Register	65	58	151
C8LSR		Mod-255 Linear Feedback Shift Register	80	72	190
C9LSR		Mod-511 Linear Feedback Shift Register	84	75	197
C10LSR		Mod-1023 Linear Feedback Shift Register	93	83	219
C11LSR		Mod-2047 Linear Feedback Shift Register	102	91	240
C12LSR		Mod-4095 Linear Feedback Shift Register	117	105	280
C13LSR		Mod-8191 Linear Feedback Shift Register	126	113	301
C14LSR		Mod-16383 Linear Feedback Shift Register	135	121	322
C15LSR		Mod-32767 Linear Feedback Shift Register	138	123	324
C16LSR		Mod-65535 Linear Feedback Shift Register	153	137	364
C17LSR		Mod-131071 Linear Feedback Shift Register	156	139	366
C18LSR		Mod-262143 Linear Feedback Shift Register	165	147	387
C19LSR		Mod-524287 Linear Feedback Shift Register	180	161	427
C20LSR		Mod-1048575 Linear Feedback Shift Register	183	163	429
MR41		4-Bit Register with 2-Bit Multiplexed Inputs	40	37	103
MR42		4-Bit Register with 2-Bit Multiplexed Inputs and CD	44	41	111
MR43		4-Bit Register with 2-Bit MUXED Inputs & Synch. Clear	45	39	113
MR44		4-Bit Register with 2-Bit MUXED Inputs & Synch. Clear	49	43	121
MR81		8-Bit Register with 2-Bit Multiplexed Inputs	80	73	204
MR82		8-Bit Register with 2-Bit Multiplexed Inputs and CD	88	81	220
Other Registers					
R41		4-Bit Data Register	32	28	72
R42		4-Bit Data Register, Clear Direct	36	32	84
R81		8-Bit Data Register	64	56	144
R82		8-Bit Data Register, Clear Direct	80	64	168
SR41		4-Bit Shift Register	32	28	72

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Name	*Industry Standard Name*	*Description*	*Array-Based Gate Count*	*Cell-Based Gate Count*	*Cell-Based Cell Units*
SR42		4-Bit Shift Register, Clear Direct	40	32	84
SR43		4-Bit Shift Register, Set Direct	36	32	80
SR44		4-Bit Shift Register, Sync. Parallel Load	42	38	96
SR45		4-Bit Shift Register, Sync. Parallel Load and Clear	45	39	104
SR46		4-Bit Shift Register, Async. Parallel Load	52	48	124
SR47		4-Bit Shift Register, Sync. Clear	36	32	84
Synchronizers					
SYNC01		Synchronizer for Asynchronous 0-to-1	16	15	39
SYNC10		Synchronizer for Asynchronous 1-to-0	16	15	39

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Chapter 6
System Building Blocks and CoreWare™ Microprocessors

By using system building blocks in a single-chip system, you can get to market faster than your competitors—and with a better solution. A single-chip system can offer the following advantages:

- shortened signal paths that reduce wire delays, allow higher clock frequencies, and save power
- increased functional density and reliability
- reduced costs
- better protection for your intellectual property

This chapter lists system building blocks and CoreWare microprocessors available at LSI Logic in the following four main sections:

- Industry Standard Peripheral Megafunctions

  Megafunctions can be combined on a chip with CoreWare microprocessors to form efficient high-performance systems. The number of megafunctions that can be combined on any one chip is determined by the size of the die chosen and the efficiency of the layout.

- Industry Standard Microcontrollers

  System architectures of various widths can be constructed from the 4- through 32-bit microcontroller slices.

- Arithmetic Elements

  These arithmetic elements can be the key building block of an ASIC device dedicated to a specific arithmetic operation, or they can be added as support for a microprocessor-based ASIC design.

- CoreWare Microprocessors

  High-performance CoreWare building blocks are fully supported for use in the LSI Logic silicon development environment.

For information and availability on the system building blocks and CoreWare listed in this chapter, contact your LSI Logic sales representative.

6.1 Industry Standard Peripheral Megafunctions

Table 6.1 lists by standard part number, computer, microprocessor, and embedded systems peripheral building blocks that are available as soft-coded (netlist format) cells.

Table 6.1 Industry Standard Peripheral Megafunctions

Industry-Standard Part Number	*Description*	*LSI Logic Number*
6402	UART	Y4020
6845	CRT Controller	M8450
6850	UART	M8500
6850+	UART with Differential Control	M8501
6854	Data Link (HDLC/SDLC) Controller	M8540
8237	4-channel 8-bit Multimode DMA Controller	I2370
8251	USART	I2511
8253	Three Programmable 16-bit Binary and BCD Counters	I2530
8254	Three Programmable 16-bit Binary and BCD Counters	I2540
8255	8-bit Bidirectional 2-Port Parallel Interface, with Handshake	I2550
8255	8-bit Bidirectional 3-Port Parallel Interface	I2551
8259	8-input Cascadable Priority Interrupt Control	I2590
8259+	8-input Cascadable Priority Interrupt Control (8086 mode only)	I2591
8284	Clock Generator/Driver for the 8085 and 8086 Microprocessors	I2840
8288	Bus Controller for the 8085 and 8086 Microprocessors	I2880
8530	Serial Communications Controller (SCC/USART)	Y5300
16450	Async Communications Element, Modem Interface	N0450
16550	Async Communications Element, Modem Interface	N0550
82284	Clock Generator/Driver for the 80286 Microprocessor	IB840
82288	Bus Controller for the 80286	IB880
MC146818	Real Time (time-of-day) Clock	Y8180
MC146818	Real Time (time-of-day) Clock (RAM-less version)	Y8181

6.2 Industry Standard Microcontrollers

Table 6.2 lists elements that are architecturally-enhanced CMOS versions of:

- 8-bit microcontroller products
- TTL 2900, 29100, and 29500 bit-slice microcontroller products

Table 6.2
Industry Standard
Microcontrollers

Industry Standard Part Number	*Size*	*Description*	*Gate Count*	*LSI Logic Number*
8031	8-bit	Microcontroller	14569	IO310
8051	8-bit	Microcontroller	19542	IO510
8042	8-bit	Keyboard Controller	11954	IO420
2901	4-bit	Cascadable Microcontroller	764	A0010
2903	4-bit	Cascadable Microcontroller	919	A0030
29203	4-bit	Cascadable Microcontroller with BCD Support	1717	A2030
2901	8-bit	with 16x8 RAM	946	A0014
29501	8-bit	Cascadable Multiport Pipeline Processor	1479	A5010
29501	8-bit	with ALU MSB Output	1481	A5011
29501	8-bit	with Scan Path to Internal Registers	1530	A5012
29101	16-bit	Microcontroller	2259	A0012
2901	16-bit	with 32x16 RAM	3435	A0015
29117	16-bit	Microcontroller	4391	A1170
29117	32-bit	Microcontroller	7381	A1171
2909	4-bit	Microprogram Sequencer (Cascadable to 12 bits)	346	A0090
2911	4-bit	Microprogram Sequencer (Cascadable to 12 bits)	347	A0110
2910	12-bit	Microprogram Controller/ Sequencer (5-deep stack)	1182	A0100
2910A	12-bit	Microprogram Controller/Sequencer (9-deep stack)	1557	A0102
2910	16-bit	Microprogram Controller/Sequencer (5-deep stack)	1492	A0101
2904		Status and Shift Control Unit	504	A0040
2914		Vectored Priority Interrupt Controller	653	A0140
2930	4-bit	Cascadable Program Control Unit	1014	A0300
2942		DMA Address Generator, Timer/Counter	904	A0421

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Table 6.2 (Cont.)
Industry Standard Microcontrollers

Industry Standard Part Number	*Size*	*Description*	*Gate Count*	*LSI Logic Number*
2960	16-bit	Error Detection/Correction Controller	694	A0601
2960	32-bit	Error Detection/Correction Controller	1295	A0602
2960	64-bit	Error Detection/Correction Controller	2379	A0603
2964		64K-bit Dynamic RAM Controller	276	A0640
29368		1M-bits DRAM Controller/Driver	679	A3680

(Sheet 2 of 2)

6.3 Arithmetic Elements

Tables 6.3 through 6.12 list elements that implement industry-standard TTL or ECL arithmetic functions. These megafunctions are available in a mixture of hard-coded (metal) and soft-coded (netlist format) cells.

Table 6.3
Arithmetic Logic Units

Industry-Standard Part Number	*Size*	*Description*	*Gate Count*	*LSI Logic Number*
74181	4-bit	Cascadable ALU	125	T1810
100181	4-bit	Cascadable ALU with BCD Support	163	B1010
74181	16-bit	ALU using Carry-Lookahead	538	T1811
74181	16-bit	ALU using Carry-Select Adder for A=B output	666	T1814
100181	16-bit	ALU with BCD Support	733	B1020
	16-bit	ALU (A=B,A-B,A=1,A-1,A=2,A)	407	B1040
	16-bit	ALU (A=B,A-B,A=1,A-1,A)	404	B1050
74181	32-bit	ALU using Carry-Lookahead	1089	T1812
74181	32-bit	ALU using Carry-Select Adder for A=B Output	1339	T1813
74181	32-bit	ALU using Carry-Select Adder with carry-out every 4 bits	1346	T1815

Table 6.4 Adders

Size	*Description*	*Gate Count*	*LSI Logic Number*
2-bit	7482 Binary Full Adder	20	FA2
4-bit	Binary Full Adder	50	FA4
4-bit	Carry-Lookahead Adder with Carry-out	51	FA4C
4-bit	Carry-Lookahead Adder with Group Generate and Propagate	63	FA4GP
8-bit	Carry-Lookahead Adder	121	FA8
16-bit	Carry-Lookahead Adder	277	FA16
16-bit	Carry-Select Adder	287	B0220
16-bit	3-Port Carry-Select Adder	450	B0600
16-bit	3-Port Adder	400	B0601
32-bit	Carry-Select Adder	643	B0230
32-bit	Carry-Select Adder with Carry-out every 4 bits	650	B0231
32-bit	Carry-Lookahead Adder	588	FA32
32-bit	Carry-Lookahead Adder with BCD Support	851	B0232
32-bit	3-Port Carry-Select Adder	904	B0610
32-bit	3-Port Adder with One 12-bit Port MSB-aligned	860	B0611
32-bit	3-Port Adder with One 12-bit Port LSB-aligned	860	B0612

Table 6.5 Comparators

Size	*Description*	*Gate Count*	*LSI Logic Number*
4-bit	Equality Comparator	15	CMP4
8-bit	Equality Comparator	30	CMP8
4-bit	7485 Magnitude Comparator	42	M85S
4-bit	Expandable Magnitude Comparator	50	M85C
16-bit	Magnitude Comparator	162	C2100
32-bit	Magnitude Comparator	334	C2200

Table 6.6 Divider Circuit

Size	*Description*	*Gate Count*	*LSI Logic Number*
16-bit	Divider (16-bit Fraction)/(16-bit Fraction)	1155	B4000

Table 6.7 Mixed-Mode Multipliers

Size	*Description*	*Gate Count*	*LSI Logic Number*
6x4	Multiplier	316	B2150
8x6	Multiplier	524	B2090
8x8	Multiplier, 17-bit Result	655	B2001
12x6	Multiplier	771	B2070
12x12	Multiplier	1236	B2013
13x12	Multiplier, Rounding at bit 12	1305	B2120
13x14	Multiplier	1506	B2110
13x18	Multiplier	1874	B2100
16x8	Multiplier	1230	B2060
16x12	Multiplier, 1-stage Pipeline	2159	B2430
16x16	Multiplier	1965	B2023
16x16	Multiplier, Rounding at LSB 15	2742	B2021
16x16	Multiplier, 1-stage Pipeline	2278	B2403
16x16	Multiplier, 1-stage Pipeline, Scan Test	3289	B2400
24x24	Multiplier	5601	B2130
24x24	Multiplier, 1-stage Pipeline	5279	B2410
25x4	Multiplier	1540	B2040
25x16	Multiplier	4740	B2050
32x32	Multiplier, 1-stage Pipeline	7125	B2440
55x56	Multiplier	29140	B2080

Table 6.8 Mixed-Mode Multiplier Accumulators (MACS)

Size	*Description*	*Gate Count*	*LSI Logic Number*
6x6	MAC, 18-bit Addend	570	B2230
12x8	MAC, 23-bit Addend	981	B2220
13x12	MAC, 27-bit Addend	2536	B2280
16x14	MAC, 35-bit Addend	1837	B2250
16x16	MAC, 32-bit Addend, 34-bit Result	2446	B2210
16x16	MAC, 32-bit Addend, 35-bit Result	2452	B2211
16x16	MAC, 36-bit Addend	2127	B2212
16x16	MAC, 36-bit Addend, 38-bit Result	2524	B2700
19x16	MAC, 35-bit Addend	2379	B2240
32x8	MAC, 40-bit Addend, 1-stage Pipeline, Scan Test	3550	B2600
32x32	MAC, 65-bit Addend, 1-stage Pipeline	7504	B2710

Table 6.9 Two's-Complement Multipliers

Size	*Description*	*Gate Count*	*LSI Logic Number*
8x8	Two's-Complement Multiplier	584	B2000
10x9	Two's-Complement Multiplier	853	B2190
12x12	Two's-Complement Multiplier	1224	B2010
12x12	Two's-Complement Multiplier, 1-stage Pipeline	1355	B2420
16x16	Two's-Complement Multiplier	2099	B2020
16x16	Two's-Complement Multiplier, 1-stage Pipeline	2605	B2401
16x16	Two's-Complement Multiplier, 1-stage Pipeline, CS	2741	B2402
18x18	Two's-Complement Multiplier	2433	B2030
32x16	Two's-Complement Multiplier, 1-stage Pipeline	4959	B2460
32x32	Two's-Complement Multiplier	8532	B2140
32x32	Two's-Complement Multiplier, 1-stage Pipeline	9363	B2441

Table 6.10 Two's-Complement Multiplier-Accumulators

Size	*Description*	*Gate Count*	*LSI Logic Number*
12x12	2's-Comp. MAC, 27-bit Addend	1352	B2200
24x24	2's-Comp. MAC, with Subtracter, Rounding at bit 22	5754	B2260
32x16	2's-Comp. MAC, 48-bit Addend	4856	B2270

Table 6.11 Special Purpose Multipliers

Size	*Description*	*Gate Count*	*LSI Logic Number*
8x8	Signed Multiplier	673	B2002
9x9	Signed Multiplier	812	B2180
9x10	Signed Multiplier	905	B2170
12x12	Unsigned Multiplier	1245	B2011
4-bit	A•B=C•D 2's-Complement Multiplier Adder	319	B2800
12-bit	A•B=C•D 2's-Complement Multiplier Adder	2829	B2810

Table 6.12 Shifter Circuits

Size	*Description*	*Gates*	*Cell ID*
8-bit	Barrel Shifter, Out-of-phase Outputs	71	C1000
8-bit	Barrel Shifter, In-phase Outputs	55	C1001
16-bit	Barrel Shifter, In-phase Outputs	124	C1010
32-bit	Barrel Shifter, Out-of-phase Outputs	291	C1020
32-bit	Arithmetic Shifter, Sign Extend, L/R Shift, 0/1 Fill (max shift =31)	442	C1120
40-bit	Arithmetic Shifter, Sign Extend (max shift =15)	385	C1100
40-bit	Arithmetic Shifter, Left Shift, 0/1 Fill (max shift =31)	476	C1102
40-bit	Arithmetic Shifter, Sign Extend, L/R Shift, 0/1 Fill (max shift =31)	689	C1101
64-bit	Arithmetic Shifter, L/R Shift, 0 Fill	957	C1110

6.4 CoreWare Microprocessors

Table 6.13 lists the high-performance CoreWare building blocks that LSI Logic provides for system-on-silicon design implementation.

They include simulation models with timing information so that designers can accurately simulate device performance and trade off various implementation options, and they include test vectors for device verification and testing.

Table 6.13
CoreWare Building Blocks

LSI Logic Number	*Description*	*Equivalent Gate Count*
Microprocessors		
CW33000	MIPS Embedded Processor	35K + 32x32 Register File + 5K RAM
	CPU Only Version	25K + 32x32 Register FIle
CW803	SPARC 32-bit RSIC Embedded Processor, 56 General Purpose Registers	20K + 56x32 Register FIle
CW807	SPARC 32-bit RSIC Embedded Processor, 120 General Purpose Registers	20K + 120x32 Register FIle
Floating-Point Processors		
FALU32	Non-Pipelined 32-bit ALU	8K
FMPY32	Non-Pipelined 32-bit Multiplier	8K
FALU32P	Pipelined 32-bit ALU	14K
FMPY32P	Pipelined 32-bit Multiplier	9K
FDIV32P	Pipelined 32-bit Divider	14.5K
FALU64	Non-Pipelined 64-bit ALU	20K
FMPY64	Non-Pipelined 64-bit Multiplier	23K
Image Compression		
CW702	JPEG Image Compression Engine	23K
Error Correction		
CW7100	Reed-Solomon CODECs	Dependent on Symbol Size and Redundancy
High-Bandwidth Interconnect		
CW1596	Scalable Coherent Interfaces (SCI)	70K