19-0474; Rev 1; 7/09

Quad, Ultra-Low-Power, 300Mbps ATE Drivers/Comparators

General Description

The MAX9972 four-channel, ultra-low-power, pin-electronics IC includes, for each channel, a three-level pin driver, a window comparator, a passive load, and force-and-sense Kelvin-switched parametric measurement unit (PMU) connections. The driver features a -2.2V to +5.2V voltage range, includes high-impedance and active-termination (3rd-level drive) modes, and is highly linear even at low voltage swings. The window comparator features 500MHz equivalent input bandwidth and programmable output voltage levels. The passive load provides pullup and pulldown voltages to the device-under-test (DUT).

Two grade versions are available, A grade and B grade. The A-grade version provides tight gain and offset matching for the driver and comparator, allowing reference levels to be shared across multiple channels. It also provides tighter tolerance of the load resistance values. The B-grade version is for system designs that incorporate independent reference levels for each channel.

Low-leakage, high-impedance, and terminate controls are operational configurations that are programmed through a 3-wire, low-voltage, CMOS-compatible serial interface. High-speed PMU switching is realized through dedicated digital control inputs.

This device is available in an 80-pin, 12mm x 12mm body, 1.0mm pitch TQFP with an exposed 6mm x 6mm die pad on the bottom of the package for efficient heat removal. The MAX9972 is specified to operate over the 0°C to +70°C commercial temperature range, and features a die temperature monitor output.

Features

- **Small Footprint—Four Channels in 0.3in^2**
- **Low-Power Dissipation: 325mW/Channel (typ)**
- **High Speed: 300Mbps at $3V_{P-P}$**
- **-2.2V to +5.2V Operating Range**
- **Active Termination (3rd-Level Drive)**
- **Integrated PMU Switches**
- **Passive Load**
- **Low-Leak Mode: 20nA (max)**
- **Low Gain and Offset Error**
- **Lead(Pb)-Free Package Available**

Applications

NAND Flash Testers

DRAM Probe Testers

Low-Cost Mixed-Signal/System-on-Chip (SoC) Testers

Active Burn-In Systems

Structural Testers

Pin Configuration appears at end of data sheet.

Ordering Information and Selector Guide

PART	ACCURACY GRADE	PIN-PACKAGE	HEAT EXTRACTION
MAX9972ACCS	A	80 TQFP-EP*	Bottom
MAX9972BCCS	B	80 TQFP-EP*	Bottom

Note: *All devices are specified over the 0°C to +70°C operating temperature range.*

All versions available in both leaded and lead(Pb)-free packaging. Specify lead(Pb)-free by adding the "+" symbol at the end of the part number when ordering.

**EP = Exposed pad.*

Quad, Ultra-Low-Power, 300Mbps ATE Drivers/Comparators

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ....-0.3V to +9.4V
V_{SS} to GND....................-6.25V to +0.3V
V_{DD} to V_{SS} ....+15.7V
V_L to GND....................-0.3V to +5V
V_{DD} to GND....................-0.3V to +9.4V
DHV_, DTV_, DLV_, DATA_, RCV_, LDV_,
DUT_ to GND....................V_{SS} to V_{DD}
CHV_, CLV_, CMPH_, CMPL_, COMPHI,
COMPLO to GND....................V_{SS} to V_{DD}
FORCE_, SENSE_, PMU_ to GND ....V_{SS} to V_{DD}
$\overline{LD}$, DIN, SCLK, $\overline{CS}$ to GND....................-0.3V to +5V
DUT_, CMPH_, CMPL_ Short-Circuit Duration....................Continuous
DHV_, DLV_, DTV_ to Each Other ....V_{SS} to V_{DD}
CHV_, CLV_ to DUT_ ....V_{SS} to V_{DD}
DOUT to GND....................-0.3V to +5V
TEMP Short-Circuit Duration ....Continuous
FORCE_ Path Switch Current....................50mA
SENSE_ Path Switch Current 1.5mA
Continuous Power Dissipation (T_A = +70°C)
80-Pin TQFP-EP (derate 35.7mW/°C above +70°C) 2857mW
Storage Temperature Range ....-65°C to +150°C
Junction Temperature....................+150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +8V, V_{SS} = -5V, V_L = +3V, V_{COMPHI} = +1V, V_{COMPLO} = 0V, $V_{LDV\_}$ = 0V, LOAD EN LOW = LOAD EN HIGH = 0, T_J = +75°C. All temperature coefficients measured at T_J = +50°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DRIVER (all specifications apply when DUT_ = DHV_, DUT_ = DTV_, or DUT_ = DLV_)							
DC CHARACTERISTICS							
Voltage Range				-2.2		+5.2	V
Gain		Measured at 0 and 3V	A grade	0.995	1	1.005	V/V
			B grade	0.95		1.05	
Gain Temperature Coefficient					50		ppm/°C
Offset		$V_{DHV\_}$ = 2V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = 1V	A grade			±10	mV
			B grade			±100	
Offset Temperature Coefficient					±250		µV/°C
Power-Supply Rejection Ratio	PSRR	V_{DD}, V_{SS} independently varied over full range				18	mV/V
Maximum DC Drive Current	$I_{DUT\_}$			±40		±90	mA
DC Output Resistance		$I_{DUT\_}$ = ±10mA (Note 2)		48.5	49.5	50.5	Ω
DC Output Resistance Variation		$I_{DUT\_}$ = -40mA to +40mA				2.5	Ω
DC Crosstalk		DHV to DLV and DTV: $V_{DLV\_}$ = $V_{DTV\_}$ = +1.5V, $V_{DHV\_}$ = -2.2V, +5.2V				5	mV
		DLV to DHV and DTV: $V_{DHV\_}$ = $V_{DTV\_}$ = +1.5V, $V_{DLV\_}$ = -2.2V, +5.2V				5	
		DTV to DHV and DLV: $V_{DHV\_}$ = $V_{DLV\_}$ = +1.5V, $V_{DTV\_}$ = -2.2V, +5.2V				5	
Linearity Error		0 to 3V (Note 3)				±5	mV
		Full range (Note 4)				±15	mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +8V, V_{SS} = -5V, V_L = +3V, V_{COMPHI} = +1V, V_{COMPLO} = 0V, $V_{LDV\_}$ = 0V, LOAD EN LOW = LOAD EN HIGH = 0, T_J = +75°C. All temperature coefficients measured at T_J = +50°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
AC CHARACTERISTICS (Note 5)							
Dynamic Output Current		(Note 1)		40			mA
Drive-Mode Overshoot, Undershoot, and Preshoot		200mV to $4V_{P-P}$ swing (Note 6)			5% +10		mV
Term-Mode Spike		$V_{DHV\_}$ = $V_{DTV\_}$ = 1V, $V_{DLV\_}$ = 0V			25		mV
		$V_{DLV\_}$ = $V_{DTV\_}$ = 0V, $V_{DHV\_}$ = 1V			25		
High-Impedance-Mode Spike		$V_{DLV\_}$ = -1V, $V_{DHV\_}$ = 0V			25		mV
		$V_{DLV\_}$ = 0V, $V_{DHV\_}$ = 1V			25		
Prop Delay, Data to Output					2		ns
Prop-Delay Temperature Coefficient					10		ps/°C
Prop-Delay Match, t_{LH} vs. t_{HL}					30		ps
Prop-Delay Skew, Drivers Within Package					150		ps
Prop-Delay Change vs. Pulse Width		Relative to 12.5ns pulse	$3V_{P-P}$, 40MHz, PW = 4ns to 21ns		20		ps
			$1V_{P-P}$, 40MHz, PW = 2.5ns to 23.5ns		90		
Prop-Delay Change vs. Common-Mode Voltage		$1V_{P-P}$, $V_{DLV\_}$ = 0 to 3V, relative to delay at $V_{DLV\_}$ = 1V			80		ps
Prop Delay, Data to High Impedance		$V_{DHV\_}$ = +1.5V, $V_{DLV\_}$ = -1.5V, both directions			1.8		ns
Prop Delay, Data to Term		$V_{DHV\_}$ = +1.5V, $V_{DLV\_}$ = -1.5V, $V_{DTV\_}$ = 0V, both directions			1.6		ns
Minimum Voltage Swing		(Note 7)			25		mV
Rise/Fall Time		$V_{DHV\_}$ = 0.2V, $V_{DLV\_}$ = 0V, 20% to 80%			0.7		ns
		$V_{DHV\_}$ = 1V, $V_{DLV\_}$ = 0V, 20% to 80%			0.7		
		$V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, 10% to 90%		1.5	2.0	2.5	
		$V_{DHV\_}$ = 4V, $V_{DLV\_}$ = 0V, R_L = 500Ω, 10% to 90%			2.6		
		$V_{DHV\_}$ = 5V, $V_{DLV\_}$ = 0V, R_L = 500Ω, 10% to 90%			3.4		
Rise/Fall-Time Matching		$V_{DHV\_}$ = 1V to 5V			±5		%
Minimum Pulse Width (Note 8)		200mV, $V_{DHV\_}$ = 0.2V, $V_{DLV\_}$ = 0V			1.8		ns
		1V, $V_{DHV\_}$ = 1V, $V_{DLV\_}$ = 0V			2.4		
		3V, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V			3.3		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +8V, V_{SS} = -5V, V_L = +3V, V_{COMPHI} = +1V, V_{COMPLO} = 0V, $V_{LDV\_}$ = 0V, LOAD EN LOW = LOAD EN HIGH = 0, T_J = +75°C. All temperature coefficients measured at T_J = +50°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
COMPARATOR (Note 9)							
DC CHARACTERISTICS (driver in high-impedance mode)							
Input Voltage Range				-2.2		+5.2	V
Differential Input Voltage		$V_{DUT\_}$ - $V_{CHV\_}$, $V_{DUT\_}$ - $V_{CLV\_}$		-7.4		+7.4	V
Hysteresis		$V_{CHV\_}$ = $V_{CLV\_}$ = 1.5V			8		mV
Input Offset Voltage		$V_{DUT\_}$ = 1.5V (V_{COMPHI} = 0.8V, V_{COMPLO} = 0.2V)	A grade			±10	mV
			B grade			±100	
Input Offset Temperature Coefficient					25		µV/°C
Common-Mode Rejection Ratio	CMRR	$V_{DUT\_}$ = 0 and 3V		60			dB
Linearity Error (Note 10)		$V_{DUT\_}$ = 1.5V				±5	mV
		$V_{DUT\_}$ = -2.2V, +5.2V				±10	
Power-Supply Rejection Ratio	PSRR	$V_{DUT\_}$ = 1.5V, supplies independently varied over full range				5	mV/V
AC CHARACTERISTICS (Note 11)							
Equivalent Input Bandwidth		Terminated (Note 12)			500		MHz
		High impedance (Note 13)			300		
Propagation Delay					3.9		ns
Prop-Delay Temperature Coefficient					4		ps/°C
Prop-Delay Match, t_{LH} to t_{HL}					120		ps
Prop-Delay Skew, Comparators Within Package		Same edges (LH and HL)			200		ps
Prop-Delay Dispersions vs. Common-Mode Voltage (Note 14)		0 to 4.9V			20		ps
		-1.9V to +4.9V			30		
Prop-Delay Dispersions vs. Overdrive		$V_{CHV\_}$ = $V_{CLV\_}$ = 0.1V to 0.9V, $V_{DUT\_}$ = $1V_{P-P}$, t_R = t_F = 500ps, 10% to 90% relative to timing at 50% point			220		ps
Prop-Delay Dispersions vs. Pulse Width		2ns to 23ns pulse width, relative to 12.5ns pulse width			±60		ps
Prop-Delay Dispersions vs. Slew Rate		0.5V/ns to 2V/ns			50		ps

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +8V, V_{SS} = -5V, V_L = +3V, V_{COMPHI} = +1V, V_{COMPLO} = 0V, $V_{LDV\_}$ = 0V, LOAD EN LOW = LOAD EN HIGH = 0, T_J = +75°C. All temperature coefficients measured at T_J = +50°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LOGIC OUTPUTS							
Reference Voltages COMPHI and COMPLO		(Note 15)		0		+3.6	V
Output High Voltage Offset		I_{OUT} = 0mA, relative to COMPHI at V_{COMPHI} = 1V				±50	mV
Output Low Voltage Offset		I_{OUT} = 0mA, relative to COMPLO at V_{COMPLO} = 0V				±50	mV
Output Resistance		$I_{CHV\_}$ = $I_{CLV\_}$ = ±10mA		40	50	60	Ω
Current Limit					25		mA
Rise/Fall Time		20% to 80%, $V_{CHV\_}$ = $1V_{P-P}$, load = T-line, 50Ω, > 1ns			0.7		ns
PASSIVE LOAD							
DC CHARACTERISTICS ($R_{DUT\_}$ ≥ 10MΩ)							
LDV_ Voltage Range				-2.2		+5.2	V
Gain				0.99		1.01	V/V
Gain Temperature Coefficient					0.02		%/°C
Offset						±100	mV
Offset Temperature Coefficient					0.02		mV/°C
Power-Supply Rejection Ratio	PSRR				10		mV/V
Output Resistance Tolerance—High Value		$I_{DUT\_}$ = ±0.2mA, $V_{LDV\_}$ = 1.5V	A grade	7.125	7.5	7.875	kΩ
			B grade	4.200	6.0	7.875	
Output Resistance Tolerance—Low Value		$I_{DUT\_}$ = ±0.1mA, $V_{LDV\_}$ = 1.5V	A grade	1.90	2.0	2.10	kΩ
			B grade	1.05	1.5	2.10	
Switch Resistance Variation		Relative to 1.5V	0 to 3V		±10		%
			Full range		±30		
Maximum Output Current (Note 16)		$V_{LDV\_}$ = -2V, $V_{DUT\_}$ = +5V			±4		mA
		$V_{LDV\_}$ = +5V, $V_{DUT\_}$ = -2V			±4		
Linearity Error, Full Range		Measured at -2.2V, +1.5V, and +5.2V (Note 16)				±25	mV
AC CHARACTERISTICS							
Settling Time, LDV_ to Output		$V_{LDV\_}$ = -2V to +5V step, $R_{DUT\_}$ = 100kΩ (Note 17)			0.5		µs
Output Transient Response		$V_{LDV\_}$ = +1.5V, $V_{DUT\_}$ = -2V to +5V square wave at 1MHz, $R_{DUT\_}$ = 50Ω			20		ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +8V, V_{SS} = -5V, V_L = +3V, V_{COMPHI} = +1V, V_{COMPLO} = 0V, $V_{LDV\_}$ = 0V, LOAD EN LOW = LOAD EN HIGH = 0, T_J = +75°C. All temperature coefficients measured at T_J = +50°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PMU SWITCHES (FORCE_, SENSE_, PMU_)						
Voltage Range			-2.2		+5.2	V
Force Switch Resistance		$V_{FORCE\_}$ = 1.5V, $I_{PMU\_}$ = ±10mA			40	Ω
Force Switch Compliance		$V_{PMU\_}$ = 6.2V, $V_{FORCE\_}$ set to make $I_{FORCE\_}$ = 30mA	25			mA
		$V_{PMU\_}$ = -3.2V, $V_{FORCE\_}$ set to make $I_{FORCE\_}$ = -30mA	25			
Force Switch Resistance Variation (Note 18)		0 to 3V		±10		%
		Full range		±30		
Sense Switch Resistance			700	1000	1300	Ω
Sense Switch Resistance Variation		Relative to 1.3V, full range		±30		%
PMU_ Capacitance		Force-and-sense switches open		5		pF
FORCE_ Capacitance				5		pF
SENSE_ Capacitance				0.2		pF
FORCE_ External Capacitance		Allowable external capacitance		2		nF
SENSE_ External Capacitance		Allowable external capacitance		1		nF
FORCE_ and SENSE_ Switching Speed		Connect or disconnect		10		µs
PMU_ Leakage		FORCE EN_ = SENSE EN_ = 0, $V_{FORCE\_}$ = $V_{SENSE\_}$ = -2.2V to +5.2V		±0.5	±5	nA
TOTAL FUNCTION						
DUT_						
Leakage, High-Impedance Mode		Load switches open, $V_{DUT\_}$ = +5.2V, $V_{CLV\_}$ = $V_{CHV\_}$ = -2.2V, $V_{DUT\_}$ = -2.2V, $V_{CLV\_}$ = $V_{CHV\_}$ = +5.2V, full range			2	µA
Leakage, Low-Leakage Mode		Full range		±1	±20	nA
Low-Leakage Recovery Time		(Note 19)		10		µs
Combined Capacitance		Term mode		2		pF
		High-impedance mode		5		
Load Resistance		(Note 20)		1		GΩ
Load Capacitance		(Note 20)		12		nF

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +8V, V_{SS} = -5V, V_L = +3V, V_{COMPHI} = +1V, V_{COMPLO} = 0V, $V_{LDV\_}$ = 0V, LOAD EN LOW = LOAD EN HIGH = 0, T_J = +75°C. All temperature coefficients measured at T_J = +50°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VOLTAGE REFERENCE INPUTS (DHV_, DTV_, DLV_, DATA_, RCV_, CHV_, CLV_, LDV_, COMPHI, COMPLO)						
Input Bias Current					±100	µA
Input Bias Current Temperature Coefficient				±200		nA/°C
Settling to Output		0.1% of full-scale step		10		µs
DIGITAL INPUTS (DATA_, RCV_, $\overline{LD}$, DIN, SCLK, $\overline{CS}$)						
Input High Voltage		(Note 21)	V_L / 2 + 0.2		+3.6	V
Input Low Voltage		(Note 21)	-0.3		V_L / 2 - 0.2	V
Input Bias Current					100	µA
SERIAL DATA OUTPUT (DOUT)						
Output High Voltage		I_{OH} = -1mA	V_L - 0.4		V_L	V
Output Low Voltage		I_{OL} = 1mA	0		+0.4	V
Output Rise and Fall Time		C_L = 10pF		1.1		ns
SCLK to DOUT Delay		C_L = 10pF	t_{DH}		t_{SCLK} - t_{DS} - 2ns	ns
SERIAL-INTERFACE TIMING (Note 22)						
SCLK Frequency					50	MHz
SCLK Pulse-Width High	t_{CH}		10			ns
SCLK Pulse-Width Low	t_{CL}		10			ns
$\overline{CS}$ Low to SCLK High Setup	t_{CSS0}		3.5			ns
SCLK High to $\overline{CS}$ Low Hold	t_{CSH0}		0			ns
$\overline{CS}$ High to SCLK High Setup	t_{CSS1}		3.5			ns
SCLK High to $\overline{CS}$ High Hold	t_{CSH1}		15			ns
DIN to SCLK High Setup	t_{DS}		3.5			ns
DIN to SCLK High Hold	t_{DH}		1			ns
$\overline{CS}$ High to $\overline{LOAD}$ Low Setup	t_{CLL}		6			ns
$\overline{LD}$ Low Hold Time	t_{LDW}		5			ns
$\overline{LD}$ High to Any Activity			0			ns
V_L Rising to $\overline{CS}$ Low		Power-on delay		2		µs
TEMP SENSOR						
Nominal Voltage		T_J = +27°C		3.00		V
Temperature Coefficient				+10		mV/°C
Output Resistance				500		Ω

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ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +8V, V_{SS} = -5V, V_L = +3V, V_{COMPHI} = +1V, V_{COMPLO} = 0V, $V_{LDV\_}$ = 0V, LOAD EN LOW = LOAD EN HIGH = 0, T_J = +75°C. All temperature coefficients measured at T_J = +50°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Positive Supply Voltage	V_{DD}	(Note 23)	7.6	8	8.4	V
Negative Supply Voltage	V_{SS}	(Note 23)	-5.25	-5	-4.75	V
Logic Supply Voltage	V_L		2.3		3.6	V
Positive Supply Current	I_{DD}	f_{OUT} = 0MHz		97	120	mA
Negative Supply Current	I_{SS}	f_{OUT} = 0MHz		99	120	mA
Logic Supply Current	I_L			0.15	0.30	mA
Static Power Dissipation		f_{OUT} = 0MHz		1.3	1.5	W
Operating Power Dissipation		f_{OUT} = 100Mbps (Note 24)		1.4		W

Note 1: All minimum and maximum specifications are 100% production tested except driver dynamic output current, which is guaranteed by design. All specifications are with DUT_ and PMU_ electrically isolated, unless otherwise noted.

Note 2: Nominal target value is 49.5Ω. Contact factory for alternate trim selections within the 45Ω to 55Ω range.

Note 3: Measured at 1.5V, relative to a straight line through 0 and 3V.

Note 4: Measured at end points, relative to a straight line through 0 and 3V.

Note 5: DUT_ is terminated with 50Ω to ground, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = 1.5V, unless otherwise specified. DATA_ and RCV_ logic levels are V_{HIGH} = 2V, V_{LOW} = 1V.

Note 6: Undershoot is any reflection of the signal back towards its starting voltage after it has reached 90% of its swing. Preshoot is any aberration in the signal before it reaches 10% of its swing.

Note 7: At the minimum voltage swing, undershoot is less than 20%. DHV_ and DLV_ references are adjusted to result in the specified swing.

Note 8: At this pulse width, the output reaches at least 90% of its nominal (DC) amplitude. The pulse width is measured at DATA_.

Note 9: With the exception of offset and gain/CMRR tests, reference input values are calibrated for offset and gain.

Note 10: Relative to a straight line through 0 and 3V.

Note 11: Unless otherwise noted, all propagation delays are measured at 40MHz, $V_{DUT\_}$ = 0 to 1V, $V_{CHV\_}$ = $V_{CLV\_}$ = +0.5V, t_R = t_F = 500ps, Z_S = 50Ω, driver in term mode with $V_{DTV\_}$ = +0.5V. Comparator outputs are terminated with 50Ω to GND. Measured from $V_{DUT\_}$ crossing calibrated CHV_/CLV_ threshold to midpoint of nominal comparator output swing.

Note 12: Terminated is defined as driver in drive mode and set to zero volts.

Note 13: High impedance is defined as driver in high-impedance mode.

Note 14: $V_{DUT\_}$ = 200mV$_{P-P}$. Propagation delay is compared to a reference time at 1.5V.

Note 15: The comparator meets all its timing specifications with the specified output conditions when the output current is less than 15mA, V_{COMPHI} > V_{COMPLO}, and V_{COMPHI} - V_{COMPLO} ≤ 1V. Higher voltage swings are valid but AC performance may degrade.

Note 16: LOAD EN LOW = LOAD EN HIGH = 1.

Note 17: Waveform settles to within 5% of final value into load 100kΩ.

Note 18: $I_{PMU\_}$ = ±2mA at $V_{FORCE\_}$ = -2.2V, +1.5V, and +5.2V. Percent variation relative to value calculated at $V_{FORCE\_}$ = +1.5V.

Note 19: Time to return to the specified maximum leakage after a 3V, 4V/ns step at DUT_.

Note 20: Load at end of 2ns transmission line; for stability only, AC performance may be degraded.

Note 21: The driver meets all of its timing specifications over the specified digital input voltage range.

Note 22: Timing characteristics with V_{LOGIC} = 3V.

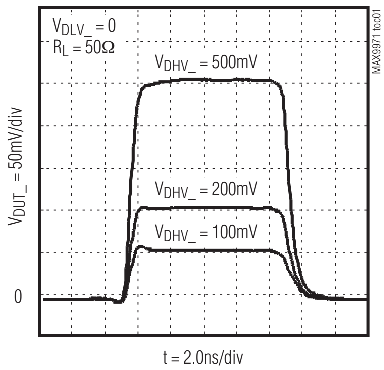
Note 23: Specifications are simulated and characterized over the full power-supply range. Production tests are performed with power supplies at typical values.

Note 24: All channels driven at 3V$_{P-P}$, load = 2ns, 50Ω transmission line terminated with 3pF.

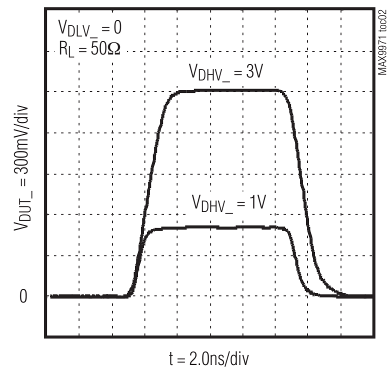
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

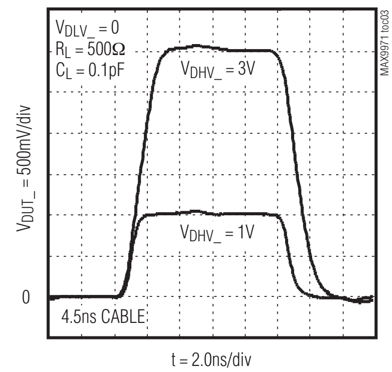
DRIVER SMALL-SIGNAL RESPONSE



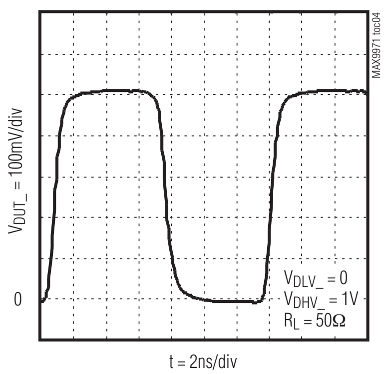
DRIVER LARGE-SIGNAL RESPONSE



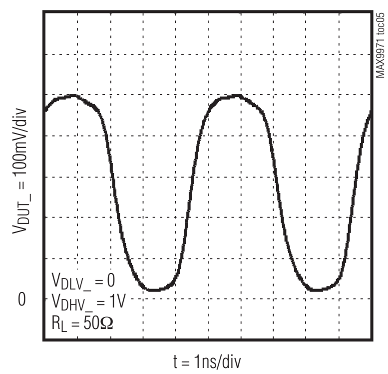
DRIVER LARGE-SIGNAL RESPONSE INTO 500Ω



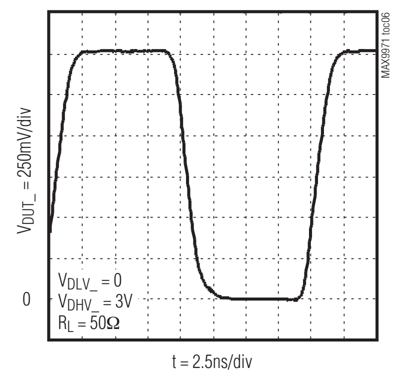
DRIVER 1V_{P-P}, 150Mbps SIGNAL RESPONSE



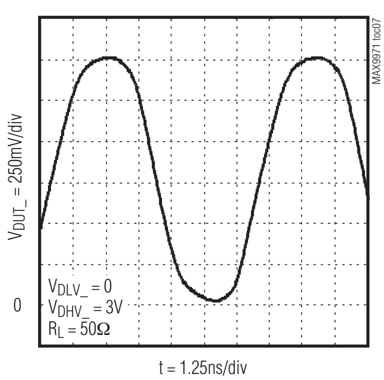
DRIVER 1V_{P-P}, 400Mbps SIGNAL RESPONSE



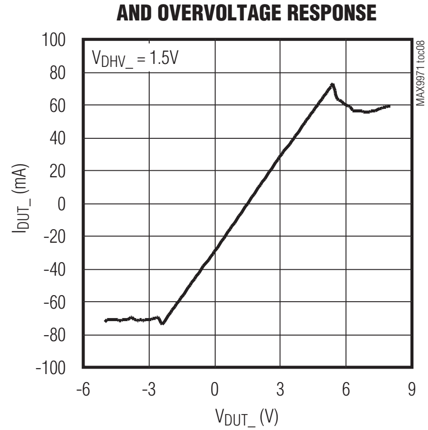
DRIVER 3V_{P-P}, 100Mbps SIGNAL RESPONSE



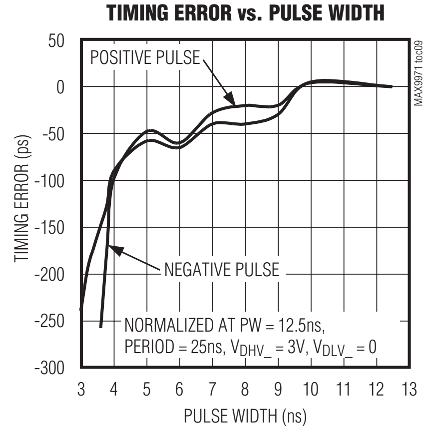
DRIVER 3V_{P-P}, 250Mbps SIGNAL RESPONSE



DRIVER DC CURRENT-LIMIT AND OVERVOLTAGE RESPONSE



DRIVER 3V TRAILING-EDGE TIMING ERROR vs. PULSE WIDTH

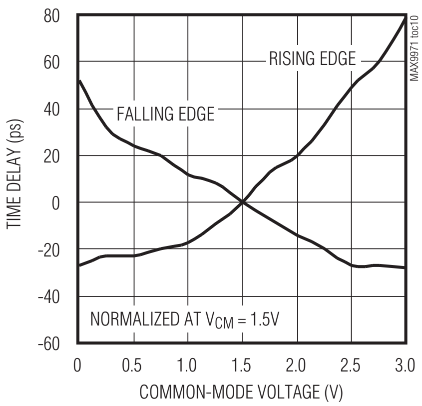


Quad, Ultra-Low-Power, 300Mbps ATE Drivers/Comparators

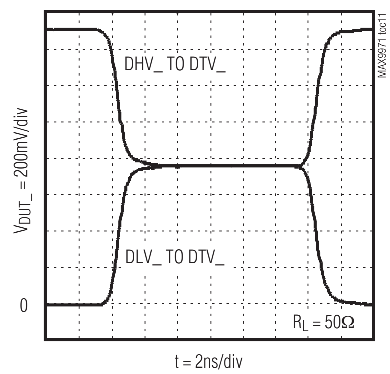
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

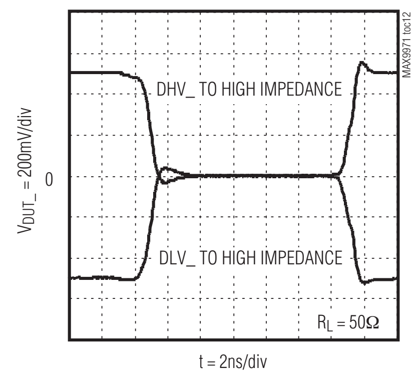
DRIVER TIME DELAY vs. COMMON-MODE VOLTAGE



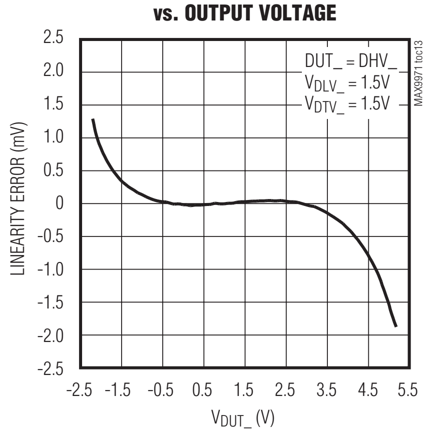
DRIVE-TO-TERM TRANSITION



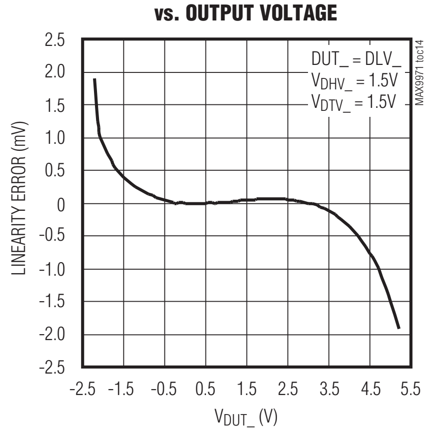
DRIVE-TO-HIGH-IMPEDANCE TRANSITION



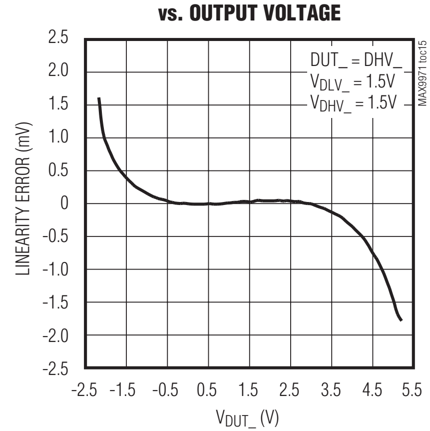
DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



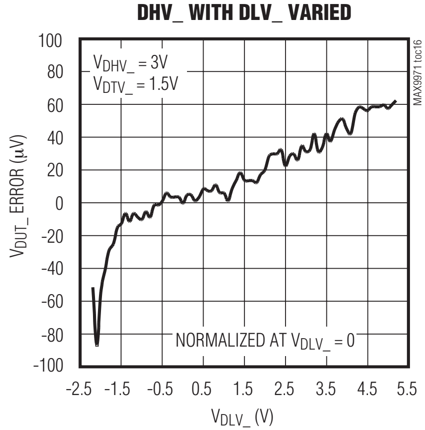
DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



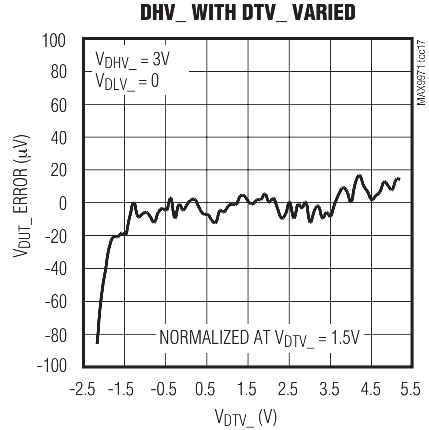
DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



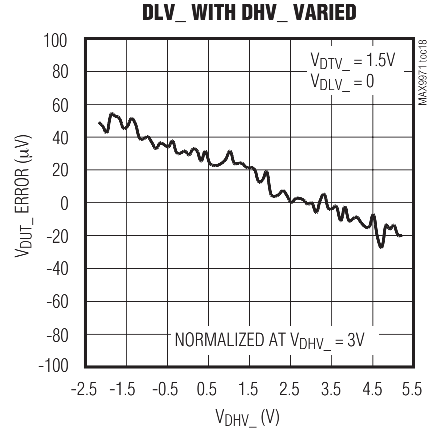
CROSSTALK, DUT_ DRIVEN BY DHV_ WITH DLV_ VARIED



CROSSTALK, DUT_ DRIVEN BY DHV_ WITH DTV_ VARIED



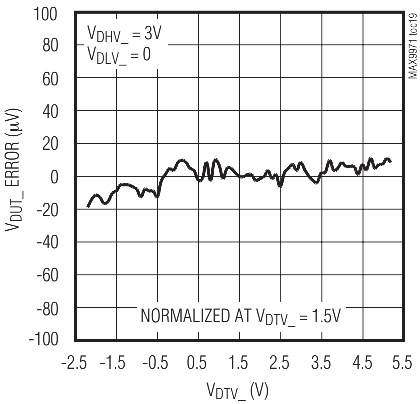
CROSSTALK, DUT_ DRIVEN BY DLV_ WITH DHV_ VARIED



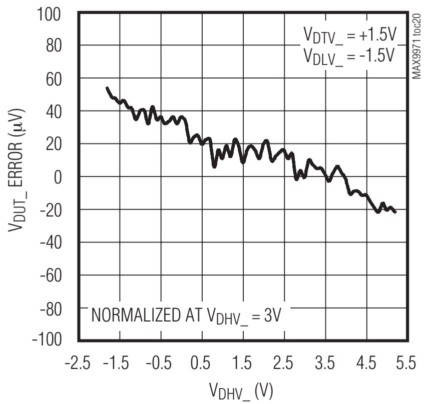
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

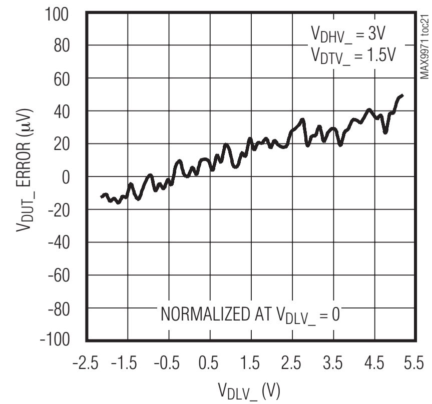
CROSSTALK, DUT_ DRIVEN BY DLV_ WITH DTV_ VARIED



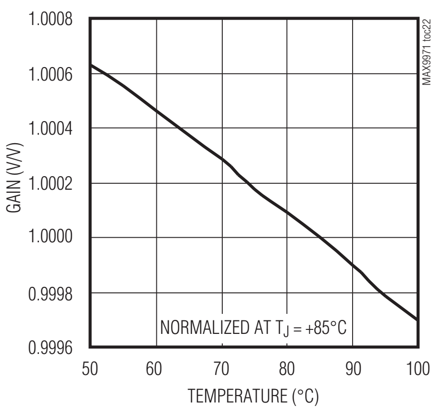
CROSSTALK, DUT_ DRIVEN BY DTV_ WITH DHV_ VARIED



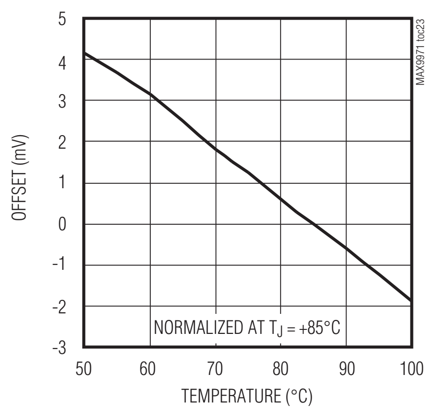
CROSSTALK, DUT_ DRIVEN BY DTV_ WITH DLV_ VARIED



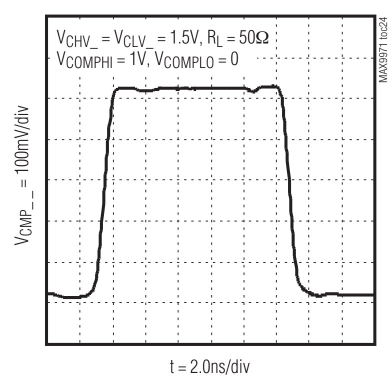
DRIVER GAIN vs. TEMPERATURE



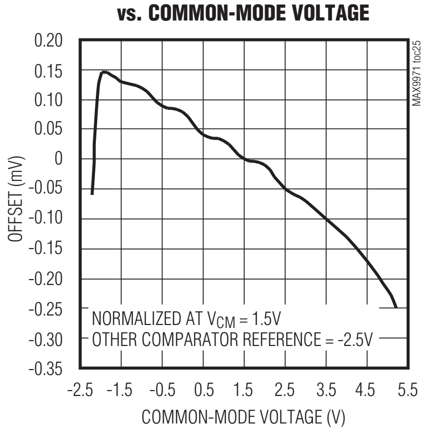
DRIVER OFFSET vs. TEMPERATURE



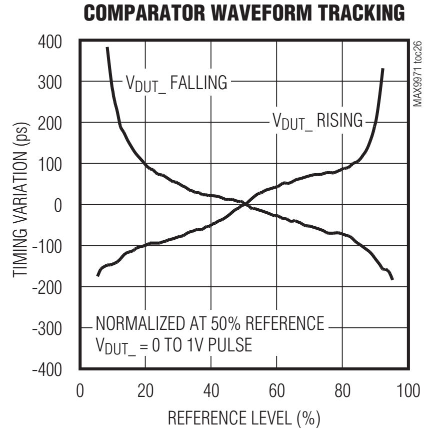
COMPARATOR RESPONSE TO 0 TO 3V SIGNAL



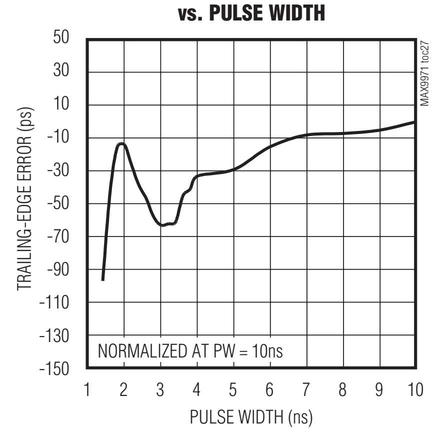
COMPARATOR OFFSET vs. COMMON-MODE VOLTAGE



COMPARATOR WAVEFORM TRACKING



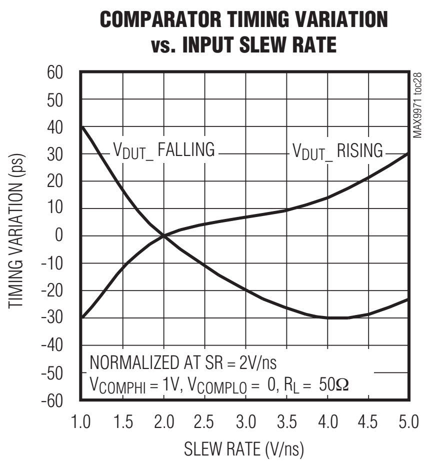
COMPARATOR TIMING VARIATION vs. PULSE WIDTH

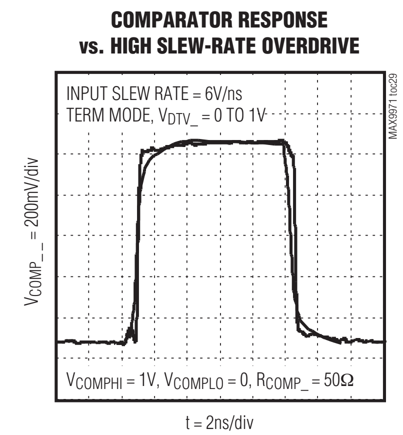


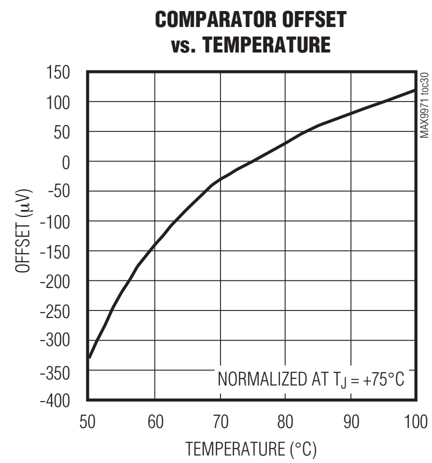
Quad, Ultra-Low-Power, 300Mbps ATE Drivers/Comparators

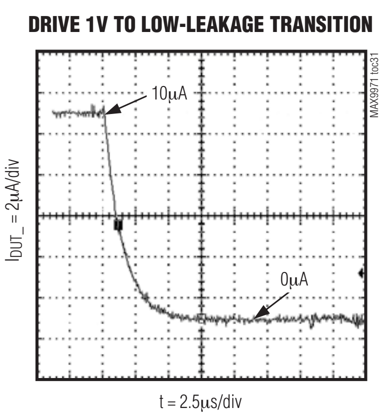
Typical Operating Characteristics (continued)

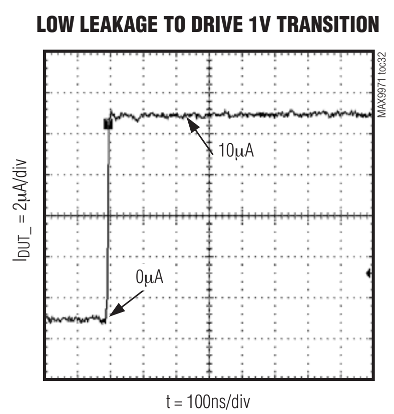
(T_A = +25°C, unless otherwise noted.)

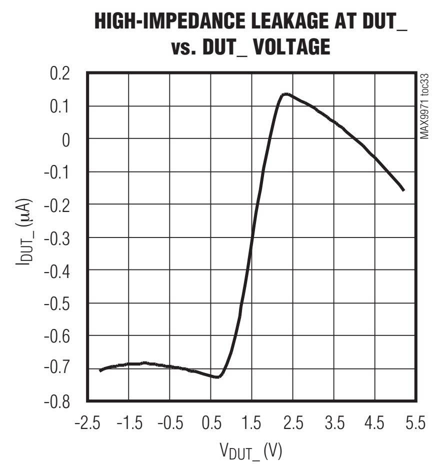


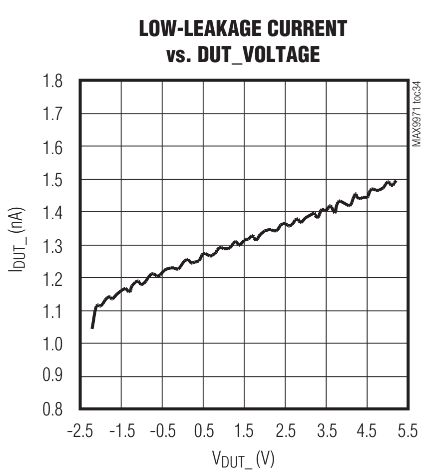


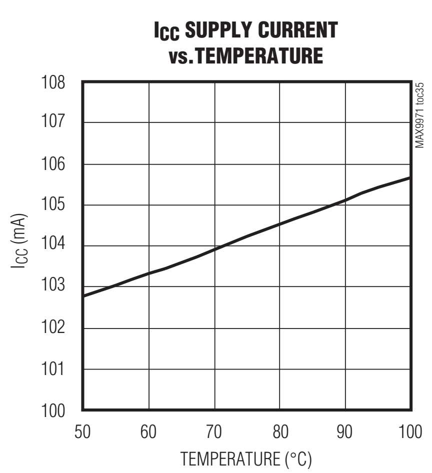


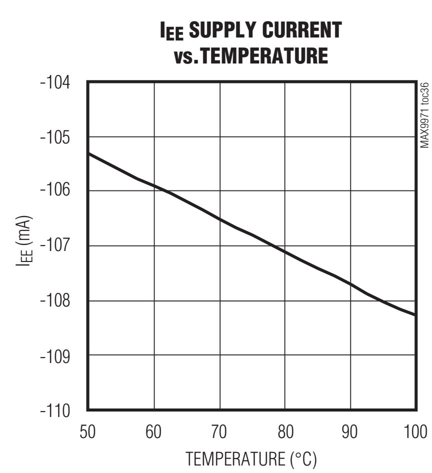








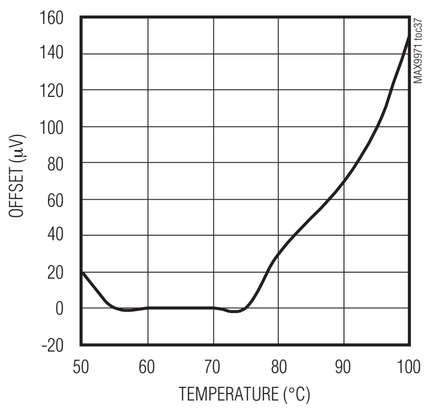




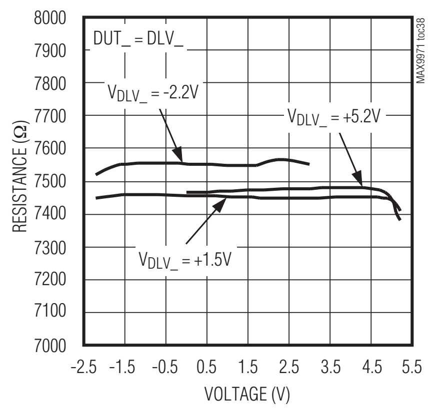
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

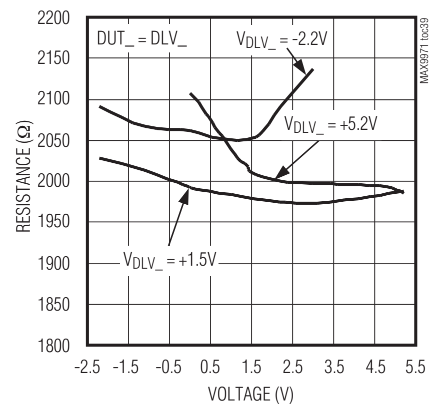
PASSIVE LOAD OFFSET vs. TEMPERATURE



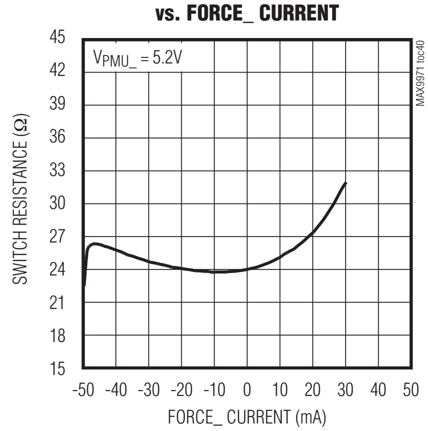
PASSIVE LOAD HIGH RESISTOR vs. VOLTAGE



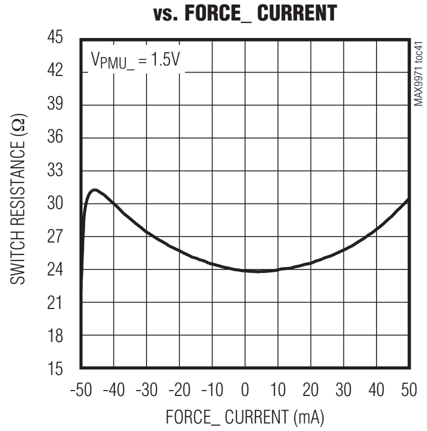
PASSIVE LOAD LOW RESISTOR vs. VOLTAGE



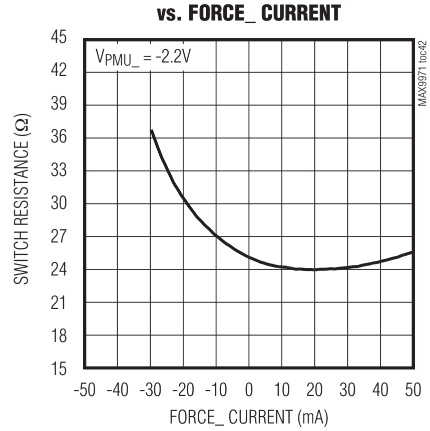
PMU_ FORCE_ SWITCH RESISTANCE vs. FORCE_ CURRENT



PMU_ FORCE_ SWITCH RESISTANCE vs. FORCE_ CURRENT



PMU_ FORCE_ SWITCH RESISTANCE vs. FORCE_ CURRENT



Pin Description

PIN	NAME	FUNCTION
1	DATA1	Channel 1 Multiplexer Control Input. Selects driver 1 input from DHV1 or DLV1 in drive mode. See Table 1 and Figure 2.
2	RCV1	Channel 1 Multiplexer Control Input. Sets channel 1 mode to drive or receive. See Table 1 and Figure 2.
3, 8, 13, 18, 51	GND	Analog Ground
4	CMPH1	Channel 1 High-Side Comparator Output
5	CMPL1	Channel 1 Low-Side Comparator Output
6	DATA2	Channel 2 Multiplexer Control Input. Selects driver 2 input from DHV2 or DLV2 in drive mode. See Table 1 and Figure 2.
7	RCV2	Channel 2 Multiplexer Control Input. Sets channel 2 mode to drive or receive. See Table 1 and Figure 2.
9	CMPH2	Channel 2 High-Side Comparator Output
10	CMPL2	Channel 2 Low-Side Comparator Output
11	CMPL3	Channel 3 Low-Side Comparator Output
12	CMPH3	Channel 3 High-Side Comparator Output
14	RCV3	Channel 3 Multiplexer Control Input. Sets channel 3 mode to drive or receive. See Table 1 and Figure 2.
15	DATA3	Channel 3 Multiplexer Control Input. Selects driver 3 input from DHV3 or DLV3 in drive mode. See Table 1 and Figure 2.
16	CMPL4	Channel 4 Low-Side Comparator Output
17	CMPH4	Channel 4 High-Side Comparator Output
19	RCV4	Channel 4 Multiplexer Control Input. Sets channel 4 mode to drive or receive. See Table 1 and Figure 2.
20	DATA4	Channel 4 Multiplexer Control Input. Selects driver 4 input from DHV4 or DLV4 in drive mode. See Table 1 and Figure 2.
21	DHV4	Channel 4 Driver High Voltage Input
22	DLV4	Channel 4 Driver Low Voltage Input
23	DTV4	Channel 4 Driver Termination Voltage Input
24	CHV4	Channel 4 Threshold Voltage Input for High-Side Comparator
25	CLV4	Channel 4 Threshold Voltage Input for Low-Side Comparator
26	DHV3	Channel 3 Driver High Voltage Input
27	DLV3	Channel 3 Driver Low Voltage Input
28	DTV3	Channel 3 Driver Termination Voltage Input
29	CHV3	Channel 3 Threshold Voltage Input for High-Side Comparator
30	CLV3	Channel 3 Threshold Voltage Input for Low-Side Comparator
31	DGND	Digital Ground Connection
32	DOUT	Serial-Interface Data Output
33	$\overline{LD}$	Load Input. Latches data from the serial input register to the control register on rising edge. Transparent when low.
34	DIN	Serial-Interface Data Input
35	SCLK	Serial Clock
36	$\overline{CS}$	Chip Select
37	SENSE4	Channel 4 PMU Sense Connection
38	FORCE4	Channel 4 PMU Force Connection

Pin Description (continued)

PIN	NAME	FUNCTION
39	SENSE3	Channel 3 PMU Sense Connection
40	FORCE3	Channel 3 PMU Force Connection
41	TEMP	Temperature Sensor Output
42, 47, 52, 56, 60	V_{DD}	Positive Power-Supply Input
43	DUT4	Channel 4 Device-Under-Test Connection. Driver, comparator, and load I/O node for channel 4.
44	PMU4	Channel 4 Parametric Measurement Connection. PMU switch I/O node for channel 4.
45, 50, 53, 57	V_{SS}	Negative Power-Supply Input
46	V_L	Logic Power-Supply Input
48	DUT3	Channel 3 Device-Under-Test Connection. Driver, comparator, and load I/O node for channel 3.
49	PMU3	Channel 3 Parametric Measurement Connection. PMU switch I/O node for channel 3.
54	PMU2	Channel 2 Parametric Measurement Connection. PMU switch I/O node for channel 2.
55	DUT2	Channel 2 Device-Under-Test Connection. Driver, comparator, and load I/O node for channel 2.
58	PMU1	Channel 1 Parametric Measurement Connection. PMU switch I/O node for channel 1.
59	DUT1	Channel 1 Device-Under-Test Connection. Driver, comparator, and load I/O node for channel 1.
61	FORCE2	Channel 2 PMU Force Connection
62	SENSE2	Channel 2 PMU Sense Connection
63	FORCE1	Channel 1 PMU Force Connection
64	SENSE1	Channel 1 PMU Sense Connection
65	COMPLO	Comparator Output-Low Voltage Reference Input
66	COMPHI	Comparator Output-High Voltage Reference Input
67	LDV4	Channel 4 Load Voltage Input
68	LDV3	Channel 3 Load Voltage Input
69	LDV2	Channel 2 Load Voltage Input
70	LDV1	Channel 1 Load Voltage Input
71	CLV2	Channel 2 Threshold Voltage Input for Low-Side Comparator
72	CHV2	Channel 2 Threshold Voltage Input for High-Side Comparator
73	DTV2	Channel 2 Driver Termination Voltage Input
74	DLV2	Channel 2 Driver Low Voltage Input
75	DHV2	Channel 2 Driver High Voltage Input
76	CLV1	Channel 1 Threshold Voltage Input for Low-Side Comparator
77	CHV1	Channel 1 Threshold Voltage Input for High-Side Comparator
78	DTV1	Channel 1 Driver Termination Voltage Input
79	DLV1	Channel 1 Driver Low Voltage Input
80	DHV1	Channel 1 Driver High Voltage Input
—	EP	Exposed Pad. Leave unconnected or connect to V_{SS}.

Quad, Ultra-Low-Power, 300Mbps ATE Drivers/Comparators

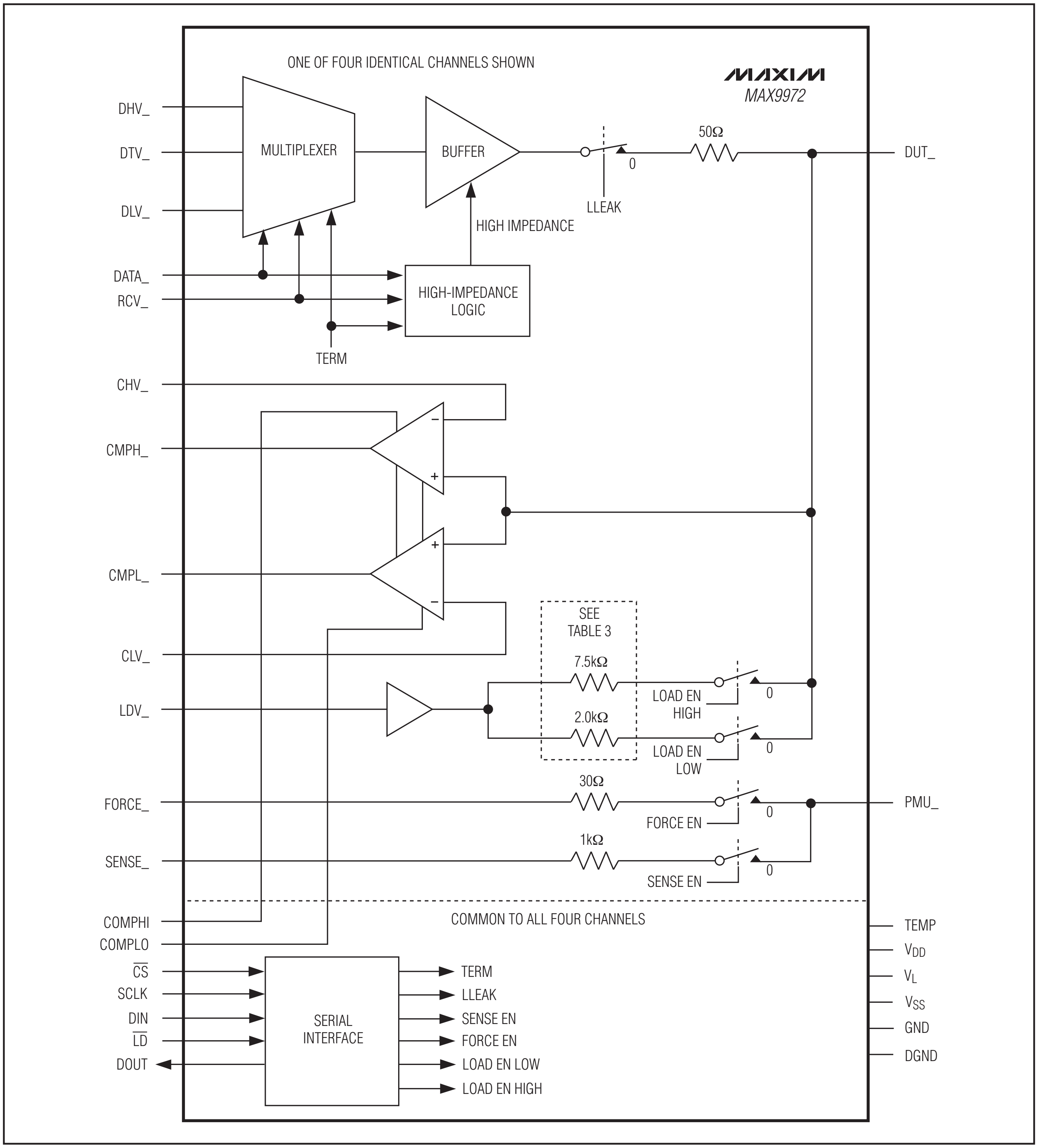


Figure 1. Block Diagram

Detailed Description

The MAX9972 is a four-channel, pin-electronics ICs for automated test equipment that includes, for each channel, a three-level pin driver, a window comparator, a passive load, and a Kelvin instrument connection (Figure 1). All functions feature a -2.2V to +5.2V operating range and the drivers include both high-impedance and active-termination (3rd-level drive) modes. The comparators feature programmable output voltages, allowing optimization for different CMOS interface standards. The loads have selectable output resistance for optimizing DUT current loading. The Kelvin paths allow accurate connection of an instrument with ±25mA source/sink capability. Additionally, the MAX9972 offers a low-leakage mode that reduces DUT_ leakage current to less than 20nA.

The MAX9972 is available in two grades. The A-grade devices provide tighter tolerances for driver gains and offsets, comparator offsets, and load resistor values. This allows reference levels to be shared across multiple channels in cost-sensitive systems. The B-grade devices are intended for system designs that incorporate independent reference levels for each channel.

Each of the four channels feature single-ended CMOS-compatible inputs, DATA_ and RCV_, for control of the driver signal path (Figure 2). The MAX9972 modal operation is programmed through a 3-wire, low-voltage CMOS-compatible serial interface.

Output Driver

The driver input is a high-speed multiplexer that selects one of three voltage inputs; DHV_, DLV_, or DTV_. This switching is controlled by high-speed inputs DATA_ and RCV_, and mode-control bit TERM (Table 1). DATA_ and RCV_ are single-ended inputs with threshold levels equal to V_L / 2. Each channel's threshold levels are independently generated to minimize crosstalk.

DUT_ can be toggled at high speed between the buffer output and high-impedance mode, or it can be placed into low-leakage mode (Figure 2, Table 1). High-speed input RCV_ and mode-control bits TERM and LLEAK control these modes. In high-impedance mode, the bias current at DUT_ is less than 2µA over the -2.2V to +5.2V range, while the node maintains its ability to track high-speed signals. In low-leakage mode, the bias current at DUT_ is further reduced to less than 20nA, and signal tracking slows.

The nominal driver output resistance is 50Ω. Custom resistance values from 45Ω to 51Ω are possible; consult factory for further information.

Table 1. Driver Channel Control Signals

EXTERNAL CONNECTIONS		INTERNAL CONTROL BITS		DRIVER OUTPUT	DRIVER MODE
RCV_	**DATA_**	**TERM**	**LLEAK**		
0	0	X	0	DUT_ = DLV_	Drive
0	1	X	0	DUT_ = DHV_	Drive
1	X	0	0	High Impedance	Receive
1	X	1	0	DUT_ = DTV_	Receive
X	X	X	1	Low Leak	Low Leakage

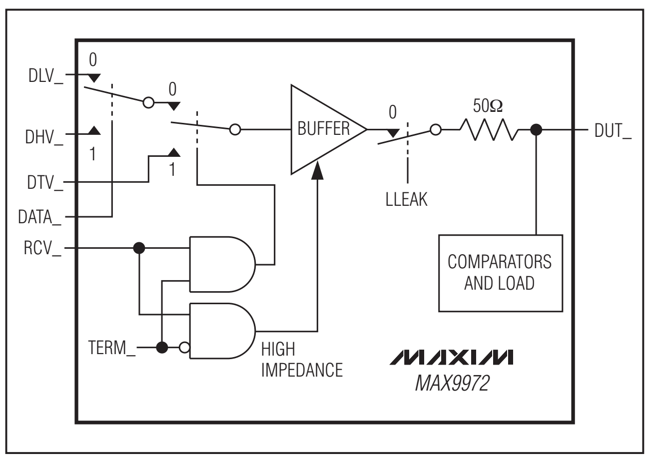


Figure 2. Multiplexer and Driver Channel

Comparators

The MAX9972 provides two independent high-speed comparators for each channel. Each comparator has one input connected internally to DUT_ and the other input connected to either CHV_ or CLV_ (see Figure 1). Comparator outputs are a logical result of the input conditions, as indicated in Table 2.

The comparator output voltages are easily interfaced to a wide variety of logic standards. Use buffered inputs COMPHI and COMPLO to set the high and low output voltages. For correct operation, COMPHI should be greater than or equal to COMPLO. The comparator 50Ω output impedance provides source termination (Figure 3).

Passive Load

The MAX9972 channels each feature a passive load consisting of a buffered input voltage, LDV_, connected to DUT_ through two resistive paths (Figure 1). Each path connects to DUT_ individually by a switch controlled through the serial interface. Programming options include none (load disconnected), either, or both paths connected. The resistor values vary depending on the accuracy grade of the device, as shown in Table 3. The loads facilitate fast open/short testing in conjunction with the comparator, and pullup of open-drain DUT_ outputs.

Parametric Switches

Each of the four MAX9972 channels provides force-and-sense paths for connection of a PMU or other DC resource to the device-under-test (Figure 1). Each force-and-sense switch is independently controlled though the serial interface providing maximum application flexibility. PMU_ and DUT_ are provided on separate pins allowing designs that do not require the parametric switch feature to avoid the added capacitance of PMU_. It also allows PMU_ to connect to DUT_ either directly or with an impedance-matching network.

Low-Leakage Mode, LLEAK

Asserting LLEAK through the serial port places the MAX9972 into a very-low-leakage state (see the *Electrical Characteristics* table). This mode is convenient for making IDDQ and PMU measurements without the need for an output disconnect relay. LLEAK control is independent for each channel.

When DUT_ is driven with a high-speed signal while LLEAK is asserted, the leakage current momentarily increases beyond the limits specified for normal operation. The low-leakage recovery specification in the *Electrical Characteristics* table indicates device behavior under this condition.

Table 2. Comparator Logic

DUT_ > CHV_	DUT_ > CLV_	CMPH_	CMPL_
0	0	0	0
0	1	0	1
1	0	1	0
1	1	1	1

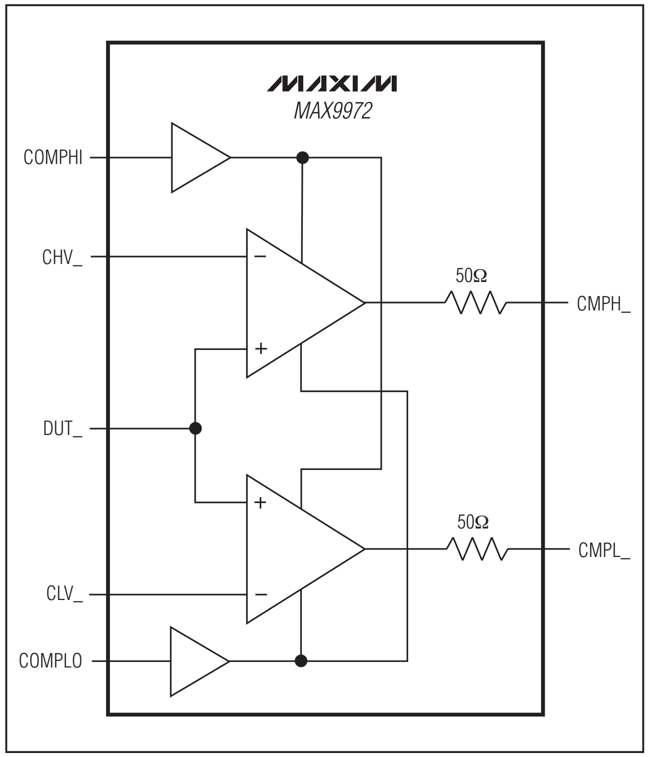


Figure 3. Complementary 50Ω Comparator Outputs

Table 3. Passive Load Resistance Values

ACCURACY GRADE	HIGH RESISTOR (kΩ)	LOW RESISTOR (kΩ)
A	7.5	2
B	6	1.5

Temperature Monitor

Each device supplies a single temperature output signal, TEMP, that asserts a nominal 3.43V output voltage at a +70°C (343K) die temperature. The output voltage increases proportionately with temperature at a rate of 10mV/°C. The temperature sensor output impedance is 500Ω, typical.

Serial Interface and Device Control

A CMOS-compatible serial interface controls the MAX9972 modes (Figure 4). Control data flow into a 12-bit shift register (LSB first) and are latched when $\overline{CS}$ is taken high. Data from the shift register are then loaded to the per-channel control latches as determined by bits D8–D11, and indicated in Figure 4 and Table 4.

The latches contain the six mode bits for each channel of the device. The mode bits, in conjunction with external inputs DATA_ and RCV_, manage the features of each channel. Transfer data asynchronously from the input registers to the channel registers by forcing $\overline{LD}$ low. With $\overline{LD}$ always low, data transfer on the rising edge of $\overline{CS}$.

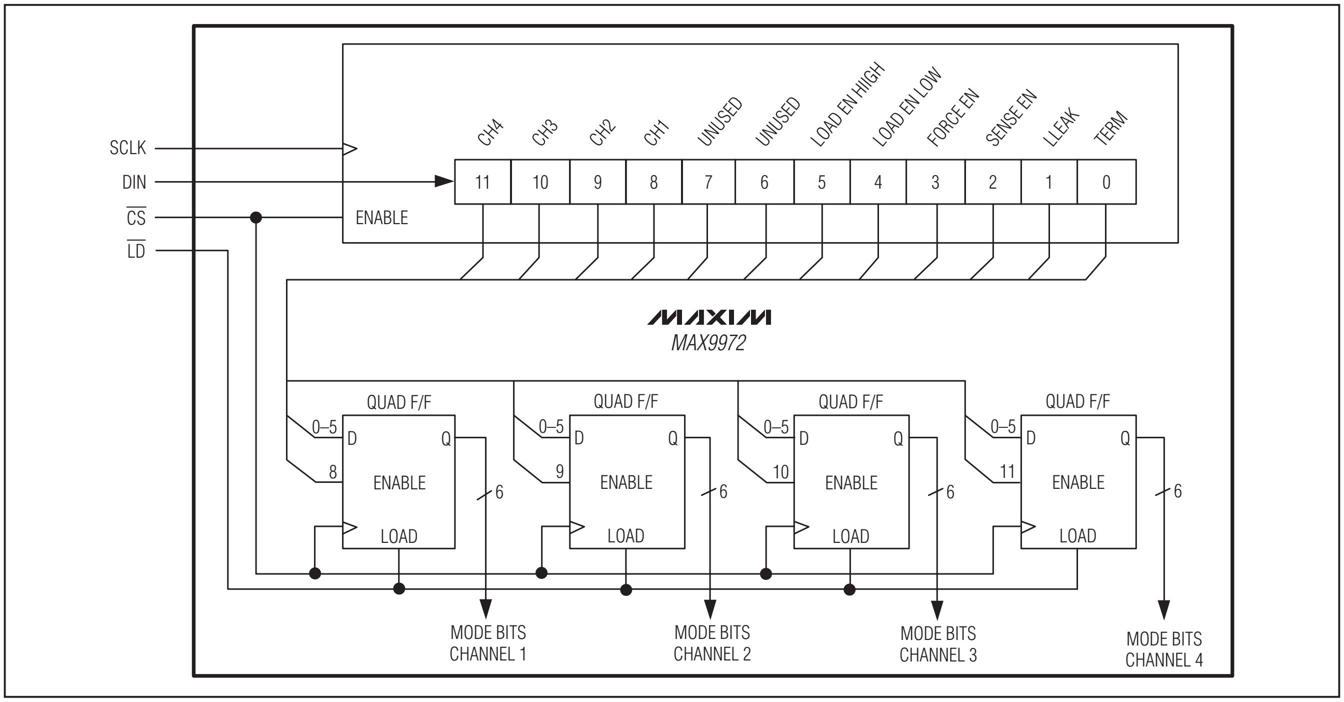


Figure 4. Serial Interface

Table 4. Control Register Bit Functions

BIT	NAME	FUNCTION	BIT STATE		POWER-UP STATE
			0	1	
0	TERM	Term Mode Control	High Impedance	Term Mode	0
1	LLEAK	Assert Low-Leakage Mode	Term Mode	Low Leakage	0
2	SENSE EN	Enable Sense Switch	Disabled	Enabled	0
3	FORCE EN	Enable Force Switch	Disabled	Enabled	0
4	LOAD EN LOW	Enable Low Load Resistor	Disabled	Enabled	0
5	LOAD EN HIGH	Enable High Load Resistor	Disabled	Enabled	0
6	—	Unused	X	X	0
7	—	Unused	X	X	0
8	CH1	Update Channel 1 Control Register	Disabled	Enabled	1
9	CH2	Update Channel 2 Control Register	Disabled	Enabled	1
10	CH3	Update Channel 3 Control Register	Disabled	Enabled	1
11	CH4	Update Channel 4 Control Register	Disabled	Enabled	1

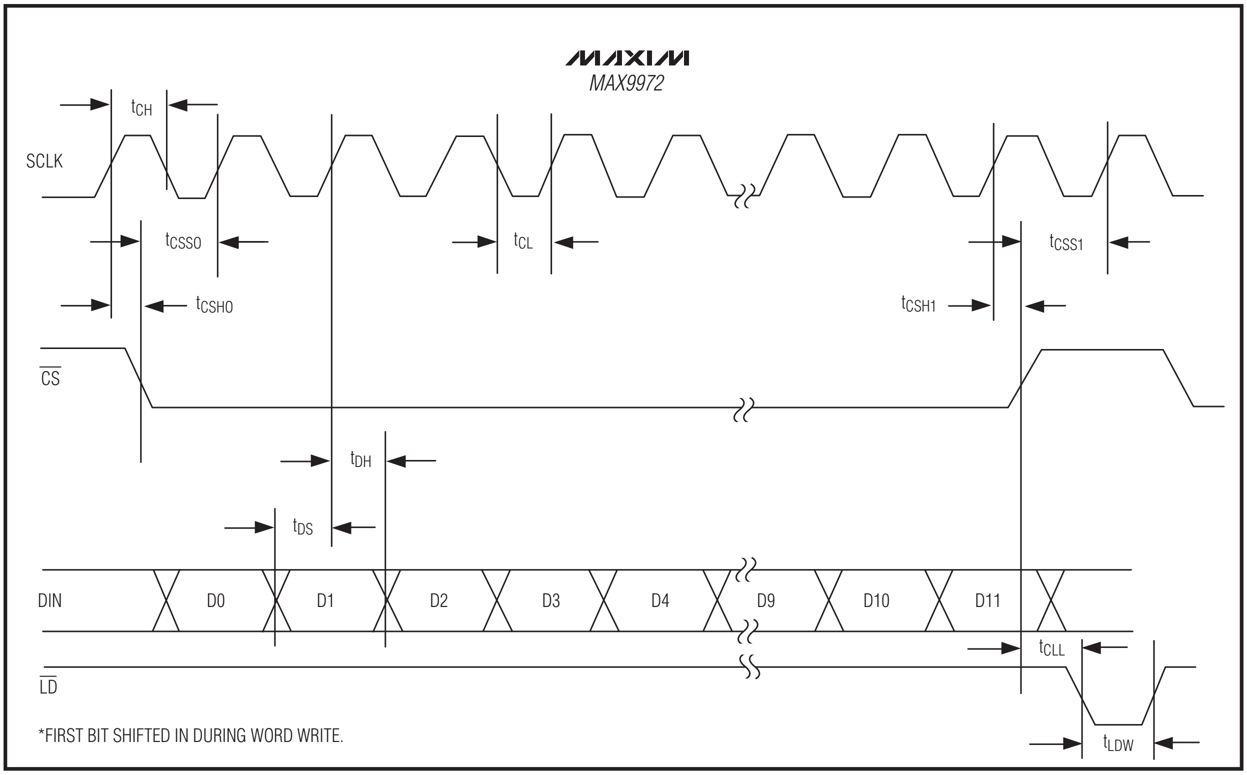


Figure 5. Serial-Interface Timing

Heat Removal

With adequate airflow, no external heat sinking is needed under most operating conditions. If excess heat must be dissipated through the exposed pad, solder it to circuit board copper. The exposed pad must be either left unconnected, isolated, or connected to V_{SS}.

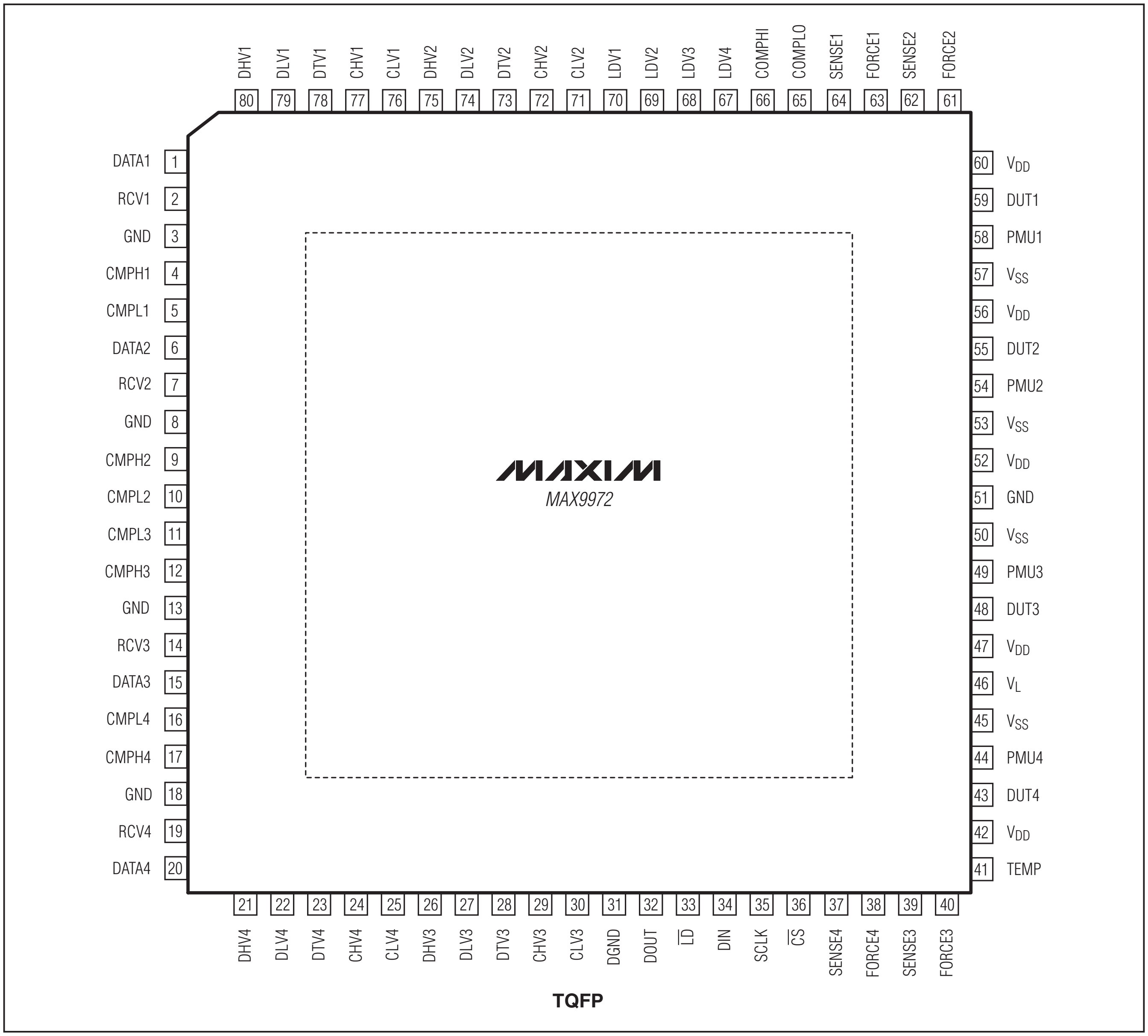
Power Minimization

To minimize power consumption, activate only the needed channels. Each channel placed in low-leakage mode saves approximately 240mW.

Chip Information

PROCESS: BiCMOS

Pin Configuration



Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
80 TQFP-EP	C80E-4	21-0115

Quad, Ultra-Low-Power, 300Mbps ATE Drivers/Comparators

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/06	Initial release	—
1	6/09	Changed driver offset max value in *Electrical Characteristics* table and removed all references to MAX9971	1–22