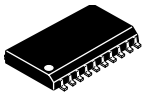
Document Number: MC34670
Rev. 3.0, 12/2006

RoHS

IEEE 802.3af PD With Current Mode Switching Regulator

34670

POWER OVER ETHERNET



EG SUFFIX (PB-FREE)
98ASB42343B
20-PIN SOICW

The 34670 combines a Power Interface Port for IEEE 802.3af Powered Devices (PD) and a high performance current mode switching regulator. It allows a designer to build PDs with a minimum of external components by means of integrating the required IEEE 802.3af functions and all functions necessary to build a high efficiency DC/DC converter.

On the PD side the 34670 fully supports the IEEE802.3af standard and provides complete signature and power classification functions. It controls inrush current limiting and incorporates adjustable undervoltage lockout. The switching regulator provides excellent line and load regulation. It drives an external Power MOSFET with sense resistor.

Features

- Integrated IEEE 802.3af Compliant Interface
- Signature Detection and Classification Functionality
- Integrated Isolation Switch
- Programmable Inrush Current Limiting Control
- Adjustable Undervoltage Lockout
- Input Voltage Range up to 80 V
- Current Mode Control
- Adjustable Oscillator
- Leading Edge Blanking
- Internal Slope Compensation Circuitry
- Input Overvoltage Protection
- 50% Duty Cycle Limitation
- Pb-Free Packaging Designated by Suffix Code EG

ORDERING INFORMATION		
Device	**Temperature Range (T_A)**	**Package**
MCZ34670EG/R2	-40°C to 85°C	20 SOICW

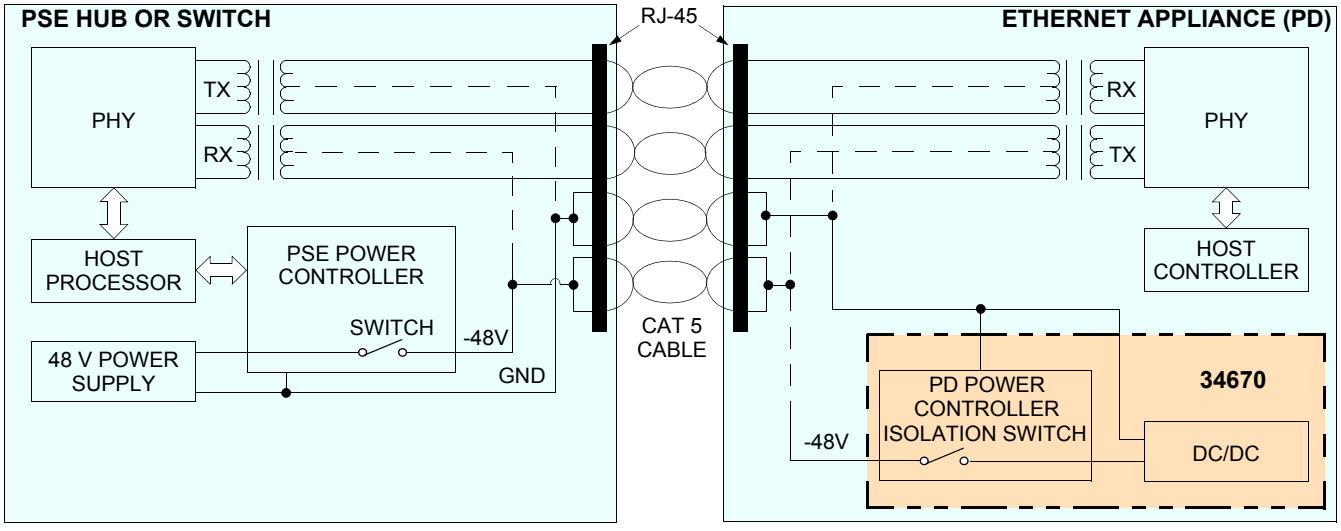


Figure 1. 34670 Simplified Application Diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

freescale semiconductor

INTERNAL BLOCK DIAGRAM

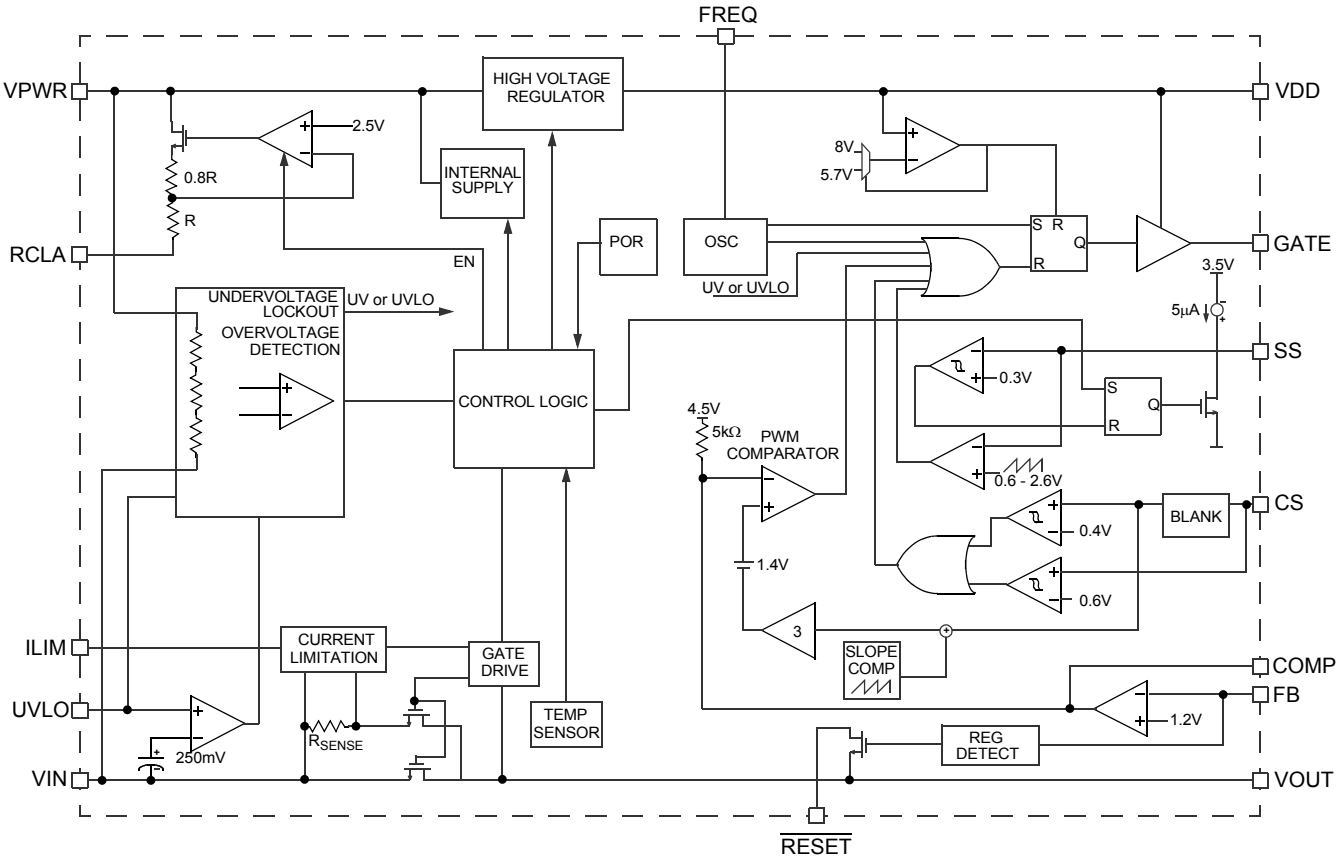


Figure 2. 34670 Simplified Internal Block Diagram

PIN CONNECTIONS

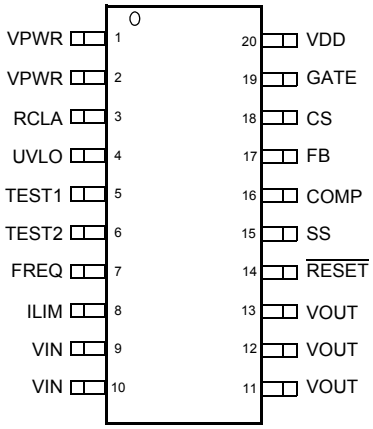


Figure 3. 34670 Pin Connections

Table 1. 34670 Pin Definitions

Pin Number	Pin Name	Formal Name	Definition
1, 2	VPWR	Positive Supply Voltage Input	This is the most positive power supply input. The load connects between this pin and the V_{OUT} pin.
3	RCLA	Classification Resistor	Connect a resistor between RCLA and V_{IN} to select the class of the PD.
4	UVLO	Undervoltage Lookout	Used to adjust the undervoltage lookout threshold voltage, connected to V_{IN} to use the default threshold voltage.
5	TEST1	Test pins	Connect to V_{IN} in application mode.
6	TEST2		
7	FREQ	Frequency Adjustment	Adjusts the internal oscillator frequency by connecting a resistor between FREQ and V_{IN}.
8	ILIM	Inrush Current Limit	Used to adjust the inrush current limit of the isolation switch, add a resistor between ILIM and V_{IN}.
9	VIN	Negative Supply Voltage	This is the most negative power supply input.
10	VIN		
11, 12	VOUT	Output Voltage	This pin is the drain of the internal Power MOSFET (high current path).
13	VOUT	Output Voltage	This pin is the drain of the internal Power MOSFET (low current path).
14	RESET	RESET Output (active low)	This is an active-low RESET output signal. This pin is referenced to V_{OUT}.
15	SS	Soft Start Input	Connect an external capacitor to SS. The internal current source charges the capacitor and generates a soft-start ramp.
16	COMP	Compensation Pin	COMP is the output of the error amplifier and is available for feedback compensation. COMP is pulled-up by an internal 5.0 kΩ resistor to 5.0 V.
17	FB	Feedback Input	This is the inverting input of the error amplifier. In non-isolated applications it's connected to the secondary output through a resistor divider.
18	CS	Current Sense	The current sense pin CS senses a voltage that is proportional to the current through the sense resistor.
19	GATE	Gate Driver Output	GATE drives the gate of the external power MOSFET. GATE sources and sinks up to 1.0 A.
20	VDD	V_{DD} Output	V_{DD} mainly supplies the gate of the external power MOSFET. Connect a capacitor from V_{DD} to V_{OUT}.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to V_{IN} unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value		Unit
ELECTRICAL RATINGS				
Power Supply Voltage	V_{PWR}	-0.3 to 80		V
Supply Current	I_{PWR}	18		mA
VOUT Pins Voltage	V_{OUT}	-0.3 to (V_{PWR} + 0.3)		V
UVLO Voltage	V_{UVLO}	-0.3 to 10		V
RCLA Voltage	V_{RCLA}	-0.3 to 5.0		V
ILIM Voltage	V_{ILIM}	-0.3 to 5.0		V
FREQ Voltage	V_{FREQ}	-0.3 to 5.0		V
		With respect to:		
		V_{OUT}[2]	**V_{IN}**[3]	
FB, COMP Voltage	V_{FB}, V_{COMP}	-0.3 to 5.0	-0.3 to 80	V
SS Voltage	V_{SS}	-0.3 to 5.0	-0.3 to 80	V
VDD Voltage	V_{DD}	-0.3 to 16	-0.3 to 80	V
GATE Voltage	V_{GATE}	-0.3 to (V_{DD} + 0.3)	-0.3 to 80	V
CS Voltage	V_{CS}	-0.3 to 5.0	-0.3 to 80	V
$\overline{\text{RESET}}$ Voltage	V_{RESET}	-0.3 to 15	-0.3 to 80	
ESD Voltage [1] Human Body Model Machine Model	V_{ESD1} V_{ESD2}	±2000 ±200		V
Output Clamp Energy	E_{CL}	12		mJ

NotesNotes

1. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω). ESD2 testing is performed in accordance with the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω).
2. Measured value relative to V_{OUT}
3. Measured value relative to V_{IN}

Table 2. Maximum Ratings (continued)

All voltages are with respect to V_{IN} unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
THERMAL RATINGS			
Operating Temperature Ambient (4) Junction (8), (9)	 T_A T_J	 -40 to 85 120	°C
Storage Temperature	T_{STG}	-65 to 150	°C
Power Dissipation (T_A = 25 °C) (7)	P_D	800	mW
Thermal Resistance Junction to Ambient 20LD SOIC W/B Package (9)	 $R_{\theta JA}$ $R_{\theta JB}$	 103 47	°C/W
Peak Package Reflow Temperature During Reflow (5), (6)	T_{PPRT}	Note 6	°C
Thermal Shutdown Temperature	T_{SHUT}	180	°C
Thermal Shutdown Recovery Temperature	T_{HYST}	150	°C

NotesNotes

4. The limiting factor is junction temperature; taking into account the power dissipation, thermal resistance, and heat sinking.
5. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
6. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL),
   Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.
7. Maximum power dissipation at indicated ambient temperature in free air with no heatsink used.
8. For T_A = 85°C and P_D = 700 mW and $R_{\theta JB}$ = 47°C/W.
9. Measured with 4 layers 2s2p JEDEC std. PCB.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions 30 V ≤ V_{PWR} ≤ 60 V, -40°C ≤ T_A ≤ 85°C, V_{IN} = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SIGNATURE DETECTION					
Input Offset Current (1.4 V ≤ V_{PORT} ≤ 9.5 V)	I_{OFFSET}	—	—	10	μA
Differential Input Resistance (1.4 V ≤ V_{PORT} ≤ 9.5 V)	R_{DIFF}	600	—	—	kΩ
CLASSIFICATION					
Classification Current (13.5 V ≤ V_{PORT} ≤ 20 V)	I_{CLASS}				mA
Class 0: R_{CLASS} = 4.42 kΩ		0	—	4.0	
Class 1: R_{CLASS} = 475 Ω		9.0	—	12	
Class 2: R_{CLASS} = 261 Ω		17	—	20	
Class 3: R_{CLASS} = 169 Ω		26	—	30	
Class 4: R_{CLASS} = 113 Ω		36	—	44	
Classification Current Limit	$I_{CLASS(LIM)}$	—	—	50	mA
RCLA Reference Voltage (13.5 V ≤ V_{PORT} ≤ 20 V)	V_{RCLA}	4.0	4.5	5.0	V
INRUSH CURRENT LIMITATION (37 V ≤ V_{PORT} ≤ 60 V) (RLIM)					
Input Inrush Current, ILIM connected to V_{IN}	I_{INRUSH}	—	—	350	mA
Input Inrush Current, ILIM connected via resistor R_{ILIM} to V_{IN}	I_{INRUSH}				
R_{ILIM} = 12.1 kΩ		130	180	250	
R_{ILIM} = 42.2 kΩ		70	110	165	
R_{ILIM} = 191 kΩ		30	65	100	
NORMAL OPERATION (VPWR, UVLO)					
Supply Voltage	V_{PWR}	—	—	60	V
Supply Current (10)	I_{PWR}	—	4.5	7.3	mA
Default Turn-On Voltage (UVLO = V_{IN})	$V_{UVLO(ON)}$	—	—	40	V
Default Turn-Off Voltage (UVLO = V_{IN})	$V_{UVLO(OFF)}$	30	—	—	V
UVLO Hysteresis when set internally	$V_{HYST(INT)}$	6.0	—	—	V
External UVLO Programming Range	$V_{UVLO(PR)}$	25	—	50	V
UVLO Reference Voltage	$V_{UVLO(REF)}$	1.96	2.0	2.04	V
UVLO Hysteresis when set externally	$V_{HYST(EXT)}$	—	15	—	%
UVLO Bias Current	$I_{UVLO(B)}$	—	—	1.0	μA
ISOLATION SWITCH (ILIM)					
On-Resistance (V_{PORT} = 48 V, I_{PORT} = 350 mA) (11)	$R_{DS(ON)}$	—	—	500	mΩ
Isolation Switch Current Limit in Normal Operation Mode	I_{LIM}	380	—	700	mA

Notes
10. GATE pin open, PWM controller running.
11. Measured across V_{IN} and V_{OUT}.

Table 3. Static Electrical Characteristics(continued)

Characteristics noted under conditions 30 V ≤ V_{PWR} ≤ 60 V, -40°C ≤ T_A ≤ 85°C, V_{IN} = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
PWM COMPARATOR (COMP)					
COMP Control Voltage Range	V_{COMP}	1.3	—	4.0	V
COMP Input Bias Current	$I_{COMP(B)}$	—	—	1.8	mA
HIGH VOLTAGE REGULATOR					
Regulator Output Voltage	VDD_{REG}	8.0	9.0	10	V
Regulator Turn-Off Voltage (12)	$V_{REG(OFF)}$		VDD_{Reg} +0.5	—	V
Regulator Current Limitation (13)	I_{REGLIM}	7.0	—	15	mA
Regulator Continuous Current	I_{REGDC}	—	—	5.0	mA
GATE DRIVER (UVLO)					
Gate Driver UVLO, Rising	$V_{GATE(R)}$	VDD-0.5	—	—	V
Gate Driver UVLO, Falling	$V_{GATE(F)}$	—	—	6.5	V
CURRENT LIMIT (CS)					
CS Threshold Voltage	V_{CS}	320	400	480	mV
CS Bias Current	$I_{CS(B)}$	—	—	30	μA
ERROR AMPLIFIER					
Reference Voltage	V_{REF}	1.164	1.2	1.236	V
OVERVOLTAGE SHUTDOWN					
OVLO Threshold, Rising	$V_{OV(R)}$	66	—	72	V
OVLO Threshold, Falling	$V_{OV(F)}$	63	—	69	V
OVLO Hysteresis	$V_{OV(HYS)}$	—	3.0	—	V
SOFT-START (SS)					
SS Output Voltage	V_{SS}	—	2.0	—	V
SS Source Current	$I_{SS(OUT)}$	3.25	5.0	6.75	μA
SS Sink Current	$I_{SS(IN)}$	—	2.0	2.25	mA
Shutdown Threshold Voltages	$V_{SS(R)}$ $V_{SS(F)}$	0.48 0.24	0.6 0.3	0.72 0.40	V
THERMAL SHUTDOWN					
Thermal Shutdown Temperature	$T_{SHUTDOWN}$	150	165	180	°C
Thermal Hysteresis	T_{HYS}	—	30	—	°C

Notes

12. An external voltage has to be applied.
13. Thermal limitations of the device might derate usable current range.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions 30 V ≤ V_{PWR} ≤ 60 V, -40°C ≤ T_A ≤ 85°C, V_{IN} = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
NORMAL OPERATION					
Turn-On Filter Time	$t_{FILT(ON)}$	—	200	—	µs
Turn-Off Filter Time	$t_{FILT(OFF)}$	—	200	—	µs
PWM COMPARATOR					
Slope Compensation Ramp as a Function of Switching Frequency					mV/µs
f_{PWM} = 100 kHz	m_{100}	—	10	—	
f_{PWM} = 250 kHz	m_{250}	—	25	—	
f_{PWM} = 400 kHz	m_{400}	—	40	—	
Duty Cycle Limit (14)	D_{MAX}	—	—	48	%
GATE DRIVER					
Rise Time (10% - 90%), C_{Load} = 2.0 nF, VDD_{REG} = 9.0 V	t_R	—	—	50	ns
Fall Time (90% - 10%), C_{Load} = 2.0 nF, VDD_{REG} = 9.0 V	t_F	—	—	30	ns
CURRENT LIMIT					
Blanking Time (14)	t_{BLANK}	40	50	60	ns
PWM OSCILLATOR					
Default Clock Frequency (FREQ connected to V_{IN})	f_{PWM}	175	225	325	kHz
Oscillator Frequency Adjusting Resistor Range	R_{FREQ}	121	—	499	kΩ
Oscillator Frequency Range, R_{FREQ} = 121 kΩ	f_{RANGE}	320	—	480	kHz
Oscillator Frequency Range, R_{FREQ} = 499 kΩ	f_{RANGE}	80	—	120	kHz
ERROR AMPLIFIER					
Gain Bandwidth (14)	GBW	1.0	—	—	MHz
DC Open Loop Gain	A_{VOL}	—	80	—	dB
$\overline{\text{RESET}}$ OUTPUT					
$\overline{\text{RESET}}$ Output Low Voltage ($I_{RESET, SINK}$ = 20 mA)	$V_{RESET,LOW}$	—	—	0.8	V
$\overline{\text{RESET}}$ Output Filter Time	$t_{\overline{RESET}}$	—	20	—	µs

Notes
14. Guaranteed by design. Not production tested.

TYPICAL SWITCHING WAVEFORMS

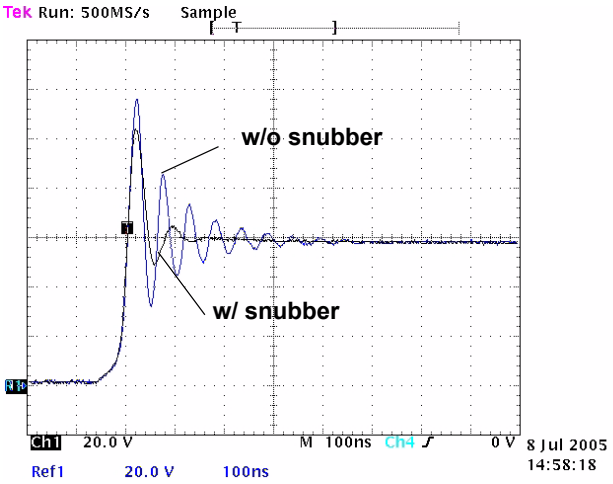


Figure 4. Drain Voltage of Switching MOSFET

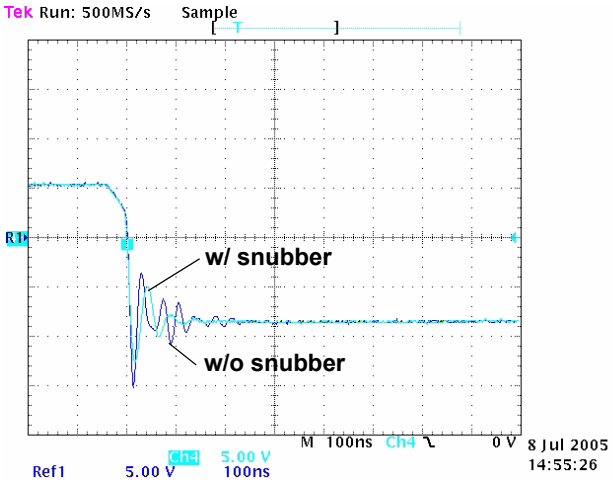


Figure 6. Secondary Voltage before Diode

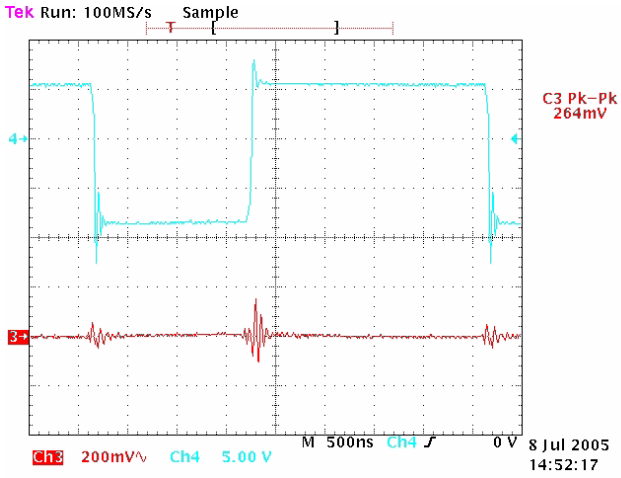


Figure 5. Secondary and Output Voltage

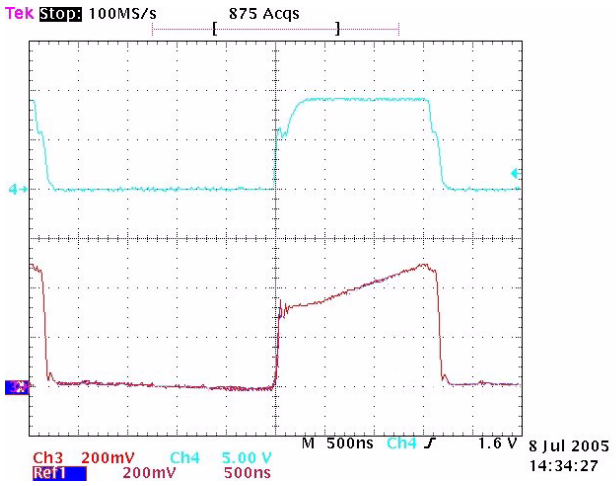
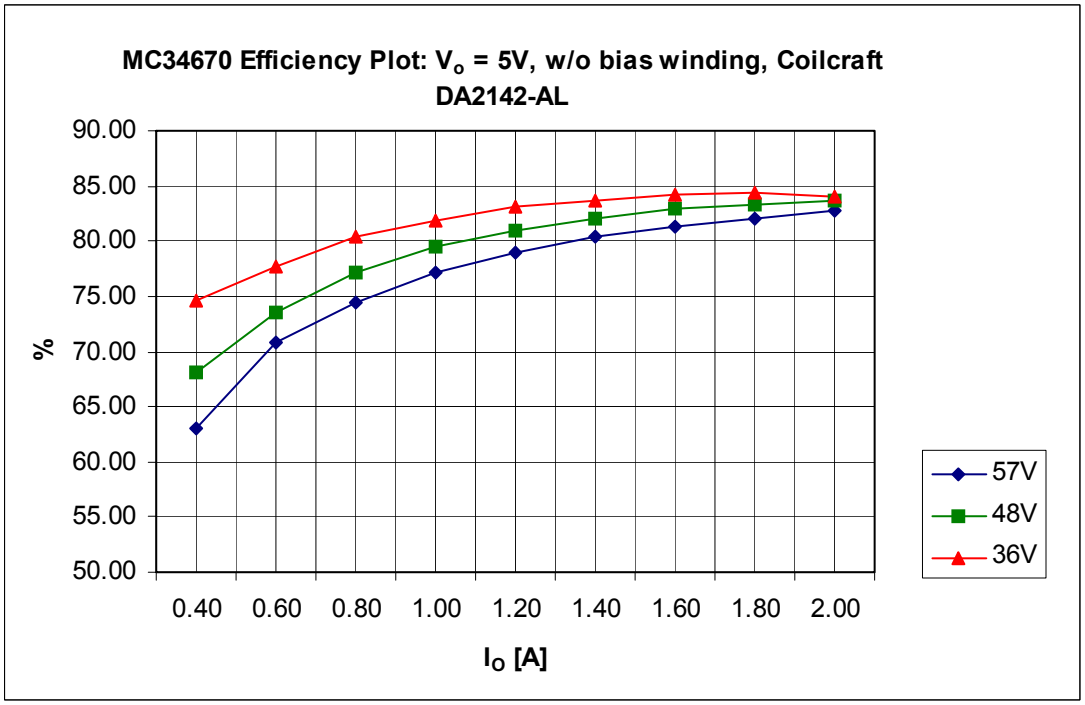


Figure 7. Gate Voltage and Voltage at CS pin

ELECTRICAL PERFORMANCE CURVES



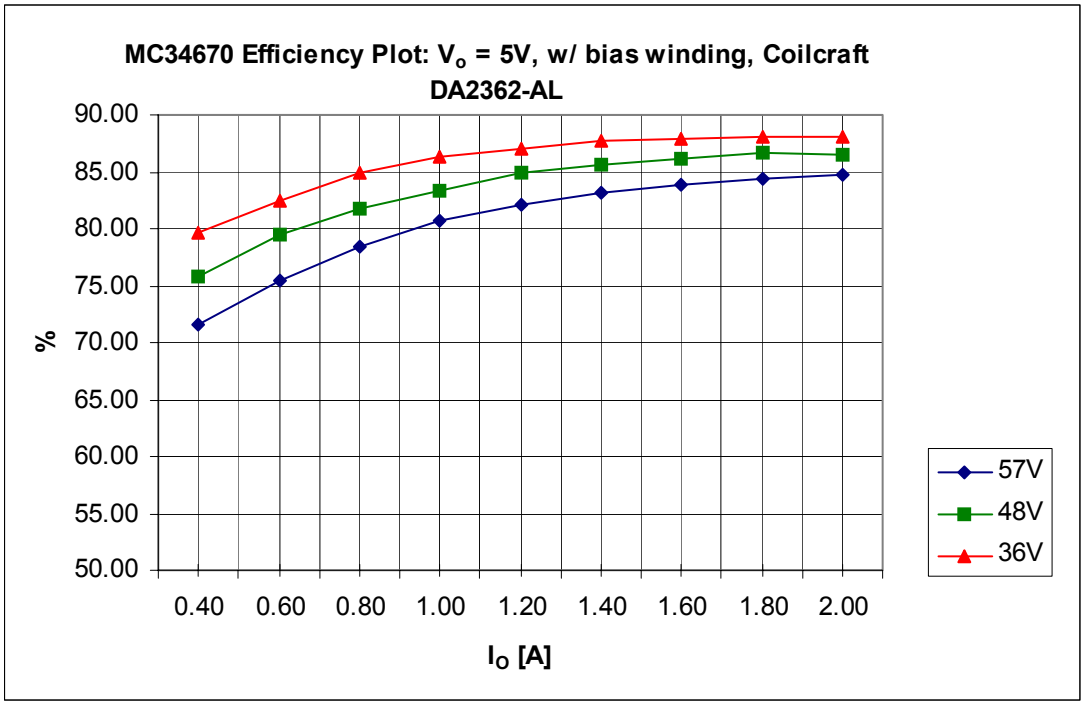


Figure 8. Efficiency Plot

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 34670 combines a Power Interface Port for IEEE 802.3af Powered Devices (PD) and a high performance current mode switching regulator. It allows a designer to build PDs with a minimum of external components by means of integrating the required IEEE 802.3af functions and all functions necessary to build a high efficiency DC/DC converter. Thus 34670 gives the system designer a device that drastically reduces cost and board space.

On the PD side the 34670 fully supports the IEEE802.3af standard and provides complete signature detection and power classification functions. It controls inrush current limiting and incorporates an adjustable undervoltage lockout. The 34670 includes thermal protection circuitry to protect the device in case of high power dissipation.

The 34670 also offers an input overvoltage detection to protect the external switching MOSFET by disabling the gate driver in case of input line overvoltage.

The switching regulator provides excellent line and load regulation. It drives an external power MOSFET with sense resistor. The switching frequency is adjustable between 100 kHz and 400 kHz. The output voltage feedback information can be accomplished by an optocoupler, if isolation is required.

An internal logic control block manages the sequencing of signature detection, classification and proper turn on and turn off of the DC/DC converter.

FUNCTIONAL PIN DESCRIPTION

POSITIVE SUPPLY VOLTAGE INPUT (VPWR)

This is the most positive power supply input. The load connects between this pin and the V_{OUT} pin.

CLASSIFICATION RESISTOR (RCLA)

Connect a resistor between RCLA and V_{IN} to select the class of the PD.

UNDERVOLTAGE LOOKOUT (UVLO)

Used to adjust the undervoltage lookout threshold voltage, connected to V_{IN} to use the default threshold voltage.

TEST PINS (TEST1, TEST2)

Connect to V_{IN} in application mode.

FREQUENCY ADJUSTMENT (FREQ)

Adjusts the internal oscillator frequency by connecting a resistor between FREQ and V_{IN}.

INRUSH CURRENT LIMIT (ILIM)

Used to adjust the inrush current limit of the isolation switch, add a resistor between ILIM and V_{IN}.

NEGATIVE SUPPLY VOLTAGE (VIN)

This is the most negative power supply input.

OUTPUT VOLTAGE (VOUT)

This pin is the drain of the internal Power MOSFET (high current path and low current path).

RESET OUTPUT (RESET)

This is an active-low RESET output signal. This pin is referenced to V_{OUT}.

SOFT START INPUT (SS)

Connect an external capacitor to SS. The internal current source charges the capacitor and generates a soft-start ramp.

COMPENSATION PIN (COMP)

COMP is the output of the error amplifier and is available for feedback compensation. COMP is pulled-up by an internal 5.0 kΩ resistor to 5.0 V.

FEEDBACK INPUT (FB)

This is the inverting input of the error amplifier. In non-isolated applications it's connected to the secondary output through a resistor divider.

CURRENT SENSE (CS)

The current sense pin CS senses a voltage that is proportional to the current through the sense resistor.

GATE DRIVER OUTPUT (GATE)

GATE drives the gate of the external power MOSFET. GATE sources and sinks up to 1.0 A.

VDD OUTPUT (VDD)

V_{DD} mainly supplies the gate of the external power MOSFET. Connect a capacitor from V_{DD} to V_{OUT}.

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

POWER DEVICES (PD) INTERFACE

The PD interface of the 34670 has been designed to comply with the requirements of the IEEE standard 802.3af. The device operates in three different modes, depending on the input voltage.

PD OPERATING MODES

The IEEE 802.3af standard defines three operating modes in general. These modes are summarized in Table 5.

Table 5. PD Operating Modes

Operating Mode	Voltage at PD Input Connector
Signature Resistor Detection	2.7 V - 10.1 V
Classification	14.5 V - 20.5 V
Normal Operation Mode	37 V - 57 V

SIGNATURE RESISTOR DETECTION

A PD shall present a valid detection signature at the PD input connector to get properly detected as a power over LAN enabled pin. Valid and non-valid detection signature regions are separated by guard bands. See Figure 9 for valid and non-valid signature regions.

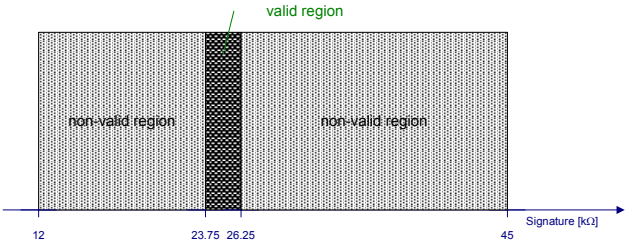


Figure 9. Signature Resistance Guard Bands

The effective resistance across the input pins is calculated by two subsequent voltage-current measurements made during the detection process by the PSE.

VALID PD DETECTION SIGNATURE CHARACTERISTICS

During signature detection phase the Power Sourcing Equipment (PSE) applies a voltage in the range 2.7 V - 10.1 V on the PI connector and looks for the 25 kΩ signature resistor. Since the PD circuitry includes bridge rectifiers, the PD has to compensate for the voltage drop across the diodes and the diodes serial resistance. The effective signature resistance dR is obtained by the V-I-Slope measurement of the PSE (Figure 10).

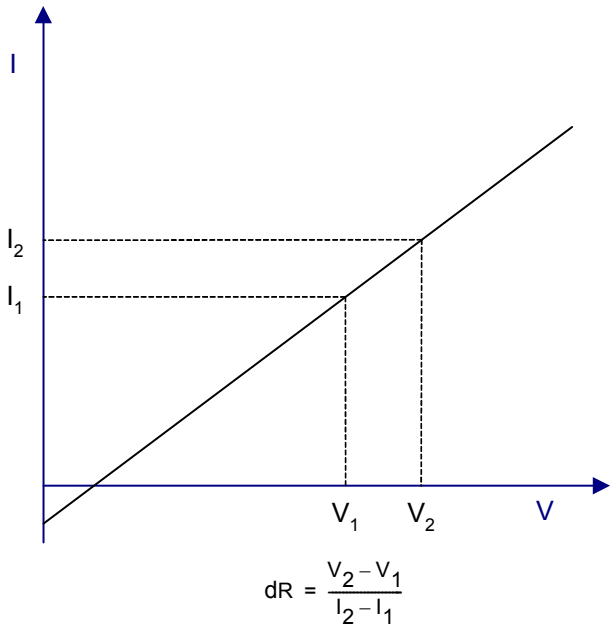


Figure 10. dR Measurement

It can be seen in Figure 11, that a signature resistor of 25 kΩ as defined in IEEE 802.3af and two diodes in series would lead to an effective resistance out of the valid region specified in Figure 9. At low voltages the effective resistance is above the maximum allowed value of 26.25 kΩ, as illustrated in Figure 11. Therefore one has to adjust the signature resistor RSIG (R_1 and R_2, see **UVLO Adjustment on page 13**) to a value below 25 kΩ to stay within the valid region.

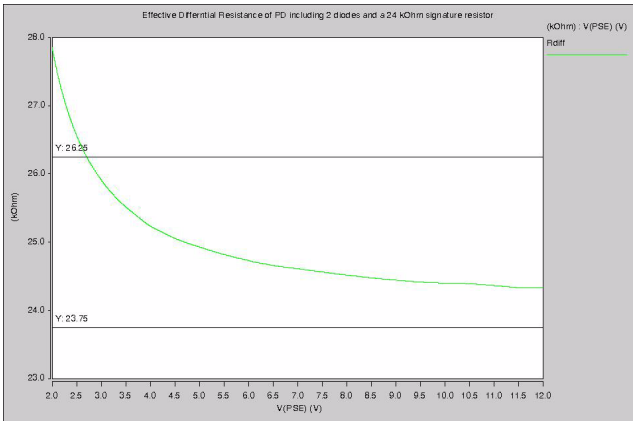


Figure 11. dR at Low Input Voltages

CLASSIFICATION

A PD may optionally be classified by the PSE. The intent of classification is to provide a method for more efficient power allocation through the PSE. The PD classification allows the PSE to identify four different (power) classes depending on the required power that the PD will draw during normal operation. The classes and the corresponding maximum power drawn by the PD is shown in Table 6.

Table 6. PD Classes

Class	Usage	Maximum Power [W]
0	Default	0.44 - 12.95
1	Optional	0.44 - 3.84
2	Optional	3.84 - 6.49
3	Optional	6.49 - 12.95
4	Reserved	—

PD CLASSES

During classification probing by the PSE, the PD applies the appropriate load current onto the line. The PSE measures the load current and can determine the classification as described in Table 7.

Table 7. PD Class vs. Classification Current

Class	Classification Current [mA]		Condition
	Min	Max	
0	0	4	14.5 - 20.5 Volts measured at PD input connector
1	9	12	
2	17	20	
3	26	30	
4	36	44	

CLASSIFICATION SIGNATURE LOAD CURRENT

The implementation for the classification circuitry is shown in Figure 12.

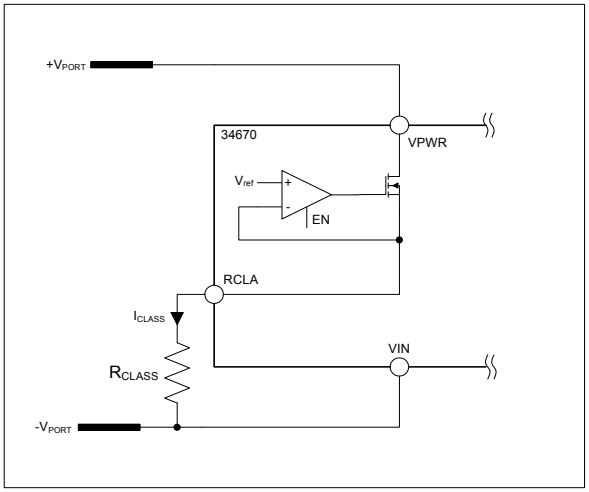


Figure 12. Classification Circuitry

A constant voltage is applied at pin RCLA and depending on the resistor R_{CLASS}, a current from $+V_{PORT}$ to $-V_{PORT}$ is flowing with the following relation:

$$I_{CLASS} = \frac{V_{RCLA}}{R_{CLASS}}$$

I_{CLASS} is the classification current that is measured by the PSE. The values for the R_{CLASS} resistor corresponding to the appropriate class are listed in Table 8.

Table 8. PD Class vs. Classification Resistor R_{CLASS}

Class	Classification Current [mA]	R_{CLASS} [Ω]
0	2.0	4.42k
1	10.5	475
2	18.5	261
3	28	169
4	40	113

UVLO ADJUSTMENT

The 34670 has default UVLO settings that corresponds to the IEEE 802.3af standard. Nevertheless the user can adjust the UVLO by an external resistor divider as sketched in Figure 13. Since the UVLO resistor divider replaces the

signature resistor, the total resistance of R_1+R_2 must equal 25 kΩ.

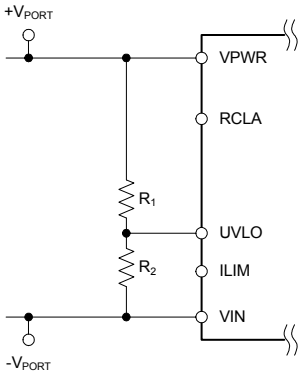


Figure 13. UVLO Adjustment by External Resistor Divider

To use the default settings for UVLO, the pin UVLO must be connected to VIN. In this case, a valid signature resistor has to be placed between -V_{PORT} and +V_{PORT}. This configuration can be seen in Figure 14.

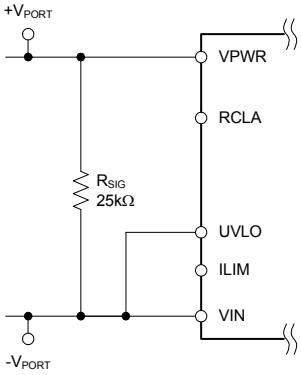


Figure 14. Default UVLO Settings

To calculate the values for R_1 and R_2 the following equations should be used:

$$R_1 + R_2 = R_{SIG}$$

$$R_2 = \frac{V_{UVLO(REF)}}{V_{UVLO(ON)}} \cdot R_{SIG}$$

where $V_{UVLO(ON)}$ is the desired turn-on voltage threshold and $V_{UVLO(ref)}$ the UVLO reference voltage.

$$R_1 = R_{SIG} - R_2$$

$$V_{UVLO(OFF)} = V_{UVLO(ON)} \cdot 0.85$$

The typical turn-off voltage $V_{UVLO(OFF)}$ is 85% of the turn on voltage $V_{UVLO(ON)}$.

INRUSH CURRENT LIMITATION

The 34670 has been designed to interface also with legacy PoE-PSEs which do not meet the inrush current requirement of the IEEE 802.3af specification. By setting the initial inrush current limit to a low level, a PD using the 34670 minimizes the current drawn from the PSE during start-up. The maximum inrush current level can be set by connecting a resistor from ILIM to V_{IN} as illustrated in Figure 15.

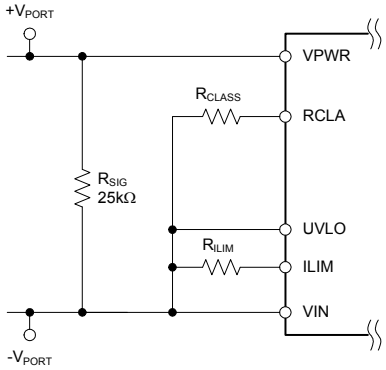


Figure 15. Inrush Current Limitation by External Resistor R_{ILIM}

The following table shows the selectable current limits and the corresponding resistor value that has to be connected between pins ILIM and VIN:

Table 9. Inrush Current Limit vs. R_{ILIM}

Inrush Current Limit [mA]	R_{ILIM} Value [kΩ]
180	12.1
110	42.2
65	191

After powering up, the 34670 switches to the high level current limit, thereby allowing the PD to consume up to 12.95 W if a 802.3af PSE is present.

PULSE WITH MODULATOR CONTROLLER

CURRENT-MODE CONTROL OPERATION

The 34670 offers current-mode control operation with leading-edge blanking. The current-limit comparator monitors the CS pin at all times and provides cycle-by-cycle current limit.

The CS signal contains a leading-edge spike that is the result of the MOSFET gate charge current, capacitive and diode reverse recovery current of the power circuit. The leading-edge blanking of the CS signal prevents the PWM comparator from premature termination of the on cycle.

The 34670 limits the duty cycle to 50%. This is advantageous for applications which are not allowed to exceed an on-time of 50 % of the switching period T_S. Beside the duty-cycle limit, slope compensation is provided to stabilize the inner current loop and avoid oscillations for

converters running in continuos conduction mode (CCM). The value of the slope compensation depends on the switching frequency. See Table 10.

Table 10. Slope Compensation Values

Switching Frequency [kHz]	Slope Compensation [mV/μs]
100	10
250	25
400	50

ISOLATED OPTOCOUPLER FEEDBACK

Isolated voltage feedback can be accomplished by using an optocoupler and a shunt regulator (see Figure 19). The output voltage accuracy is a function of the accuracy of the shunt regulator and feedback resistor divider tolerance, therefore the feedback resistors should have an appropriate accuracy.

Since the error amplifier function is implemented on the secondary side by the optocoupler and a 3-pin adjustable shunt regulator, the internal error amplifier of the 34670 is not used. The FB pin is connected to V_{OUT}, thus disabling the internal open-drain error amplifier.

The bias voltage for the optocoupler is accomplished through the internal 5.0 kΩ pull-up resistor between COMP and an internal 5.0 V reference.

When a TL431 or TLV431 shunt regulator is used for output voltage regulation, the output voltage is set by the ratio of resistors R_1 and R_2, see Figure 16 for details. The output voltage is given by the following equation:

$$V_O = V_{REF} \cdot \left(1 + \frac{R_1}{R_2}\right)$$

where V_{REF} = 1.24 V for the TLV431 (V_{REF} = 2.5 V for the TL431).

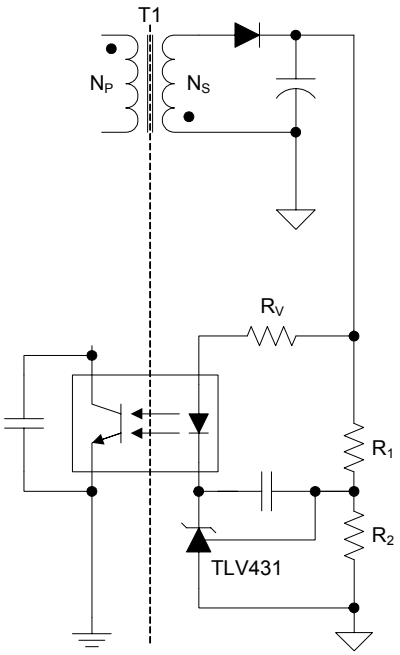


Figure 16. Isolated Optocoupler Feedback

ISOLATED PRIMARY CONTROL FEEDBACK

Another option to accomplish isolated feedback is the use of a tertiary winding (see Figure 21). The advantage of this solution without optocoupler and shunt regulator is clearly the cost effectiveness. Nevertheless the line and load regulation is worse than with optocoupler feedback.

When isolated primary feedback is used, the loop compensation components are connected between pins COMP and FB.

INTERNAL REGULATORS

The internal high voltage regulator of the 34670 regulates from the input voltage across VPWR and VIN down to the V_{DD} voltage. During start-up the high voltage regulator provides the necessary voltage for the internal gate driver to commence switching. If the external MOSFET gate drive pulls less than 3.0 mA under all circumstances, an auxiliary transformer winding that usually provides the bias voltage for the chip and the gate driver is not required.

In cases where the external MOSFET gate drive pulls more than 5.0 mA, an auxiliary winding is needed to reduce the power dissipation in the internal high voltage LDO. See Figure 18 for an application drawing. It is recommended to add a 0.1 μF ceramic capacitor in parallel with the existing load capacitor. This reduces noise at the V_{DD} pin caused by the auxiliary winding.

The high voltage regulator is disabled when the V_{DD} pin is forced by an external voltage above the V_{DD} regulation point.

This reduces power dissipation in the device and improves overall efficiency.

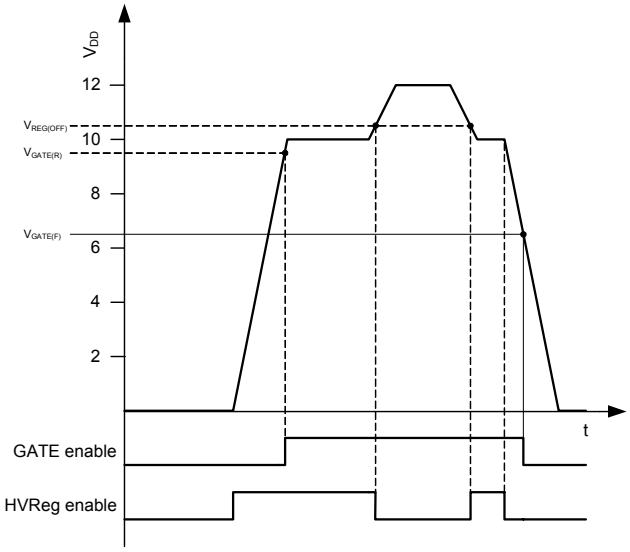


Figure 17. V_{DD} and MOSFET Driver Output Behavior

A load capacitor connected to V_{DD} ensures a proper filtering of the V_{DD} voltage. The minimum capacitance value for this load capacitor should be at least 10 μF. An electrolytic type capacitor is sufficient.

Please refer to application note **A/N3279** for further information about the size of the capacitor.

If V_{DD} falls below the UVLO threshold, the voltage regulator is disabled and the MOSFET driver output (GATE) is held low.

PWM CONTROLLER UVLO, SOFT-START, AND SHUTDOWN FUNCTION

The soft-start function provided by the 34670 allows the output voltage to ramp up in a controlled way, thus eliminating output voltage overshoot.

While the PWM controller is in undervoltage lockout, the capacitor C_{SS} connected to the SS pin is fully discharged. After coming out of undervoltage lockout, an internal current source starts charging the capacitor C_{SS} to initiate soft-start. When V_{SS} has reached 0.6 V, the gate driver is enabled and PWM operation begins. The duty cycle during soft-start is primarily controlled by the internal sawtooth voltage and the voltage at the SS pin. If the voltage at the SS pin is above 2.6 V, the regular PWM control through pins CS, COMP, and FB takes over and soft-start is finished.

The following equation calculates the total soft-start time:

$$t_{SS}[ms] = 0.4 \cdot C_{SS}[nF]$$

OVERVOLTAGE SHUTDOWN

The 34670 includes an overvoltage protection (OVP) feature that turns off the external MOSFET when the input voltage exceeds the overvoltage threshold.

When the overvoltage protection is triggered ($V_{PWR} > V_{OV(R)}$), the gate driver is immediately disabled. At the same time, the slow discharge of C_{SS} is initiated. While the soft-start capacitor is discharging, the gate driver remains disabled. Once V_{SS} = 0.3 V and the overvoltage ($V_{PWR} < V_{OV(F)}$) condition disappears, operation resumes through a regular soft-start.

CURRENT-SENSE COMPARATOR

The current-sense (CS) comparators and its associated circuitry limits the peak current through the MOSFET. Current is sensed at CS pin as a voltage across the sense resistor R_{CS} between the source of the MOSFET and V_{OUT}.

The CS input has two voltage trip levels, a 600mV high limit and a 400 mV low limit. When the voltage on CS produced by a current through the current sense resistor exceeds the high limit threshold, the current ON-cycle is immediately terminated and the GATE output is pulled low.

If the low limit threshold is exceeded for longer than 50 ns (typical blanking time), the current ON-cycle is also terminated. The blanking time ensures a false termination of the switching cycle caused by the leading-edge spike on the sense waveform.

The current-sense resistor R_{CS} is selected according to the following equation:

$$R_{CS} = \frac{400mV}{I_{LIM(primary)}}$$

where $I_{LIM(primary)}$ is the maximum peak primary-side current.

In case of an overcurrent in the external MOSFET the current switching cycle is terminated and GATE is pulled low. The soft-start capacitor C_{SS} is discharged and after removal of the faulty condition the PWM is re-started through a regular soft start.

PWM OSCILLATOR

A default 250 kHz oscillator sets the switching frequency of the PWM controller. The frequency of the oscillator can be adjusted between 100 kHz and 400 kHz by an optional external resistor R_{FREQ} connected from the FREQ pin of the integrated circuit to V_{IN}.

The appropriate switching frequency f_{PWM} can be calculated as shown below:

$$f_{PWM}[kHz] = \frac{47920}{R_{FREQ}[k\Omega]} + 4$$

where f_{PWM} is the PWM switching frequency and R_{FREQ} is the frequency adjusting resistor.

To use the default frequency of 250 kHz the FREQ pin can be connected to V_{IN} or can be left open.

$\overline{\text{RESET}}$ OUTPUT

The $\overline{\text{RESET}}$ pin is an open drain output. The reset control circuit supervises the FB voltage and recognizes if the output

voltage is out of regulation. In this case the $\overline{\text{RESET}}$ pin is pulled low.

The $\overline{\text{RESET}}$ output can only be used in non-isolated applications.

There is a 20 μs delay filter preventing erroneous $\overline{\text{RESET}}$ output pulses. During soft-start, $\overline{\text{RESET}}$ is held low. $\overline{\text{RESET}}$ is released when the PWM controller is in regulation.

N-CHANNEL MOSFET GATE DRIVER

GATE drives an N-channel MOSFET. GATE sources and sinks large transient currents up to 1.0 A to charge and discharge the MOSFET gate. The GATE output is supplied by the internal generated V_{DD} voltage, which is internally set to approximately 9.0 V.

For Power-over-Ethernet applications, the used MOSFET must be able to withstand a DC level of ~60 V plus the reflected voltage at the primary side of the transformer. This requires a MOSFET rated at 150 V or 200 V.

TYPICAL APPLICATIONS

Please refer to application note AN3279 for further information of PD design and layout recommendations.

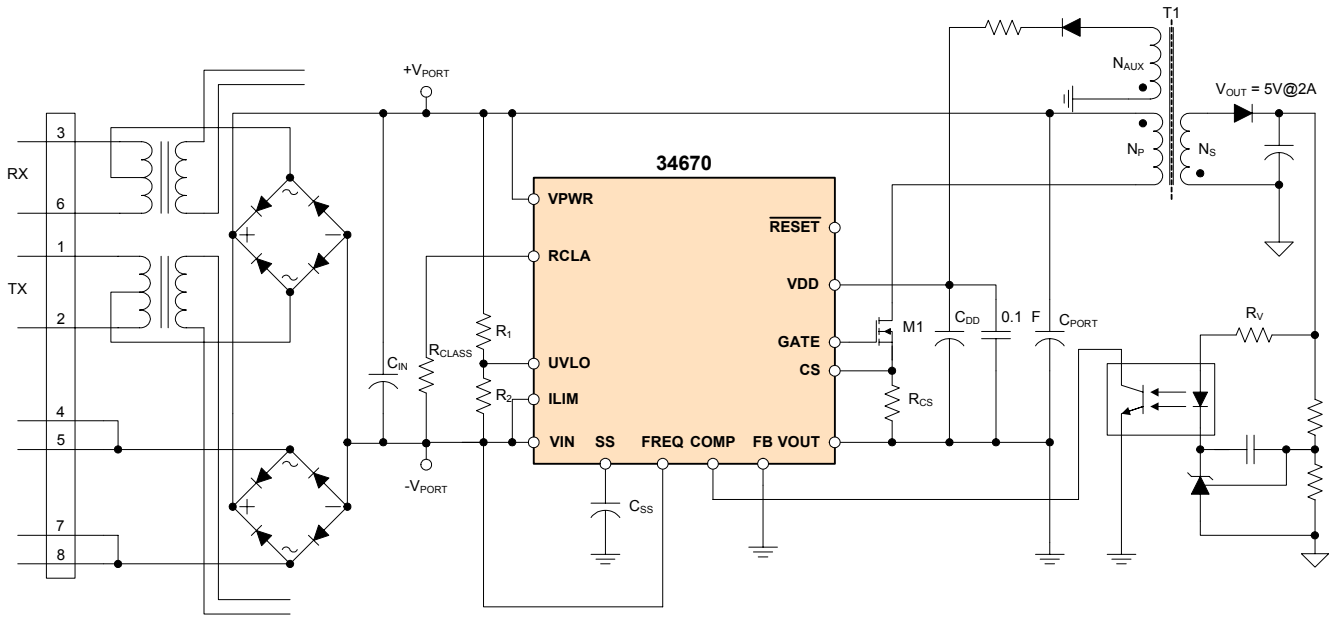


Figure 18. Isolated Flyback Converter with Bias Winding

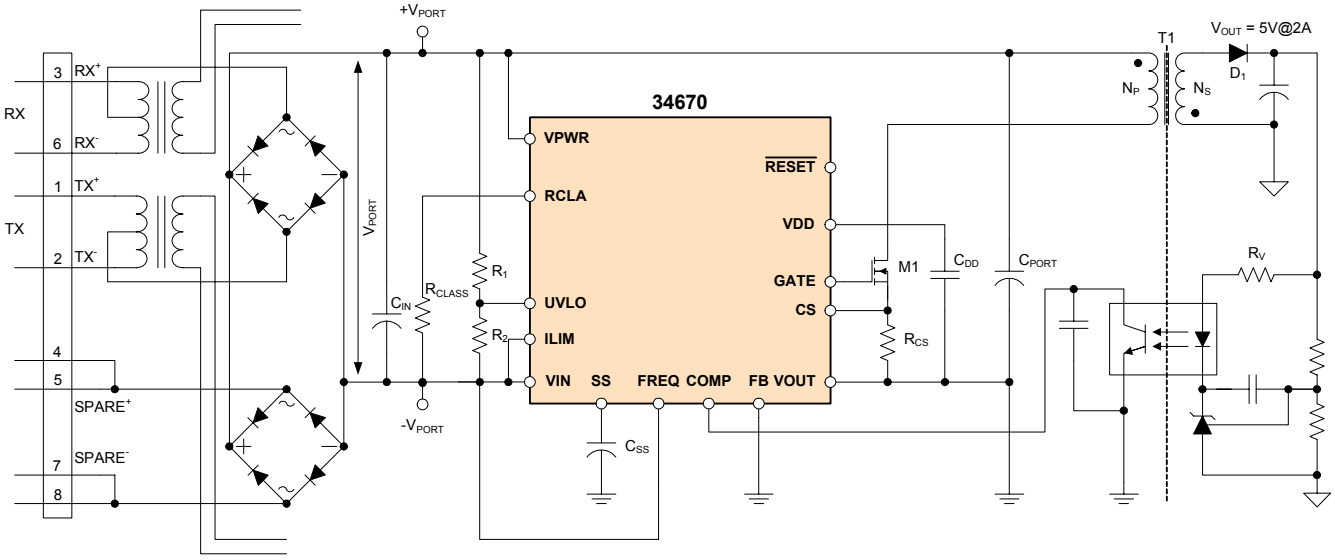


Figure 19. Isolated Flyback Converter without Bias Winding

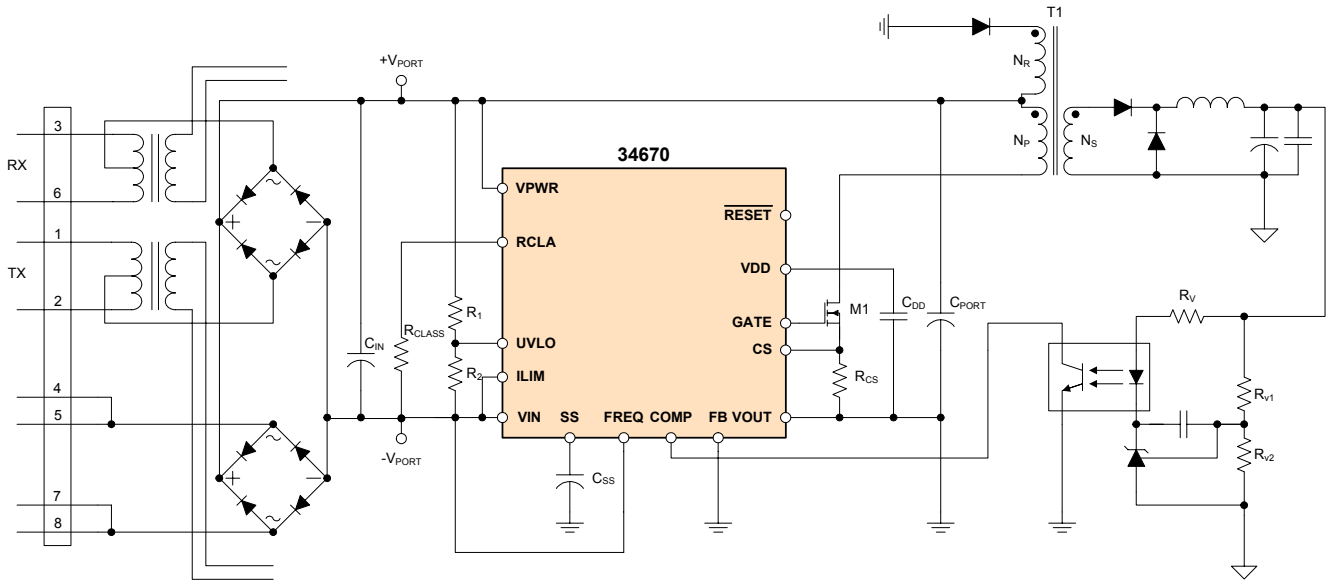


Figure 20. Isolated Forward Converter

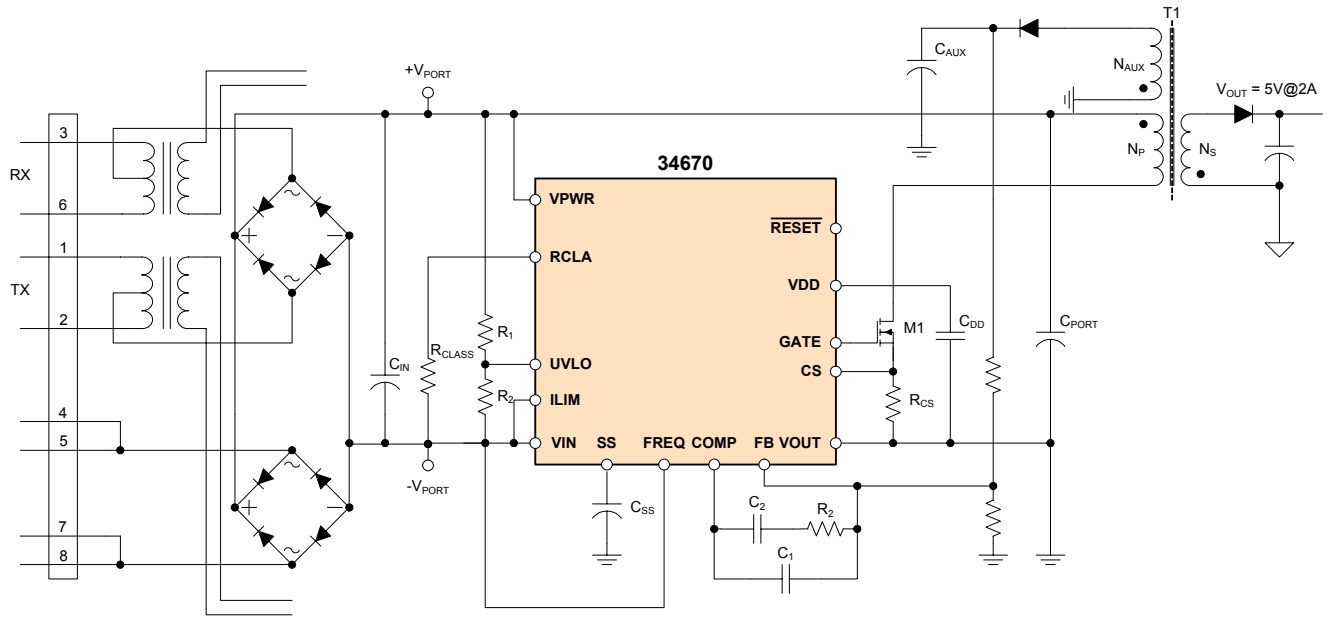


Figure 21. Isolated Flyback with Primary Control

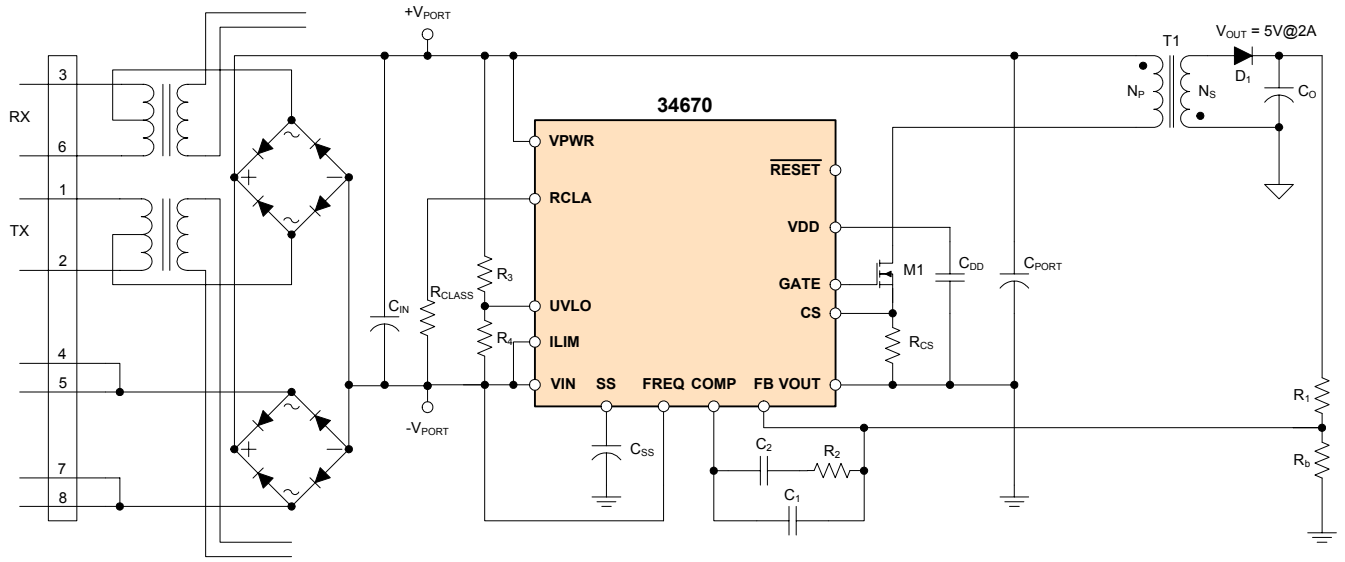


Figure 22. Non-Isolated Flyback Converter

REFERENCE DOCUMENTS

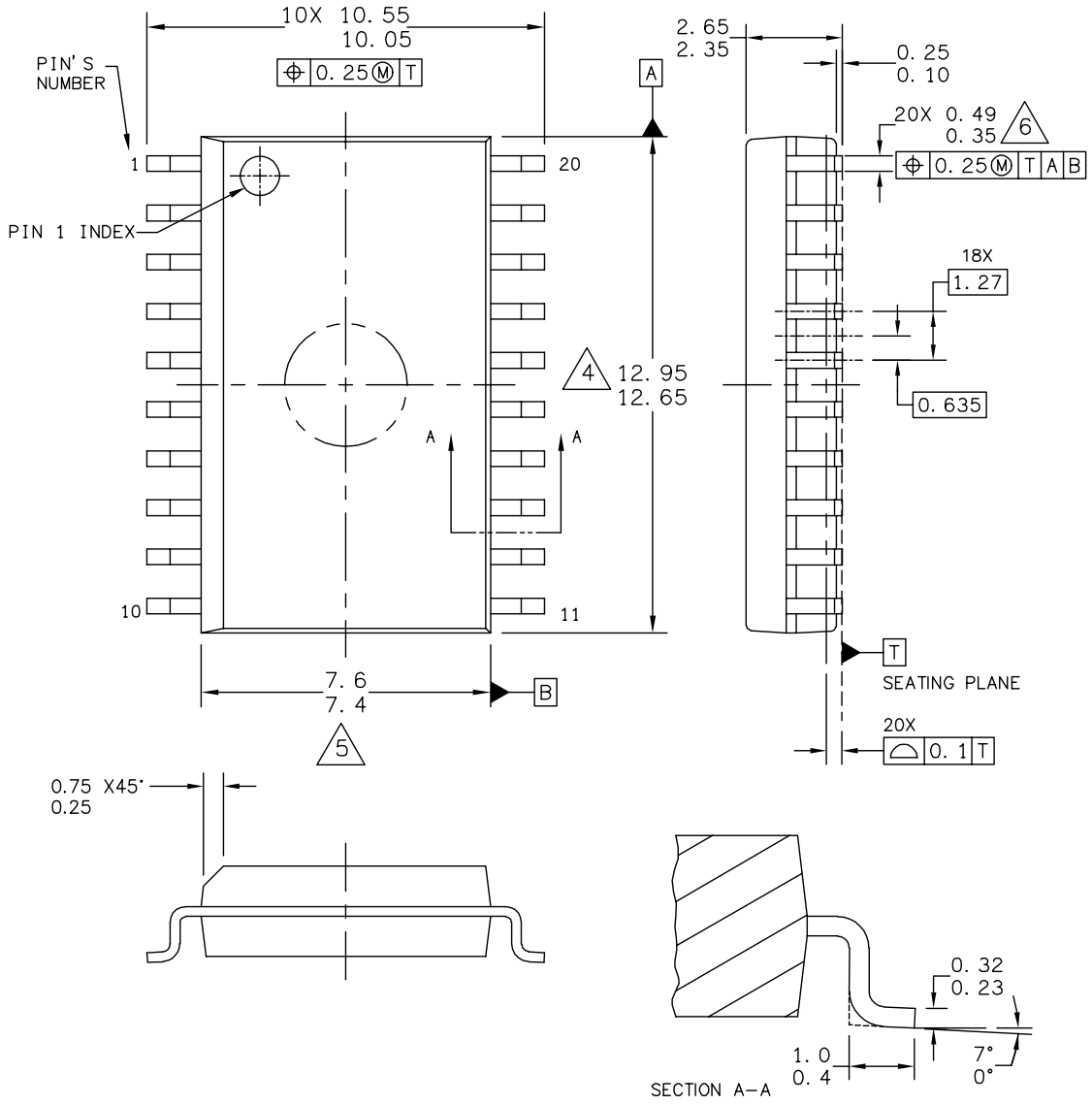
Table 11. Reference Documents

Title	LIterature Order Number	Publication Date
IEEE Std 802.3af™-2003	IEEE Std 802.3af™-2003	18 June 2003
MC34670 Usage and Configuration	AN3279	

PACKAGING

PACKAGE DIMENSIONS

For the most current package revision, visit **www.freescale.com** and perform a keyword search using the “98A” listed below.



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	CASE NUMBER: 751D-07	23 MAR 2005
	STANDARD: JEDEC MS-013AC	

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PLASTIC PACKAGE
98ASB42343B
ISSUE J

34670

REVISION HISTORY

Revision	Date	Description of Changes
1.0	8/2006	• Initial release
2.0	9/2006	• Change to UVLO Hysteresis when set internally on page 6, Regulator Current Limitation [13] on page 7, OVLO Threshold, Rising on page 7, OVLO Threshold, Falling on page 7, Shutdown Threshold Voltages on page 7, and Default Clock Frequency (FREQ connected to VIN) on page 8 • Changed Data Sheet category to “Advanced Information*”
3.0	12/2006	• Typ and Max change to RCLA Reference Voltage (13.5 V ≤ V_{PORT} ≤ 20 V) on page 6 • Deleted Oscillator Frequency Adjusting Resistor Range in Static Electrical Characteristics • Split Oscillator Frequent Range into two parameters, Oscillator Frequency Range, R_{FREQ} = 121 kΩ on page 8 and Oscillator Frequency Range, R_{FREQ} = 499 kΩ on page 8 • Added note to Duty Cycle Limit [14] on page 8, Blanking Time [14] on page 8, and Gain Bandwidth [14] on page 8 • Changed nomenclature for Peak Package Reflow Temperature During Reflow [5], [6] on page 5 • Changed name and value for Thermal Shutdown Recovery Temperature on page 5

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