Abridged Version

SSI 73M2918/2918A

Plug and Play Microcontroller and UART

Advance Information

January 1995

DESCRIPTION

The SSI 73M2918 is a combination of the SSI 73M2910 modem microcontroller, a virtual 550 UART, and built-in hardware to support the Plug and Play ISA standard, implemented in Silicon Systems' advanced CMOS process. The 8-bit processor has the same attributes as the 8052 including instruction cycle time, UART, timers, interrupts, 256 bytes of on-chip RAM and programmable I/O. The virtual 550 UART utilizes proprietary technology, which results in a complete emulation of the industry standard 550 UART, and adds significant features. The 550 UART emulator provides familiar 550 functions to the PC and replaces the serial link between the PC and the dedicated processor with a parallel data interface. The architecture results in a high-performance system solution that is optimized for low power applications.

The 73M2918 also includes the user friendly HDLC packetizer that is available in the 73M2910. It has a serial I/O, hardware support for 16- and 32-bit CRC, zero insert/delete control, a dedicated interrupt and a clear channel mode for by-passing the packetizer.

(continued)

FEATURES

- 8052-compatible instruction set
- Virtual 550 UART
- Dedicated Plug and Play ISA bus hardware
- 33 MHz 73M2918, 44 MHz 73M2918A operation
- Operates at 3.3V and 5V
- HDLC Support logic (Packetizer, 16 and 32 CRC, zero ID)
- 24 pins for user programmable I/O ports
- 8 pins programmable chip select logic for memory mapped peripheral eliminating glue logic
- 3 external interrupt sources (programmable polarity)
- 16 dedicated latched address pins
- Multiplexed data/address bus
- Instruction cycle time identical to 8052
- Buffered oscillator (or OSC/2, OSC/1.5) output pin

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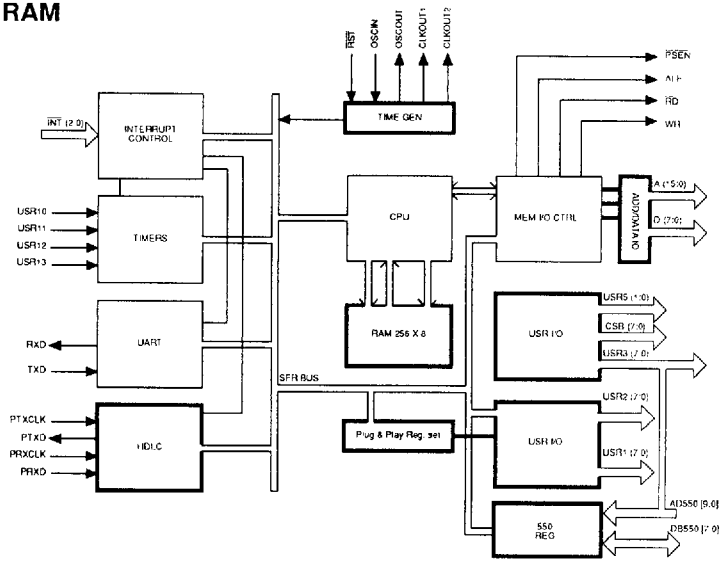
BLOCK DIAGRAM



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DESCRIPTION (continued)

Other features include additional user programmable I/O with programmable bank select and chip select logic, designed to eliminate board level glue logic. It also includes two general purpose input pins with programmable wakeup capability.

For devices that require non-multiplexed address and data buses, eight latched outputs for the low byte of the address are available.

The 73M2918 has two extra interrupt sources, an external interrupt and an HDLC interrupt. The HDLC interrupt has two registers associated with it: the HDLC interrupt register which is used to determine the source of the interrupt, and the HDLC interrupt enable register that enables the source of the interrupt.

The state of the external interrupts can be read through a register allowing the interrupt pins to be used as inputs. The interrupt pins INT0 and INT1 can be either negative edge, positive edge or level triggered. INT2 pin is always edge triggered.

Two buffered clock outputs have been added to support peripheral functions such as UARTs, modems and other clocked devices. The main internal processor clock frequency can be divided by 2 for power conservation in functional modes that only require half the clock speed.

Additional internal special function registers are used for firmware control over the HDLC Packetizer, the clocks and the programmable I/O ports.

The processor's timing has been altered slightly to allow more address setup time for slower peripheral program ROM and memory mapped peripherals. This can offer the system designers an advantage when using higher oscillator frequencies.

For low power applications the 73M2918 operates from 3 to 5 volts at 22 MHz and supports two power conservation modes: Idle and power-down. In the power-down state the total current consumption is less than 1 μA at room temperature.

This device is offered in a small form factor 100-lead TQFP package and a 100-lead QFP package.

DEVELOPER'S NOTE

The SSI 73M2918/2918A is also available in a 100-pin PGA package for system developers. The PGA package is more convenient and reliable for development emulation systems than the other package styles. Emulation systems for the SSI 73M2918/2918A are available through Signum Systems,171 E. Thousand Oaks Blvd., # 202, Thousand Oaks, CA 91360, (805) 371-4608.

8052 REFERENCE

This document will describe the features unique to the SSI 73M2918/2918A. Please refer to an 8052 Programmer's Guide, Architectural Overview and Hardware Description for details on the SSI 73M2918/2918A core processor instruction set, timers, UART, interrupt control, and memory structure.

FEATURES (continued)

- 1.8432 MHz UART clock available if crystal frequencies 11.0592 MHz, 22.1184 MHz, 18.432 MHz, or 13.824 MHz are used
- Bank select circuitry to support up to 128K of external program memory
- Available in a 100-Lead QFP package

For a complete SSI 73M2918/2918A data sheet contact your local Silicon Systems sales office. See listing of sales offices in Section 11.

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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