2K X 8 High Speed CMOS Electrically Erasable PROM

FEATURES

- 2048 x 8 Bit CMOS E^2PROM
- High Speed Read Access
  - — 55ns, 60ns, 70ns, 85ns
- Bipolar PROM Socket Compatibility
- Electrically Reprogrammable
  - — Program Voltage: 10.8 - 20.5V
- Fast Byte Write: 5ms
- TTL Compatible Inputs and Outputs
- Static — No Clocks Required
- Low Current Requirements
  - — 90mA active (max.)
  - — 45mA standby (max.)
  - — 110mA programming (max.)
- 10 Year Data Retention
- 100% Factory Tested Programmability
- PROM Programmer Support Available

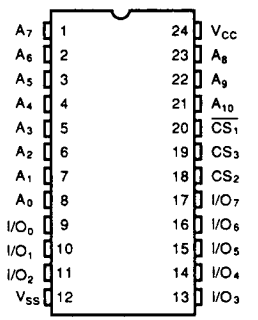
OVERVIEW

The XL46C15 is a 2K x 8 bit CMOS electrically erasable programmable read only memory (E^2PROM) offering unprecedented data access speed. The device is packaged to conform to the JEDEC-approved 24-pin configuration for 2K x 8 bit bipolar PROMs.

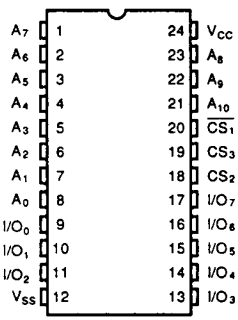
Through the application of revolutionary design techniques, this versatile low power device is able to provide data access times competing with those of bipolar PROMs. Complete PROM compatibility is provided in both read and standby modes allowing this E^2PROM to replace bipolar PROMs in existing sockets. The key user limitations of bipolar PROM technology, such as one-time programmability and high power requirements, are overcome by the XL46C15. In addition to being an attractive PROM replacement in existing systems, the XL46C15 also opens up a whole new domain of design possibilities.

PIN CONFIGURATIONS

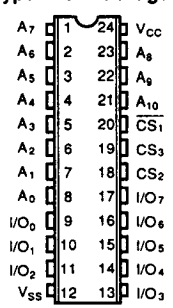
24 Pin PDIP
Type "P" Package



24 Pin CERDIP
Type "C" Package



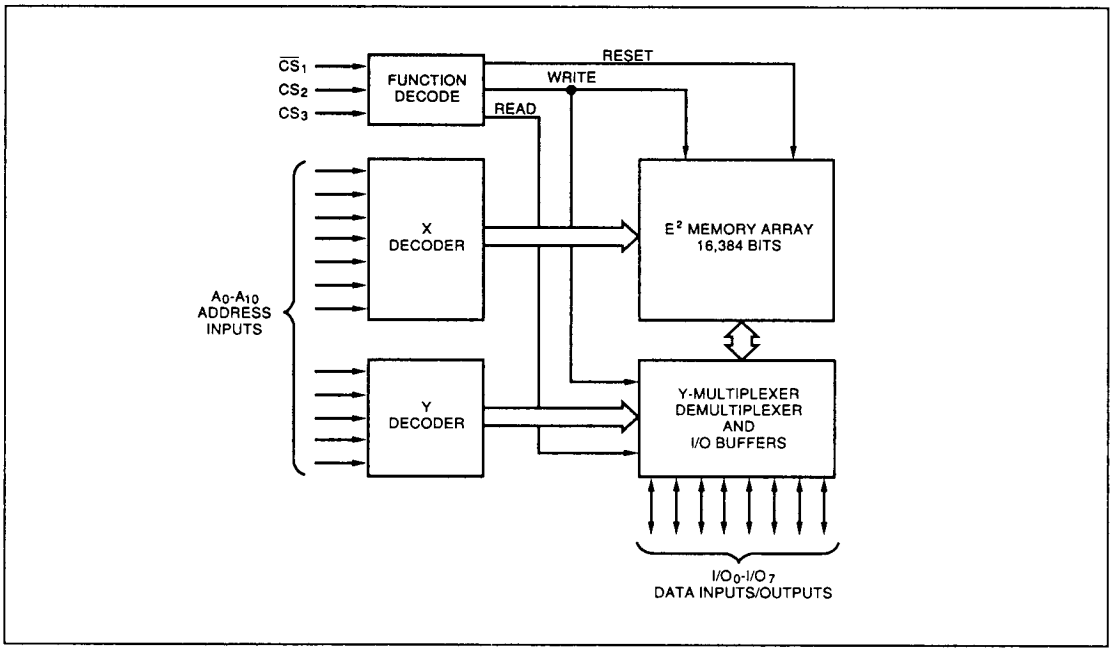
24 Pin Skinny DIP
Type "P3" Package



PIN NAMES

A_0-A_{10}	Address Inputs
I/O_0-I/O_7	Data Inputs/Outputs
$\overline{CS}_1$, CS_2, CS_3	Chip Select Inputs
V_{CC}	+5V Supply
V_{SS}	Ground

BLOCK DIAGRAM



Unprecedented E²PROM applications are now possible since this CMOS E²PROM combines the advantages of bipolar access speeds, low CMOS power needs and nonvolatile data alterability. Typical applications include high speed process controllers, environmentally adaptive robotics, programmable character generators and user programmable video display pattern generators. EXEL high speed E²PROMs can replace system combinations of high speed static RAM and nonvolatile storage used in read mostly environments.

In existing bipolar PROM applications, the CMOS XL46C15 reduces active and standby power requirements substantially. The reprogrammable nature of E²PROM technology provides the ideal prototyping tool for PROM applications and allows cost effective in-field code updates without requiring the removal and replacement of one time programmable PROMs.

DEVICE OPERATION

Read

Data is read from the XL46C15 with a bipolar PROM compatible read cycle. This read cycle is initiated by applying a LOW to $\overline{CS}_1$, a HIGH to CS_2 and a HIGH to CS_3. Data is available within t_{AA} from the time that the address inputs are valid, or t_{CS} after the last chip select input is asserted, whichever is later. When any of the chip select control inputs are not asserted, the I/O pins remain in a high impedance state to eliminate system bus contention.

Programming Mode

The XL46C15 uses a complementary cell technique to obtain high speed data access. The complementary cells are programmed in a two stage process. The first stage is a chip reset cycle which brings both halves of every cell in the memory to a HIGH level. This cycle completes in a maximum of 50ms. The second stage is the write cycle during which each byte is individually addressed and written.

Both of these cycles are performed with $\overline{CS}_1$ at VPP (10.8V to 20.5V). This ensures high data integrity when the device is used in a 5V-only PROM socket yet allows easy rewrites when the device is placed in a PROM programmer or supplied with a high voltage signal.

Chip Reset Cycle

The chip reset cycle is executed by applying V_{PP} to $\overline{CS}_1$ and a HIGH (V_{IH}) to CS_2 (see Figure 3). During the chip reset cycle both halves of each complementary cell in the memory array are set to a logic "1." Since a bit is read by comparing the voltage difference between the two halves of the cell through a differential amplifier, any data read after a chip reset cycle but before a write cycle to the addressed location will be arbitrary and invalid. Once the chip is reset, the memory is ready to be written.

Byte Write Cycle

A byte may not be rewritten without first resetting the chip. Initially, and after each chip reset operation, all bits are in an indeterminate state and are prepared for programming. A byte write cycle is executed by applying V_{PP} to $\overline{CS}_1$ and a LOW (V_{IL}) to CS_2 while holding valid address and data values constant for a minimum t_{WP} specification (see Figure 4). Since a high voltage supply is required for data alteration, the device will operate as a read only memory in a 5V-only environment.

Standby Mode

Power consumption is reduced by 50% when the device is deselected. Applying a HIGH to $\overline{CS}_1$, a LOW to CS_2, or a LOW to CS_3 puts the device in standby mode. Power consumption is further reduced in a CMOS environment when the address inputs are held at V_{CC} or V_{SS}.

Endurance

The XL46C15 is designed for applications requiring up to 100 write cycles per byte. Contact EXEL for special screening to higher levels of endurance.

PROGRAMMER SUPPORT

Many PROM and EPROM programmer manufacturers are supporting the XL46C15. Please contact EXEL for a list of qualified programmers.

MODE SELECTION

$\overline{CS}_1$	CS_2	CS_3	Mode	I/O Pins
V_{IL}	V_{IH}	V_{IH}	Read	D_{OUT}
<6V	V_{IL}	X	Standby	High Z
V_{IH}	X	X	Standby	High Z
<6V	X	V_{IL}	Standby	High Z
V_{PP}	V_{IL}	X	Byte Write	D_{IN}
V_{PP}	V_{IH}	X	Chip Reset	High Z

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... -0°C to +70°C
Storage Temperature ..... -65°C to +150°C
Lead Soldering Temperature (less than 10 seconds) ..... 300°C
Supply Voltage ..... -1.0V to +7.0V
Voltage on Any Pin (Except $\overline{CS_1}$) ..... -1.0V to (V_{CC} +0.5V)
Voltage on $\overline{CS_1}$ Pin ..... -1.0V to +20.5V
ESD Rating 2000V
DC Output Current ..... -70mA

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5V ±5%

Symbol	Parameter	Test Conditions	Limits		Units
			Min.	Max.	
V_{IL}	Input Low Voltage		-0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} +0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 6mA; V_{CC} = 4.75V		0.45	V
V_{OH}	Output High Voltage	I_{OH} = -2mA; V_{CC} = 4.75V	2.4		V
V_C	Input Clamp Voltage	I_{IN} = -18mA; V_{CC} = 4.75V		-1.0	V
V_{PP}	Program Voltage on $\overline{CS_1}$		10.8	20.5	V
I_{SC}	Output Short Circuit Current[1]	V_{OUT} = 0V; V_{CC} = 5.25V		-70	mA
I_{PP}	VPP Supply Current	WRITE or RESET modes		1.5	mA
I_{IH}	Input Leakage Current — HIGH	V_{IN} = V_{CC} = 5.25V		10	mA
I_{LI}	Input Leakage Current — LOW	V_{IN} = 0V; V_{CC} = 5.25V		-10	mA
I_{LO}	Output Leakage Current	STANDBY mode; V_{CC} = 5.25V V_{OUT} = 0 to 5.5V;		±10	mA
I_{CC}	V_{CC} Current — Active (TTL)	READ mode; t_{RC} = min.		90	mA
I_{SB}	V_{CC} Current — Standby (TTL)	STANDBY mode		45	mA
I_{SBC}	V_{CC} Current — Standby (CMOS)	$\overline{CS_1}$ V_{CC} - 0.2V; CS_2,CS_3 0.2V ; V_{IN} 0.2V or V CC - 0.2V		35	mA

Note:
1. During I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

CAPACITANCE

T_A = +25°C, f = 1.0MHz, V_{CC} = 5V

Symbol	Operating Temperature	Test Conditions	Limits		Units
			Min.	Max.	
$C_{I/O}$	Input/Output Capacitance	STANDBY mode; $V_{I/O}$ = 2V		10	pF
C_{IN}	Input Capacitance	V_{OUT} = OV		10	pF

AC CHARACTERISTICS

Read Cycle (See Figures 1 and 2.)
T_A = 0°C to +70°C, V_{CC} = 5V ±5%

Symbol	Parameter	XL46C15-55 Limits		XL46C15-60 Limits		XL46C15-70 Limits		XL46C15-85 Limits		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	55		60		70		85		ns
t_{AA}	Address Access Time		55		60		70		85	ns
t_{CS}	$\overline{CS_1}$, CS_2 or CS_3 Access Time		35		40		40		45	ns
t_{LZ}	Chip Enable to Output LOW Z	5		5		5		5		ns
t_{HZ}	Chip Disable to Output HIGH Z	0	35	0	40	0	40	0	45	ns
t_{OH}	Output Hold from Address Change	10		10		10		10		ns

Chip Reset and Byte Write Cycles (See Figures 3 and 4.)
T_A = +20°C to +30°C, V_{CC} = 5V ±5%

Symbol	Parameter	XL46C15 Limits		Units
		Min.	Max.	
t_{RP}	Reset Pulse Width	50		ms
t_{WP}	Write Pulse Width	5		ms
t_{SC}	CS_2 Setup Time	0		ns
t_{HC}	CS_2 Hold Time	0		ns
t_{WR}	Write Recovery Time[1]	10		ms
t_{AS}	Address Setup Time	0		ns
t_{AH}	Address Hold Time	500		ns
t_{DS}	Data Setup Time	0		ns
t_{DH}	Data Hold Time	0		ns

Note:
1. t_{WR} is defined as the minimum time required after a write pulse before initiating a data read cycle. This parameter is measured from the time at which the falling edge of $\overline{CS_1}$ reaches 5.5V until a valid read cycle is initiated. If a read cycle is initiated earlier than the minimum t_{WR} the output data may be invalid. Subsequent write cycles may be initiated immediately without delaying for t_{WR}.

Input Signal Amplitude	0V to 3V
Input Rise and Fall Times	5ns (1V to 2V)
Frequency	1MHz
Timing Reference Value	1.5V

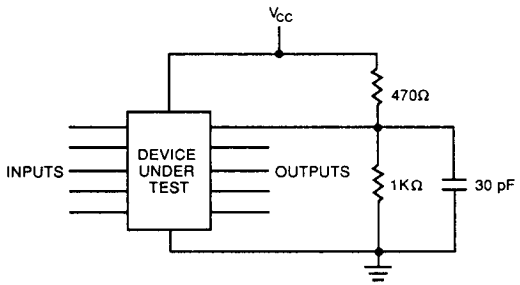


Figure 1. AC TEST CONDITIONS

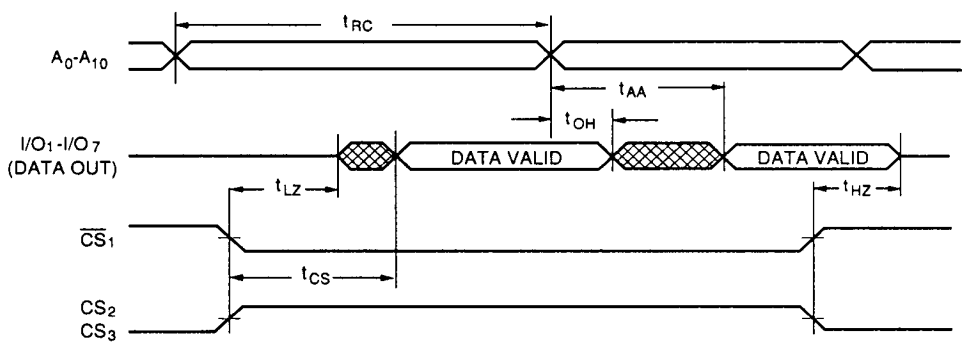


FIGURE 2. READ CYCLE TIMING

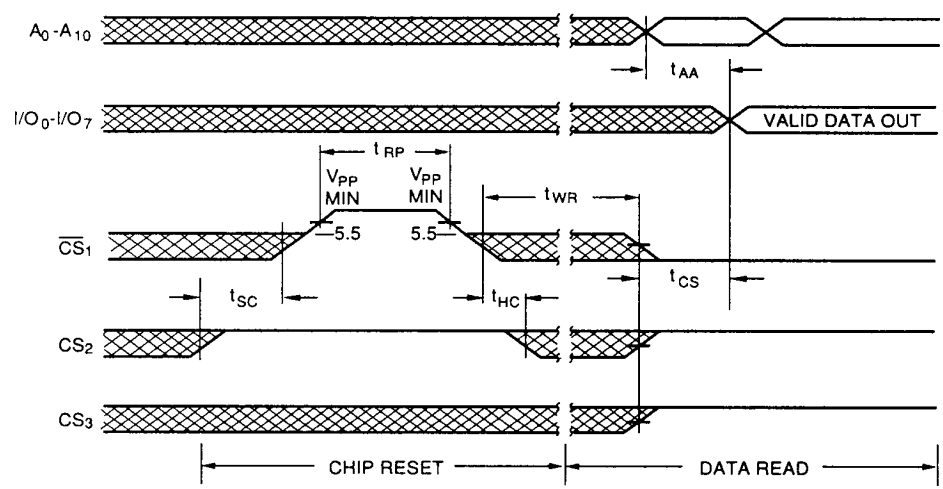


FIGURE 3. CHIP RESET CYCLE

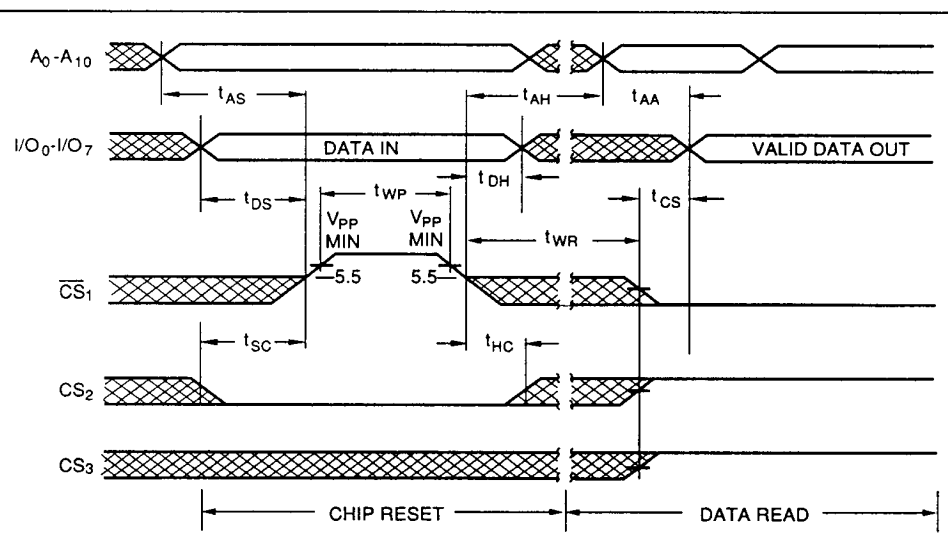


FIGURE 4. BYTE WRITE CYCLE