SEMICONDUCTOR

**TOSHIBA**

TECHNICAL DATA

TOSHIBA PHOTOCOUPLER

# 6N135, 6N136

GaAℓAs IRDE & PHOTO IC

(6N135)

DIGITAL LOGIC ISOLATION.

LINE RECEIVER.

POWER SUPPLY CONTROL

SWITCHING POWER SUPPLY

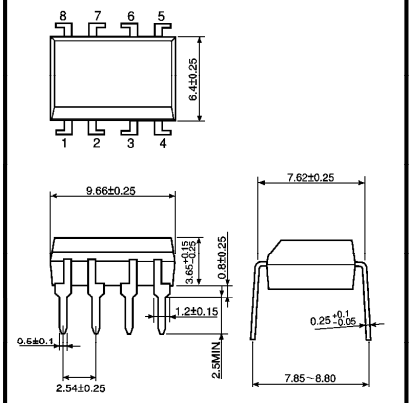
TRANSISTOR INVERTER.

The TOSHIBA 6N135 and 6N136 consists of a high emitting diode and a one chip photo diode-transistor.

Each unit is 8-lead DIP package.

- Isolation Voltage : 2500Vrms (Min.)
- High Speed : $t_{pHL}$, $t_{pLH} = 0.5\mu s$ (Typ.) ($R_L = 1.9k\Omega$)
- TTL Compatible
- If base pin is open, output signal will be noisy by environmental condition. For this base, TLP550 is suitable
- UL Recognized : UL1577, File No. E67349

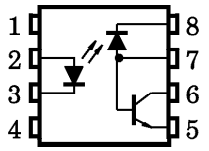
Unit in mm



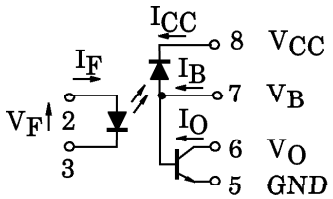

| | |
|---|---|
| JEDEC | — |
| EIAJ | — |
| TOSHIBA | 11-10C4 |

Weight : 0.54g

PIN CONFIGURATIONS




1. N.C.
2. ANODE
3. CATHODE
4. N.C.
5. EMITTER
6. COLLECTOR
7. BASE, ANODE
8. CATHODE



(6N135)

MAXIMUM RATINGS (Ta = 25°C)

| | CHARACTERISTIC | | SYMBOL | RATING | UNIT |
|---|---|---|---|---|---|
| LED | Forward Current | (Note 1) | $I_F$ | 25 | mA |
| | Pulse Forward Current | (Note 2) | $I_{FP}$ | 50 | mA |
| | Total Pulse Forward Current | (Note 3) | $I_{FPT}$ | 1 | A |
| | Reverse Voltage | | $V_R$ | 5 | V |
| | Diode Power Dissipation | (Note 4) | $P_D$ | 45 | mW |
| DETECTOR | Output Current | | $I_O$ | 8 | mA |
| | Peak Output Current | | $I_{OP}$ | 16 | mA |
| | Emitter-Base Reverse Voltage (Pin 5-7) | | $V_{EB}$ | 5 | V |
| | Supply Voltage | | $V_{CC}$ | −0.5~15 | V |
| | Output Voltage | | $V_O$ | −0.5~15 | V |
| | Base Current (Pin 7) | | $I_B$ | 5 | mA |
| | Output Power Dissipation | (Note 5) | $P_o$ | 100 | mW |
| Operating Temperature Range | | | $T_{opr}$ | −55~100 | °C |
| Storage Temperature Range | | | $T_{stg}$ | −55~125 | °C |
| Lead Solder Temperature (10s) | | (Note 6) | $T_{sol}$ | 260 | °C |
| Isolation Voltage | | (Note 7) | $BV_S$ | 2500 | Vrms |

Note 1 : Derate 0.8mA above 70°C.
Note 2 : 50% duty cycle, 1ms pulse width.
Derate 1.6mA / °C above 70°C.
Note 3 : Pulse width 1$\mu$s, 300pps.
Note 4 : Derate 0.9mW / °C above 70°C.
Note 5 : Derate 2mW / °C above 70°C.
Note 6 : Soldering portion of lead : up to 2mm from the body of the device.
Note 7 : R.H.≦60%, AC / 1min.

(6N135)

ELECTRICAL CHARACTERISTICS

OVER RECOMMENDED TEMPERATURE (Ta = 0°C~70°C Unless otherwise noted)

| CHARACTERISTIC | | SYMBOL | TEST CONDITION | MIN. | ※※TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| Current Transfer Ratio | 6N135 | CTR | $I_F$=16mA, $V_O$=0.4V<br>$V_{CC}$=4.5V, Ta=25°C (Note 8) | 7 | 18 | — | % |
| | 6N136 | | | 19 | 24 | — | % |
| | 6N135 | CTR | $I_F$=16mA, $V_O$=0.5V<br>$V_{CC}$=4.5V (Note 1) | 5 | 13 | — | % |
| | 6N136 | | | 15 | 21 | — | % |
| Logic Low Output Voltage | 6N135 | $V_{OL}$ | $I_F$=16mA, $I_O$=1.1mA<br>$V_{CC}$=4.5V | — | 0.1 | 0.4 | V |
| | 6N136 | | $I_F$=16mA, $I_O$=2.4mA<br>$V_{CC}$=4.5V | — | 0.1 | 0.4 | V |
| Logic High Output Current | | $I_{OH}$ | $I_F$=0mA, $V_O$=$V_{CC}$=5.5V<br>Ta=25°C | — | 3 | 500 | nA |
| | | | $I_F$=0mA, $V_O$=$V_{CC}$=15V<br>Ta=25°C | — | 0.1 | 1 | μA |
| | | $I_{OH}$ | $I_F$=0mA, $V_O$=$V_{CC}$=15V | — | — | 50 | μA |
| Logic Low Supply Current | | $I_{CCL}$ | $I_F$=16mA, $V_O$=Open<br>$V_{CC}$=15V | — | 40 | — | μA |
| Logic High Supply Current | | $I_{CCH}$ | $I_F$=0mA, $V_O$=Open<br>$V_{CC}$=15V, Ta=25°C | — | 0.01 | 1 | μA |
| | | $I_{CCH}$ | $I_F$=0mA, $V_O$=Open<br>$V_{CC}$=15V | — | — | 2 | μA |
| Input Forward Voltage | | $V_F$ | $I_F$=16mA, Ta=25°C | — | 1.65 | 1.7 | V |
| Temperature Coefficient of Forward Voltage | | $\Delta V_F / \Delta Ta$ | $I_F$=16mA | — | −1.9 | — | mV / °C |
| Input Reverse Breakdown Voltage | | $BV_R$ | $I_R$=10μA, Ta=25°C | 5 | — | — | V |
| Input Capacitance | | $C_{IN}$ | f=1MHz, $V_F$=0 | — | 60 | — | pF |
| Resistance (Input-Output) | | $R_{I-O}$ | $V_{I-O}$=500V (Note 9) R.H.≦60% | — | $10^{12}$ | — | Ω |
| Capacitance (Input-Output) | | $C_{I-O}$ | f=1MHz (Note 9) | — | 0.6 | — | pF |
| Transistor DC Current Gain | | $h_{FE}$ | $V_O$=5V, $I_O$=3mA | — | 80 | — | — |

※※ All typicals at Ta=25°C

(6N135)

SWITCHING SPECIFICATIONS

(Unless otherwise specified. Ta = 25°C, $V_{CC}$ = 5V, $I_F$ = 16mA)

| CHARACTERISTIC | | SYMBOL | TEST CIRCUIT | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|
| Propagation Delay Time to Logic Low at Output | 6N135 | $t_{pHL}$ | 1 | $R_L$ = 4.1kΩ | — | 0.2 | 1.5 | μs |
| | 6N136 | | | $R_L$ = 1.9kΩ | — | 0.2 | 0.8 | μs |
| Propagation Delay Time to Logic High at Output | 6N135 | $t_{pLH}$ | 1 | $R_L$ = 4.1kΩ | — | 1.0 | 1.5 | μs |
| | 6N136 | | | $R_L$ = 1.9kΩ | — | 0.5 | 0.8 | μs |
| Common Mode Transient Immunity at Logic High Level Output (Note 10) | 6N135 | $CM_H$ | 2 | $I_F$ = 0mA, $V_{CM}$ = 10$V_{p-p}$, $R_L$ = 4.1kΩ | — | 1000 | — | V / μs |
| | 6N136 | | | $I_F$ = 0mA, $V_{CM}$ = 10$V_{p-p}$, $R_L$ = 1.9kΩ | — | 1000 | — | V / μs |
| Common Mode Transient Immunity at Logic Low Level Output (Note 10) | 6N135 | $CM_L$ | 2 | $V_{CM}$ = 10$V_{p-p}$, $R_L$ = 4.1kΩ, $I_F$ = 16mA | — | −1000 | — | V / μs |
| | 6N136 | | | $V_{CM}$ = 10$V_{p-p}$, $R_L$ = 1.9kΩ, $I_F$ = 16mA | — | −1000 | — | V / μs |
| Bandwidth (Note 11) | | BW | — | $R_L$ = 100Ω | — | 2 | — | MHz |

Note 8 : DC CURRENT TRANSFER RATIO is defined as the ratio of output collector current, $I_O$, to the forward LED input current, $I_F$, times 100%.

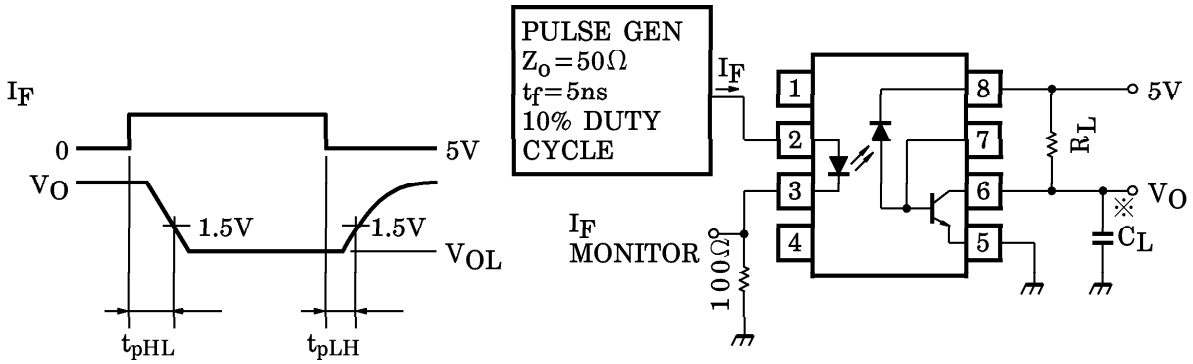
9 : Device considered a two-terminal device : Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7 and 8 shorted together.

10 : Common mode transient immunity in Logic High level is the maximum tolerable (positive) dVCM / dt on the leading edge of the common mode pulse, VCM, to assure that the output will remain in a Logic High state (i.e., $V_O$ > 2.0V).
Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dVCM / dt on the trailing edge of the common mode pulse signal, VCM, to assure that the output will remain in a Logic Low state (i.e., $V_O$ < 0.8V).

11 : The frequency at which the AC output voltage is 3dB below the low frequency asymptote.

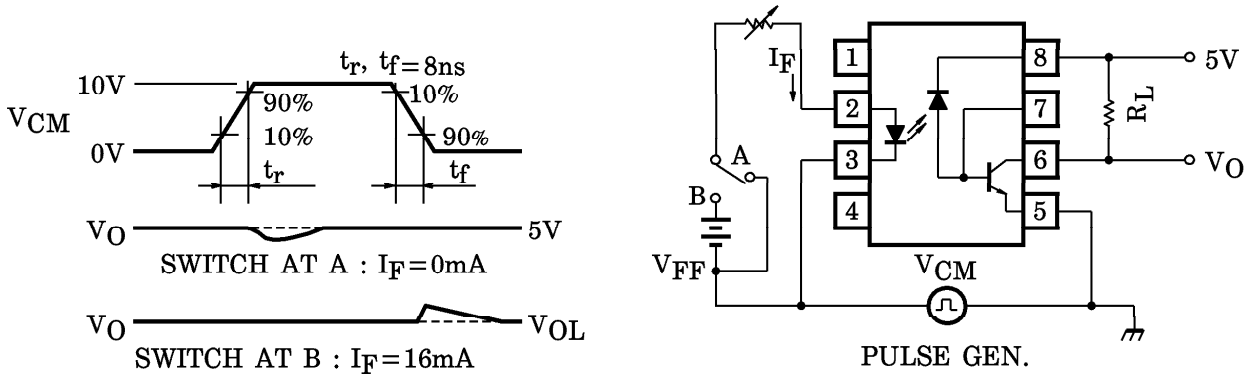
(6N135)

TEST CIRCUIT 1.



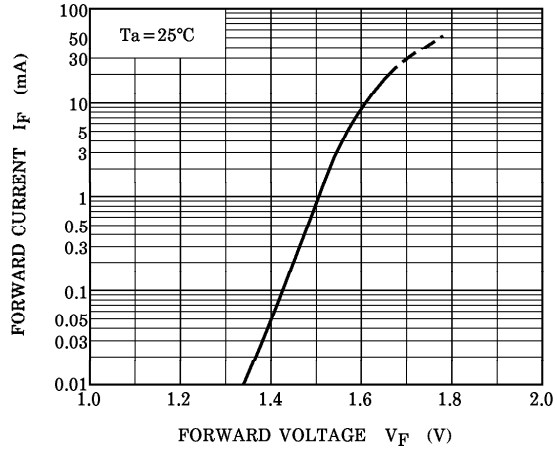

※ $C_L$ is approximately 15pF which includes probe and stray wiring capacitance.

TEST CIRCUIT 2.

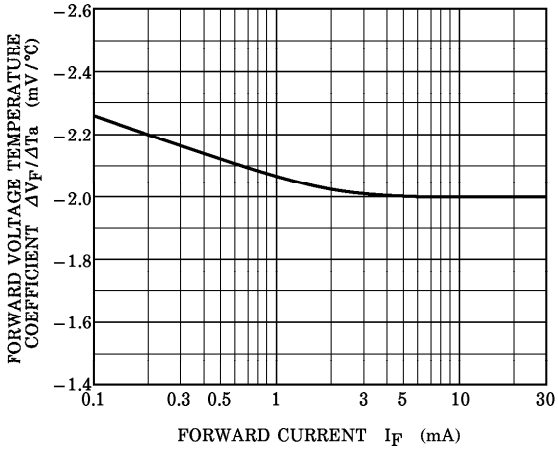


(6N135)

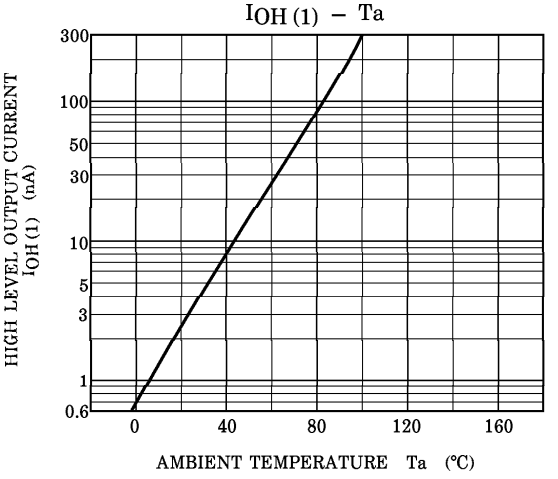
$I_F - V_F$



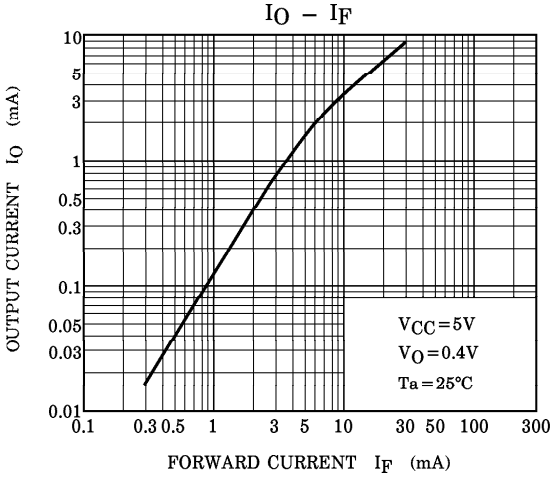

$\Delta T_F / \Delta Ta - I_F$



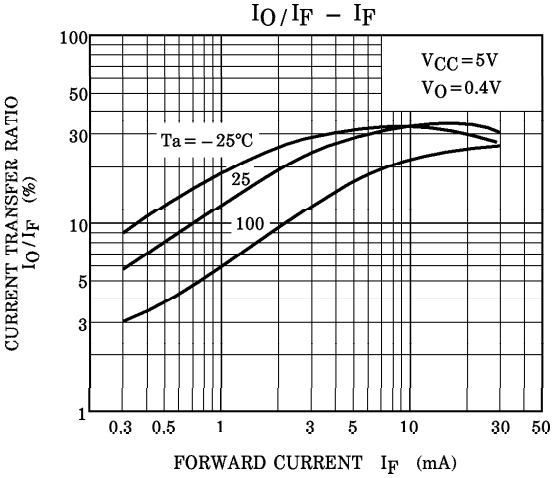

$I_{OH\,(1)} - Ta$



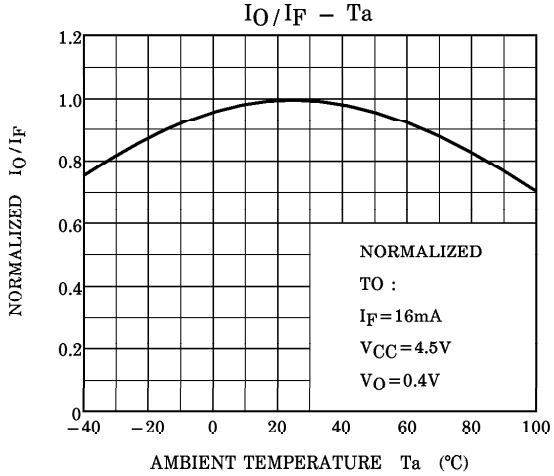

$I_O - I_F$




$I_O / I_F - I_F$

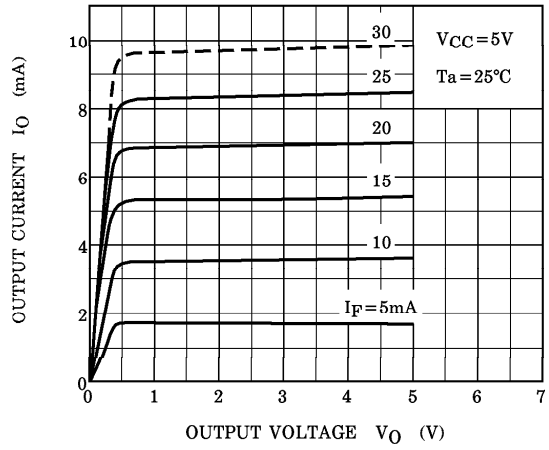



$I_O / I_F - Ta$

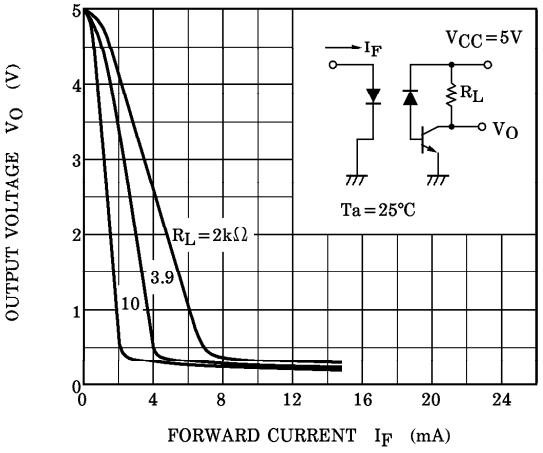


(6N135)

$I_O - V_O$




$V_O - I_F$




$t_{pHL}$, $t_{pLH}$ – $R_L$