



256K x 9 Buffered SRAM Module with Separate I/O

Features

- High-density 2-megabit SRAM module with parity
- High-speed CMOS SRAMs
— Access time of 30 ns
- Buffered address and control inputs
- Low active power
— 6.2W (max.)
- SMD technology
- TTL-compatible inputs and outputs
- Low profile
— Max. height of .52 in.

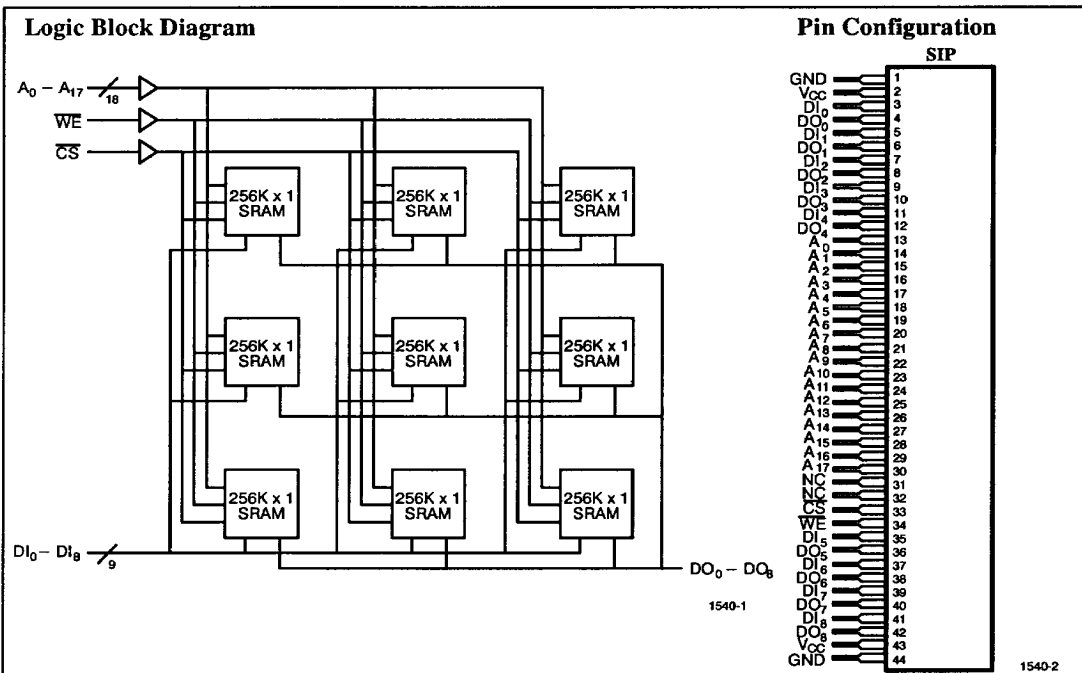
- Small PCB footprint
— 1.6 sq. in.

Functional Description

The CYM1540 is a very high performance 2-megabit static RAM module organized as 256K words by 9 bits. This module is constructed using nine 256K x 1 static RAMs in SOJ packages mounted on an epoxy laminate board with pins. Input buffers are provided on the address and control lines to reduce input capacitance and loading. Writing to the module is accomplished when the chip select (\overline{CS}) and write enable (\overline{WE}) inputs are both LOW. Data on the

data input pins (DI_0 through DI_8) of the device is written into the memory location specified on the address pins (A_0 through A_{17}). Reading the device is accomplished by taking chip select (\overline{CS}) LOW, while write enable (\overline{WE}) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins (A_0 through A_{17}) will appear on the appropriate data output pins (DO_0 through DO_8).

The data output pins remain in a high-impedance state when chip select (\overline{CS}) is HIGH or when write enable (\overline{WE}) is LOW.



9
MODULES

Selection Guide

	1540-30	1540-35	1540-45
Maximum Access Time (ns)	30	35	45
Maximum Operating Current (mA)	1125	1125	1125
Maximum Standby Current (mA)	350	350	350

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature	-45°C to +125°C
Ambient Temperature with Power Applied	-10°C to +85°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

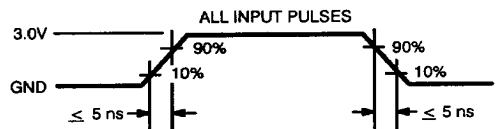
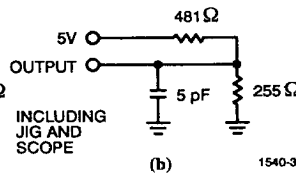
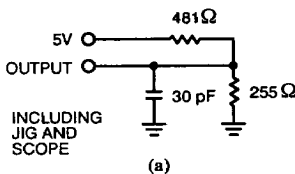
Parameters	Description	Test Conditions	CYM1540		Units
			Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4	V
V _{IHA}	Input HIGH Voltage A ₀ - A ₁₇ , \overline{CS} , \overline{WE}		2.0	6.0	V
V _{IHD}	Input HIGH Voltage D _{I0} - D _{I8}		2.2	6.0	V
V _{ILA}	Input LOW Voltage A ₀ - A ₁₇ , \overline{CS} , \overline{WE}			0.8	V
V _{ILD}	Input LOW Voltage D _{I0} - D _{I8}		-0.5	0.8	V
V _{IK}	Input Clamp Level A ₀ - A ₁₇ , \overline{CS} , \overline{WE}	V _{CC} = Min., I _{IN} = -18 mA		-1.2	V
I _{IL}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-10	+10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} Output Disabled	-10	+10	μA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, CS ≤ V _{IL}		1125	mA
I _{SB1}	Automatic \overline{CS} Power-Down Current [1]	V _{CC} = Max., \overline{CS} ≥ V _{IH} Min. Duty Cycle = 100%		350	mA
I _{SB2}	Automatic \overline{CS} Power-Down Current [1]	V _{CC} = Max., \overline{CS} ≥ V _{CC} - 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} < 0.2V		230	mA

Capacitance [2]

Parameters	Description	Test Conditions	Max.	Units
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	15	pF
C _{OUT}	Output Capacitance		15	pF

Notes:

1. A pull-up resistor to V_{CC} on the \overline{CS} input is required to keep the device deselected during power-up, otherwise I_{SB} will exceed values given.
2. Tested on a sample basis.

AC Test Loads and Waveforms


Switching Characteristics Over the Operating Range^[3]

Parameters	Description	1540-30		1540-35		1540-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t _{RC}	Read Cycle Time	30		35		45		ns
t _{AA}	Address to Data Valid		30		35		45	ns
t _{OHA}	Data Hold from Address Change	5		5		5		ns
t _{ACS}	\overline{CS} LOW to Data Valid		30		35		45	ns
t _{LZCS}	\overline{CS} LOW to Low Z	5		5		5		ns
t _{HZCS}	\overline{CS} HIGH to High Z ^[4]	3	20	3	20	3	25	ns
t _{PU}	\overline{CS} LOW to Power-Up	3		3		3		ns
t _{PD}	\overline{CS} HIGH to Power-Down		30		35		45	ns
WRITE CYCLE ^[5]								
t _{WC}	Write Cycle Time	30		35		45		ns
t _{SCS}	\overline{CS} LOW to Write End	20		25		35		ns
t _{AW}	Address Set-Up to Write End	20		25		35		ns
t _{HA}	Address Hold from Write End	4		4		5		ns
t _{SA}	Address Set-Up from Write Start	5		5		5		ns
t _{PWE}	\overline{WE} Pulse Width	20		25		35		ns
t _{SD}	Data Set-Up to Write End	20		25		35		ns
t _{HD}	Data Hold from Write End	5		5		5		ns
t _{LZWE}	\overline{WE} HIGH to Low Z	3		3		3		ns
t _{HZWE}	\overline{WE} LOW to High Z ^[4]	3	20	3	25	3	30	ns

Notes:

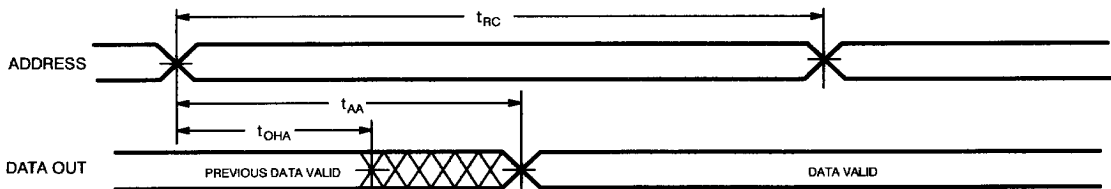
- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- t_{HZCS} and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
- The internal write time of the memory is defined by the overlap of \overline{CS} LOW and \overline{WE} LOW. Both signals must be LOW to initiate a write and

either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

- \overline{WE} is HIGH for read cycle.
- Device is continuously selected, $\overline{CS} = V_{IL}$.
- Address valid prior to or coincident with \overline{CS} transition low.
- If \overline{CS} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.

Switching Waveforms

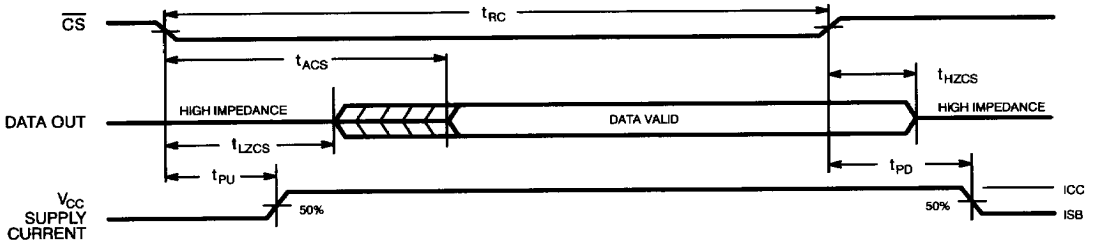
Read Cycle No. 1^[6, 7]



1540-5

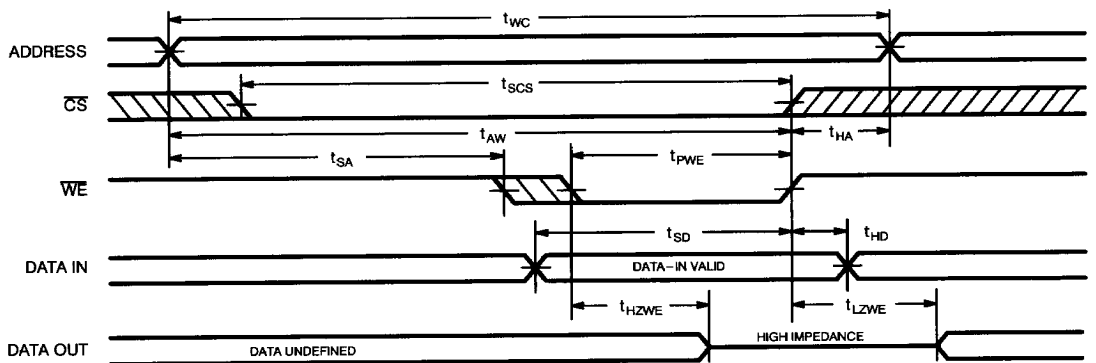
Switching Waveforms (continued)

Read Cycle No. 2 [6, 8]



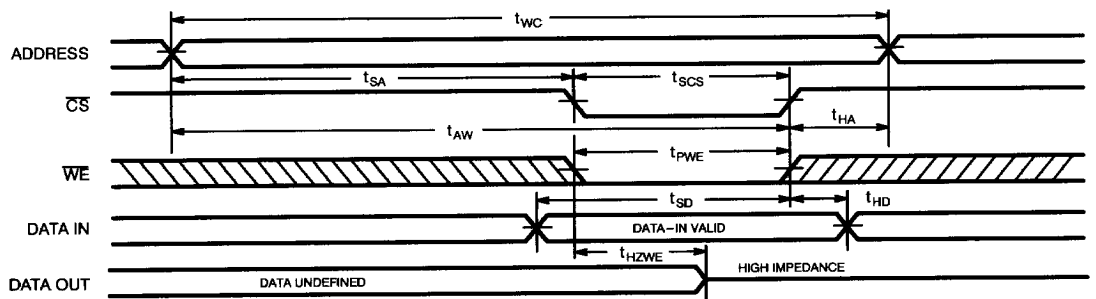
1540-6

Write Cycle No. 1 (\overline{WE} Controlled) [5]



1540-7

Write Cycle No. 2 (\overline{CS} Controlled) [5, 9]



1540-8

Truth Table

CS	WE	Data In	Data Out	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	X	Data Out ₀₋₈	Read
L	L	Data In ₀₋₈	High Z	Write

Ordering Information

Speed	Ordering Code	Package Type	Operating Range
30	CYM1540-30C	PF02	Commercial
	CYM1540-30C	PS04	
35	CYM1540-35C	PF02	Commercial
	CYM1540-35C	PS04	
45	CYM1540-45C	PF02	Commercial
	CYM1540-45C	PS04	

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