Features

256Kx32 bit CMOS Static
DSP Memory Solution
- Texas Instruments TMS320C3x, TMS320C4x
- Analog SHARC™ DSP
- Motorola DSP96002

Random Access Memory Array
- Fast Access Times: 15, 17, 20 and 25ns
- Individual Byte Enables
- User Configurable Organization with Minimal Additional Logic
- Master Output Enable and Write Control
- TTL Compatible Inputs and Outputs
- Fully Static, No Clocks

Surface Mount Package
- 68 Lead PLCC, No. 99, JEDEC MO-47AE
- Small Footprint, 0.990 Sq. In.
- Multiple Ground Pins for Maximum Noise Immunity

Single +5V (±5%) Supply Operation

256Kx32, 5V Static Ram

The EDI8L32256C is a high speed, 5V, 8 megabit SRAM. The device is available with access times of 15, 17, 20 and 25ns, allowing the creation of a no wait state DSP memory solution.

The device can be configured as a 256Kx32 and used to create a single chip external data memory solution for Texas Instruments' TMS320C30/31, TMS 320C32 or TMS320C4x, Motorola's DSP96002 and Analog Device's SHARC™ DSP.

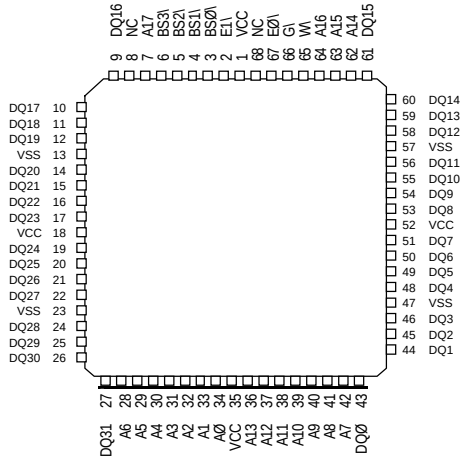
Alternatively the device's chip enables can be used to configure it as a 512Kx16. A 512Kx48 program memory array for Analog's SHARC™ DSP is created using three devices. If this memory is too deep, two 256Kx24s (EDI8L24256C) can be used to create a 256Kx48 array or two 128Kx24s (EDI8L24128C) can be used to create a 128Kx48 array.

The device provides a 32% space savings when compared to two monolithic 256Kx16, 44 pin SOJs.

The device provides a memory upgrade of the EDI8L32128C (128Kx32) and the EDI8L3265C (64Kx32). For more memory the device can be upgraded to the EDI8L32512C (512Kx32).

NOTE: Solder Reflow temperature should not exceed 260°C for 10 seconds.

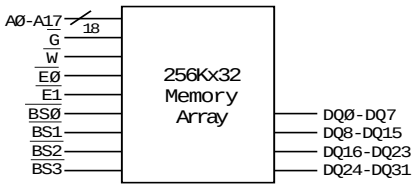
Pin Configurations and Block Diagram



Note: For memory upgrade information refer to page 8, Figure 8 "EDI MCM-L upgrade path".

Pin Names

AØ-A17	Address Inputs
$\overline{EØ}$-$\overline{E1}$	Chip Enables (One per Word)
$\overline{BSØ}$-$\overline{BS3}$	Byte Selects (One per Byte)
$\overline{W}$	Master Write Enable
$\overline{G}$	Master Output Enable
DQØ-DQ31	Common Data Input/Output
VCC	Power (+5V±5%)
VSS	Ground
NC	No Connection



Absolute Maximum Ratings*

Voltage on any pin relative to VSS	-0.5V to 7.0V
Operating Temperature TA (Ambient)	
Commercial	0°C to + 70°C
Industrial	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Power Dissipation	3.1 Watts
Output Current.	20 mA
Junction Temperature, TJ	175°C

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.75	5.0	5.25	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	VCC+0.5	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels	VSS to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 1

(note: For TEHQZ,TGHQZ and TWLQZ, CL = 5pF)

Figure 1

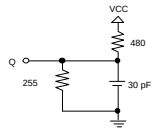
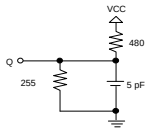


Figure 2



DC Electrical Characteristics

Parameter	Sym	Conditions	Min	Max 15/17	Max 20/25	Units
Operating Power Supply Current	ICC1	$\overline{W}$= VIL, II/O = 0mA, Min Cycle		575	480	mA
Standby (TTL) Supply Current	ICC2	$\overline{E}$ ≥ VIH, VIN ≤ VIL or VIN ≥ VIH, f=ØMHz		120	120	mA
Full StandbySupply Current	ICC3	$\overline{E}$ ≥ VCC-0.2V VIN ≥ VCC-0.2V or VIN ≤ 0.2V		20	20	mA
Input Leakage Current	ILI	VIN = 0V to VCC		±10		µA
Output Leakage Current	ILO	V I/O = 0V to VCC		±10		µA
Output High Volltage	VOH	IOH = -4.0mA	2.4			V
Output Low Voltage	VOL	IOL = 8.0mA		0.4		V

Truth Table

$\overline{E}$	$\overline{W}$	$\overline{G}$	$\overline{BS}$Ø-3	Mode	Output	Power
H	X	X	X	Standby	High Z	ICC2,ICC3,
L	H	H	X	Output Disable	High Z	ICC1
L	X	X	H	Output Disable	High Z	ICC1
L	H	L	L	Read	DOUT	ICC1
L	L	X	L	Write	DIN	ICC1

X Means Don't Care

Capacitance

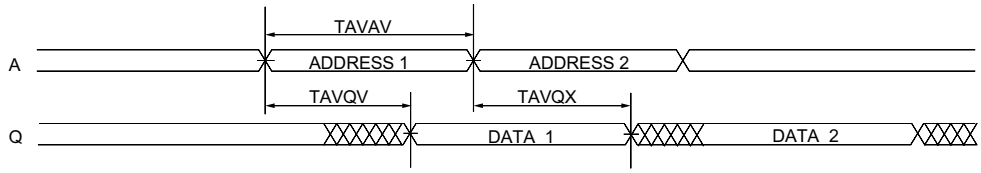
(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Address Lines	CA	20	pF
Data Lines	CD/Q	10	pF
Write & Output Enable Lines	$\overline{W}$, $\overline{G}$	6	pF
Chip Enable Lines/Byte Select	$\overline{E}$, $\overline{BS}$	9	pF

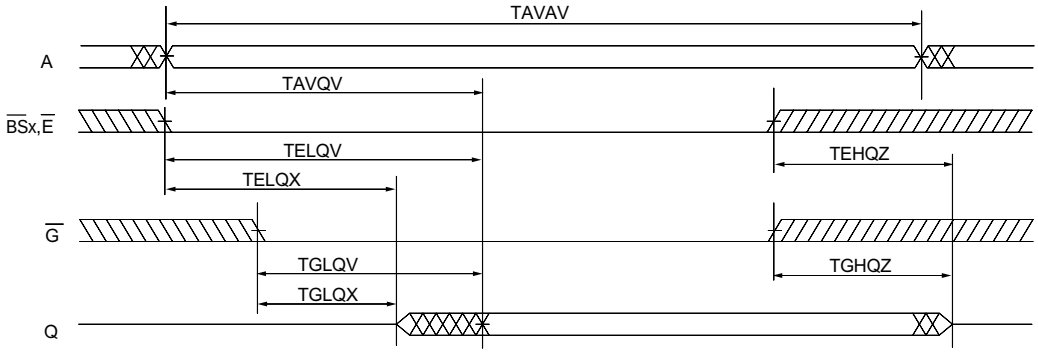
AC Characteristics Read Cycle

	Symbol		15ns		17ns		20ns		25ns		
Parameter	**JEDEC**	**Alt.**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Read Cycle Time	TAVAV	TRC	15		17		20		25		ns
Address Access Time	TAVQV	TAA		15		17		20		25	ns
Chip Enable Access Time	TELQV	TACS		15		17		20		25	ns
Byte Select Access Time	TBLQX	TBLZ		15		17		20		25	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	3		3		3		3		ns
Byte Select to Output in Low Z	TBLQX	TBLZ	3		3		3		3		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ		8		8		10		10	ns
Byte Select to Output in High Z	TBHQZ	TBHZ		8		8		10		10	ns
Output Hold from Address Change	TAVQX	TOH	3		3		3		3		ns
Output Enable to Output Valid	TGLQV	TOE		6		8		10		10	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	2		2		2		2		ns
Output Disable to Output in High Z(1)	TGHQZ	TOHZ		5		6		8		10	ns

Read Cycle 1 - $\overline{W}$ High, $\overline{G}$, $\overline{E}$ Low



Read Cycle 2 - $\overline{W}$ High

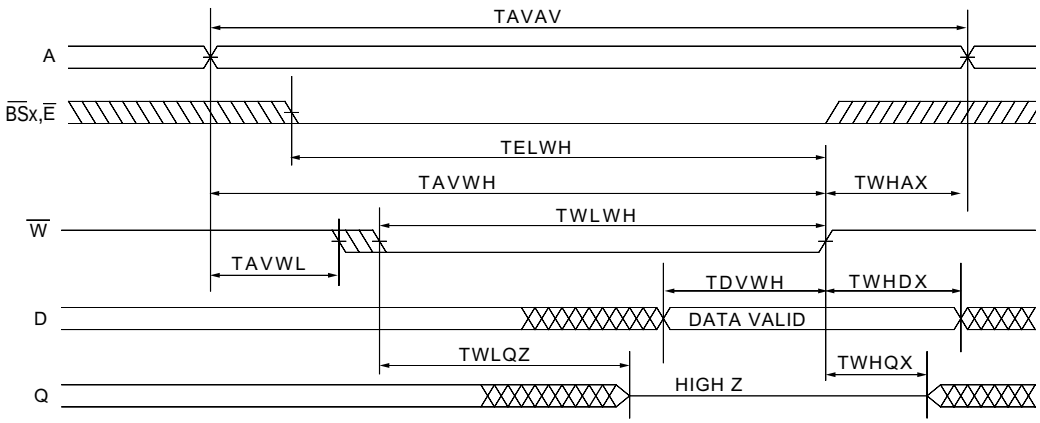


AC Characteristics Write Cycle

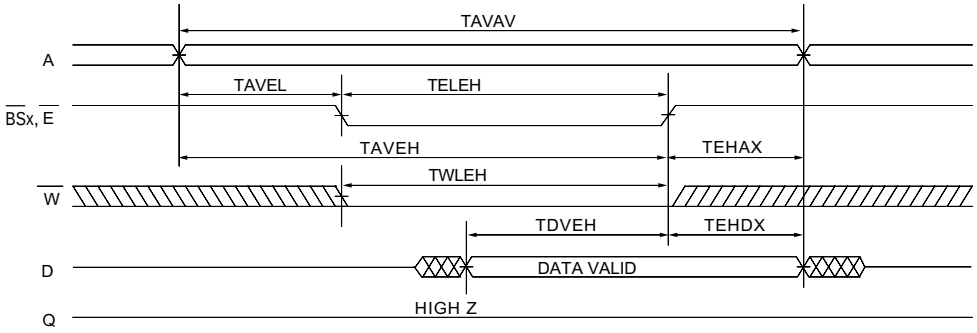
	Symbol		15ns		17ns		20ns		25ns		
Parameter	**JEDEC**	**Alt.**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Write Cycle Time	TAVAV	TWC	15		17		20		25		ns
Chip Enable to End of Write	TELWH	TCW	9		10		15		20		ns
	TELEH	TCW	9		10		15		20		ns
Byte Select to End of Write	TBLWH	TBW	9		10		15		20		ns
Address Setup Time	TAVWL	TAS	0		0		0		0		ns
	TAVEL	TAS	0		0		0		0		ns
Address Valid to End of Write	TAVWH	TAW	10		12		15		15		ns
	TAVEH	TAW	10		12		15		15		ns
Write Pulse Width	TWLWH	TWP	10		12		15		15		ns
	TWLEH	TWP	10		12		15		15		ns
Write Recovery Time	TWHAX	TWR	0		0		0		0		ns
	TEHAX	TWR	0		0		0		0		ns
Data Hold Time	TWHDX	TDH	0		0		0		0		ns
	TEHDX	TDH	0		0		0		0		ns
Write to Output in High Z (1)	TWLQZ	TWHZ	0	6	0	7	0	7	0	10	ns
Data to Write Time	TDVWH	TDW	6		8		8		12		ns
	TDVEH	TDW	6		8		8		12		ns
Output Active from End of Write (1)	TWHQX	TWLZ	2		2		2		2		ns

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1 - $\overline{W}$ Controlled



Write Cycle 2 - $\overline{E}$ Controlled



Ordering Information

Commercial (0°C to 70°C)

Part Number	Speed (ns)	Package No.
EDI8L32256C15AC	15	99
EDI8L32256C17AC	17	99
EDI8L32256C20AC	20	99
EDI8L32256C25AC	25	99

Industrial (-40°C to +85°C)

Part Number	Speed (ns)	Package No.
EDI8L32256C17AI	17	99
EDI8L32256C20AI	20	99
EDI8L32256C25AI	25	99

Package Description

Package No. 99
68 Lead PLCC
JEDEC MO-47AE

Weight = 4.2g

Theta J_A = 40˚C/W

Theta J_C = 15˚C/W