HD81502FS
ISDN I-Interface LSI

The HD81502FS provides ISDN basic user-network interface (layer 1) functions, ISDN user-network interface data link layer (layer 2) functions, and ISDN user-network interface layer 3 functions conforming to CCITT I-Series Recommendations. It has a built-in S-interface (for slave mode), 8-bit CPU, and host CPU interface. It includes general-purpose timers, a watchdog timer, memory management unit (MMU), B-channel select function, and loopback test function. Low power dissipation means that the HD81502FS can be operated from a local power supply. The ideal application for the HD81502FS is ISDN (TE1) terminal equipment.

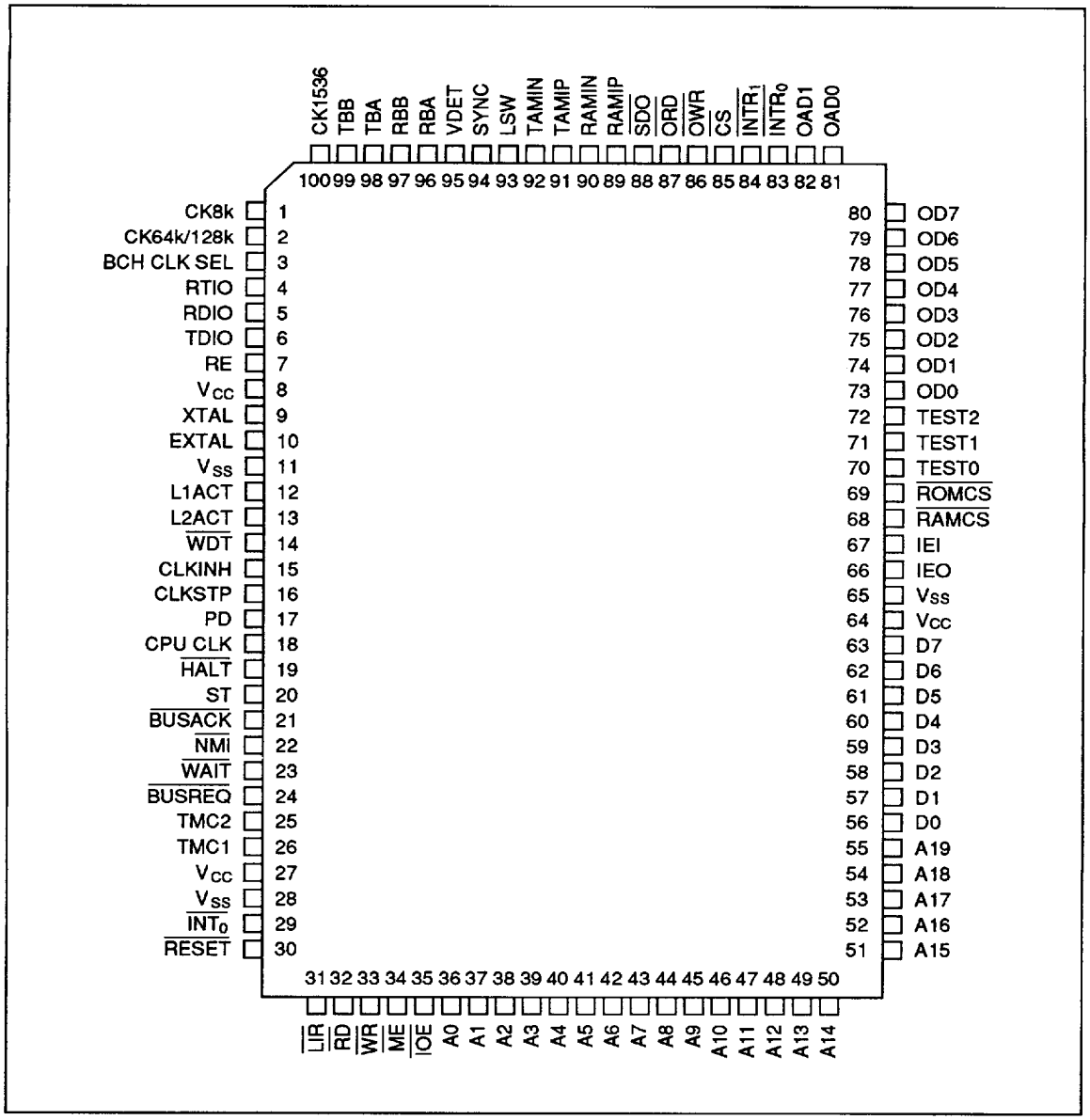
Features

- Layer 1 (CCITT Recommendation I.430) (Slave operation)
  - — Transmission rate: 192 kb/s
  - — Channel structure: 2B + D
  - — Synchronization control (timing recovery, frame alignment)
  - — D-channel collision control using E-bit (internal retransmission control function)
  - — Multiframing control using Q-bit
  - — E-bit output function
  - — Two B-channel operating modes
    Individual mode (64 kb/s per channel)
    Bulk mode of B1 + B2 (128 kb/s total)
  - — Choice of internal or external clock for B-channel data input/output
  - — Incoming detection function
- Layer 2 (CCITT Recommendation I.441)
  - — High-level data link control (HDLC) frame control (including flag control, FCS addition/check, 0 insertion/deletion, idle detection, etc.)
- Host microprocessor interface
  - — Directly connectable to 8086-series microprocessors
  - — Programmed I/O data transfer mode
  - — 8-bit data bus
- Built-in 8-bit microprocessor (64180Z core)
  - — Protocol processing for layers 2 and 3
  - — MMU: 1-MB address space
  - — Two timers
  - — One watchdog timer (WDT)
- B-channel select function
  - — B1/B2 I/O pins are selectable
- Loopback test function
- Memory chip select function
- Layers 1 and 2 only operating mode
- Power-down mode for low power operation
  - — Power can be supplied externally from the network (phantom mode)
- Built-in crystal oscillator circuit
- High reliability and lower power dissipation realized by 1.3-μm CMOS process
- TTL/CMOS compatible inputs and outputs
- +5 V ± 5% single power supply
- 100-pin Quad. Flat Package (QFP)

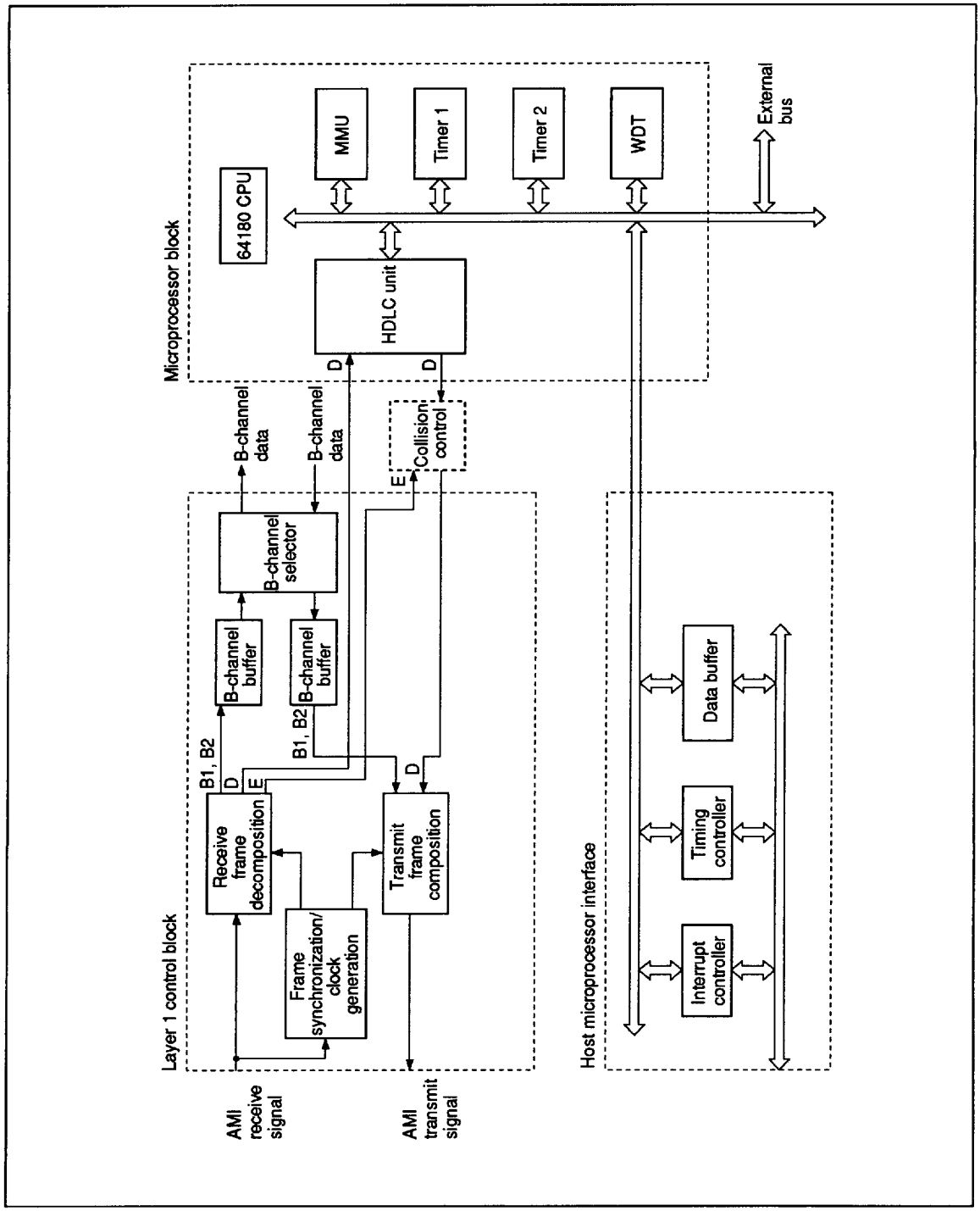
Operating Modes

- Layer mode selection
  - — Normal mode: All functions of layers 1 and 2
  - — Layer 1 only mode: Independent operation of layer 1 functions
  - — Layer 2 only mode: Independent operation of layer 2 functions
- B-channel data input/output clock selection
  - — Internal clock mode: Internal clock is used (8 kHz, 64/128 kHz clock)
  - — External clock mode: External clock is used (8 kHz, 64/128 kHz clock)
- B-channel configuration
  - — Normal mode: B1 and B2 are used as separate 64 kbit/s channels.
  - — Bulk mode: B1 and B2 are used as one 128 kbit/s channel (B1 + B2).
- Collision control
  - — Normal mode: The collision detection function operates only on the address field.
  - — ID mode: The collision detection function operates on the address and information fields. (A collision may not be detected in frames. Normal mode if the same address is assigned to two.) In this mode, the CPU must retransmit the data after a collision has occurred.
- B-channel select function
  - — Normal mode: Receive B1 and B2 channel data on RBA and RBB, respectively, transmit B1 and B2 channel data on TBA and TBB, respectively
  - — Reverse mode: Receive B2 and B1 channel data on RBA and RBB, respectively
  - — Transmit B2 and B1 channel data on TBA and TBB, respectively
- Loopback mode
  - — D-channel local/remote loop
  - — B-channel local/remote loop
- Low power dissipation mode selection
  - — Normal mode: 6.144-MHz layer 2 microprocessor operation clock (110 mW typ)
  - — Power-down mode: 3.072-MHz layer 2 microprocessor operation clock (70 mW typ)
  - — Clock stop mode: All functions disabled except incoming detection (0.525 mW or less)

Pin Arrangement



Block Diagram



Layer 1 Control Block

This block implements basic user-network interface functions using a 2B + D channel structure as specified by CCITT Recommendation I.430. The intended application is ISDN terminal equipment.

Microprocessor Block

This block consists of an HDLC unit, an 8-bit CPU, two timers, a watchdog timer(WDT), and a memory management unit (MMU). It implements ISDN layer 2 and 3 functions (see CCITT Recommendations I.441 and I.451; respectively).

Host Microprocessor Interface Block

This block allows data to be transferred to/from a host microprocessor.

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	–0.3 to +7.0	V
Input voltage	V_{in}	–0.3 to V_{CC} + 0.3	V
Operating temperature	T_{opr}	–10 to +70	°C
Storage temperature	T_{stg}	–55 to +125	°C

Note: Although this product has circuits to protect input pins from electrostatic discharge and strong electric fields, be careful not to apply voltages higher than absolute maximum ratings.

To assure normal operation, we recommend V_{in} and V_{out} to be in the range of $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{CC}$.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Operating temperature	T_{opr}	–10	25	70	°C
Input voltage	V_{in}	–0.3	—	V_{CC} + 0.3	V

DC Characteristics (V_{CC} = 5 V ± 5%, V_{SS} = 0 V, T_a = –10 to +70°C, unless otherwise specified)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input high voltage: $\overline{\text{RESET}}$, EXTAL, $\overline{\text{NMI}}$, and VDET pins	V_{IH1}	V_{CC} – 0.6	—	V_{CC} + 0.3	V	
Input high voltage: pins other than $\overline{\text{RESET}}$, EXTAL, $\overline{\text{NMI}}$, and VDET	V_{IH2}	2.2	—	V_{CC} + 0.3	V	
Input low voltage: $\overline{\text{RESET}}$, EXTAL, $\overline{\text{NMI}}$, and VDET pins	V_{IL1}	–0.3	—	0.6	V	
Input low voltage: Pins other than $\overline{\text{RESET}}$, EXTAL, $\overline{\text{NMI}}$, and VDET pins	V_{IL2}	–0.3	—	0.8	V	
Output high voltage: All output pins	V_{OH}	2.4	—	—	V	I_{OH} = –200 µA
		V_{CC} – 1.2	—	—	V	I_{OH} = –20 µA
Output low voltage: All output pins	V_{OL}	—	—	0.45	V	I_{OL} = 2.2 mA
Input leakage current: Input pins other than XTAL and EXTAL	$\|I_{IL}\|$	—	—	10	µA	V_{in} = 0.5 to V_{CC} – 0.5
High-impedance state leakage current	$\|I_{TL}\|$	—	—	10	µA	V_{in} = 0.5 to V_{CC} – 0.5
Power dissipation (normal operation)	I_{CC}	—	19	30	mA	No load on output; CPU f = 6.144 MHz*1
		—	13	18	mA	CPU f = 3.072 MHz*2
Power dissipation (clock stop mode)	I_{CCSTP}	—	—	100	µA	
Pin capacitance	C_P	—	—	15	pF	

Notes: 1. When PD = low.
2. When PD = high.