

### DESCRIPTION

The HYM532120A is a 1M x 32-bit Fast page mode CMOS DRAM module consisting of two HY5118160B in 42/42 pin SOJ or TSOPII on a 72 pin glass-epoxy printed circuit board. 0.22 $\mu$ F decoupling capacitor is mounted for each DRAM.

The HYM532120AW/ASLW/ATW/ASLTW are Tin-Lead plated and HYM532120AWG/ASLWG /ATWG/ASLTWG are Gold plated socket type Single In-line Memory Modules suitable for easy interchange and addition of 4M byte memory.

### FEATURES

- Low power dissipation  
Max. self-refresh 3.85mW (SL-part)  
Max. battery back-up 4.95mW (SL-part)  
Max. CMOS standby 3.3mW (SL-part)

11.0mW

Max. TTL standby 22.0mW

Max. operating

| Speed | Power |
|-------|-------|
| 60    | 1.76W |
| 70    | 1.65W |
| 80    | 1.54W |

- Single power supply of 5V $\pm$  10%
- TTL compatible inputs and outputs
- Fast access time

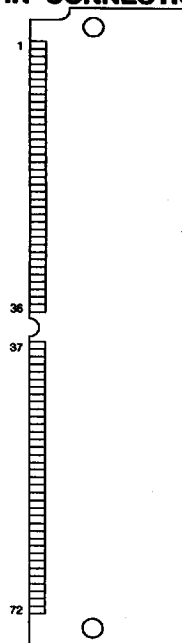
| Speed | tRAC  | tCAC | tpc  |
|-------|-------|------|------|
| 60    | 70ns  | 15ns | 45ns |
| 70    | 80ns  | 20ns | 50ns |
| 80    | 100ns | 20ns | 60ns |

- Fast page mode operation
- CAS-before-RAS, RAS-only, Hidden refresh, Self-refresh
- 1024 refresh cycles / 256ms (SL-part)  
1024 refresh cycles / 16ms

### PIN DESCRIPTION

|            |                       |
|------------|-----------------------|
| RAS0, RAS2 | Row Address Strobe    |
| CAS0-CAS3  | Column Address Strobe |
| WE         | Write Enable          |
| A0-A9      | Address Input         |
| DQ0-DQ34   | Data Input/Output     |
| PD1-PD4    | Presence Detect       |
| Vcc        | Power (+ 5V)          |
| Vss        | Ground                |

### PIN CONNECTION



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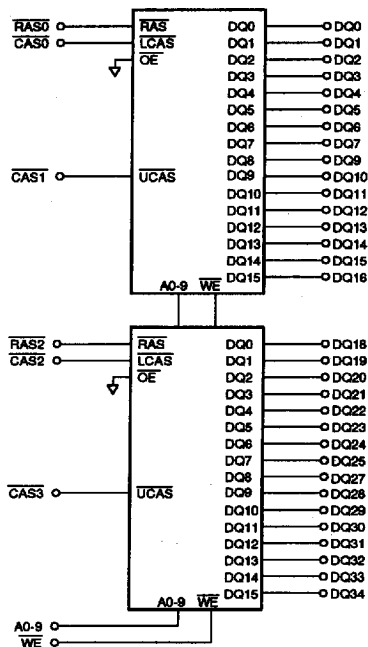
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PIN NAME

| #  | NAME | #  | NAME |
|----|------|----|------|
| 1  | Vss  | 37 | NC   |
| 2  | DQ0  | 38 | NC   |
| 3  | DQ18 | 39 | Vss  |
| 4  | DQ1  | 40 | CAS0 |
| 5  | DQ19 | 41 | CAS2 |
| 6  | DQ2  | 42 | CAS3 |
| 7  | DQ20 | 43 | CAS1 |
| 8  | DQ3  | 44 | RAS0 |
| 9  | DQ21 | 45 | NC   |
| 10 | Vcc  | 46 | NC   |
| 11 | NC   | 47 | WE   |
| 12 | A0   | 48 | NC   |
| 13 | A1   | 49 | DQ9  |
| 14 | A2   | 50 | DQ27 |
| 15 | A3   | 51 | DQ10 |
| 16 | A4   | 52 | DQ28 |
| 17 | A5   | 53 | DQ11 |
| 18 | A6   | 54 | DQ29 |
| 19 | NC   | 55 | DQ12 |
| 20 | DQ4  | 56 | DQ30 |
| 21 | DQ22 | 57 | DQ13 |
| 22 | DQ5  | 58 | DQ31 |
| 23 | DQ23 | 59 | Vcc  |
| 24 | DQ6  | 60 | DQ32 |
| 25 | DQ24 | 61 | DQ14 |
| 26 | DQ7  | 62 | DQ33 |
| 27 | DQ25 | 63 | DQ15 |
| 28 | A7   | 64 | DQ34 |
| 29 | NC   | 65 | DQ16 |
| 30 | Vcc  | 66 | NC   |
| 31 | A8   | 67 | PD1  |
| 32 | A9   | 68 | PD2  |
| 33 | NC   | 69 | PD3  |
| 34 | RAS2 | 70 | PD4  |
| 35 | NC   | 71 | NC   |
| 36 | NC   | 72 | Vss  |

BLOCK DIAGRAM



PRESENCE DETECT PINS

| PIN | -60 | -70 | -80 |
|-----|-----|-----|-----|
| PD1 | Vss | Vss | Vss |
| PD2 | Vss | Vss | Vss |
| PD3 | NC  | Vss | NC  |
| PD4 | NC  | NC  | Vss |

## ABSOLUTE MAXIMUM RATINGS

| SYMBOL    | PARAMETER                          | RATING      | UNIT |
|-----------|------------------------------------|-------------|------|
| TA        | Ambient Temperature                | 0 to 70     | °C   |
| TSTG      | Storage Temperature                | -55 to 150  | °C   |
| VIN, VOUT | Voltage on Any Pin Relative to Vss | -1.0 to 7.0 | V    |
| Vcc       | Voltage on Vcc Relative to Vss     | -1.0 to 7.0 | V    |
| Ios       | Short Circuit Output Current       | 50          | mA   |
| Pd        | Power Dissipation                  | 2.0         | W    |

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

## RECOMMENDED DC OPERATING CONDITIONS

(TA= 0°C to 70°C)

| SYMBOL | PARAMETER          | MIN. | TYP. | MAX.     | UNIT |
|--------|--------------------|------|------|----------|------|
| Vcc    | Supply Voltage     | 4.5  | 5.0  | 5.5      | V    |
| VIH    | Input High Voltage | 2.4  | -    | Vcc+ 1.0 | V    |
| VIL    | Input Low Voltage  | -1.0 | -    | 0.8      | V    |

NOTE : All voltages are referenced to Vss.

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**DC CHARACTERISTICS**

(TA= 0°C to 70°C, VCC= 5V± 10%, VSS= 0V, unless otherwise noted.)

| SYMBOL | PARAMETER                                                | TEST CONDITIONS                                                                                                            | SPEED/<br>POWER                    | MIN. | MAX.              | UNIT | NOTE  |
|--------|----------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------|------------------------------------|------|-------------------|------|-------|
| ILI    | Input Leakage Current<br>(Any Input Pin)                 | VSS≤ VIN≤ VCC+ 1.0,<br>All other pins not under test= VSS                                                                  |                                    | -20  | 20                | μA   |       |
| ILO    | Output Leakage Current<br>(High Impedance State)         | VSS≤ VOUT≤ VCC,<br>RAS & CAS at VIH                                                                                        |                                    | -10  | 10                | μA   |       |
| Icc1   | VCC Supply Current,<br>Operating                         | trC= trC (min.)                                                                                                            | 60<br>70<br>80                     | -    | 320<br>300<br>280 | mA   | 1,2,3 |
| Icc2   | VCC Supply Current,<br>TTL Standby                       | RAS & CAS at VIH,<br>other inputs≥ VSS                                                                                     |                                    | -    | 4                 | mA   |       |
| Icc3   | VCC Supply Current,<br>RAS-only refresh                  | trC= trC (min.)                                                                                                            | 60<br>70<br>80                     | -    | 320<br>300<br>280 | mA   | 1,3   |
| Icc4   | VCC Supply Current,<br>Fast Page mode                    | tPC= tPC (min.)                                                                                                            | 60<br>70<br>80                     | -    | 220<br>200<br>180 | mA   | 1,2,3 |
| Icc5   | VCC Supply Current,<br>CMOS Standby                      | RAS & CAS ≥ VCC-0.2V                                                                                                       | SL-part                            | -    | 2<br>0.6          | mA   | 5     |
| Icc6   | VCC Supply Current,<br>CAS-before-RAS refresh            | trC= trC (min.)                                                                                                            | 60<br>70<br>80                     | -    | 320<br>300<br>280 | mA   | 1,3   |
| Icc7   | VCC Supply Current,<br>Battery Back Up<br>(SL-part only) | trC= 250μs,<br>CAS= CBR cycling or 0.2V<br>WE= VCC-0.2V<br>A0-A9= VCC-0.2V or 0.2V<br>DQ0-DQ34= VCC-0.2V, 0.2V,<br>or open | trAS≤<br>300ns<br><br>trAS≤<br>1μs | -    | 0.7<br>0.9        | mA   | 1,4,5 |
| Icc8   | VCC Supply Current,<br>Self Prefresh<br>(SL-Part only)   | RAS & CAS ≤0.2v<br>other pins same as Icc7                                                                                 |                                    |      | 0.7               | mA   |       |
| VOL    | Output Low Voltage                                       | IOL= 4.2mA                                                                                                                 |                                    | -    | 0.4               | V    |       |
| VOH    | Output High Voltage                                      | IOH= -5mA                                                                                                                  |                                    | 2.4  | -                 | V    |       |

**NOTE :**

- Icc1, Icc3, Icc4, Icc6 and Icc7 depend on cycle rate.
- Icc1, Icc3, Icc4 and Icc6 depend on output loading. Specified values are obtained with the output open.
- Icc is specified as average current. for Icc1, Icc3 and Icc6, address can be changed maximum two times while RAS= VIL. for Icc4, address can be changed maximum once while CAS= VIH.
- Only trAS(max.)= 1μs is applied to refresh of battery backup but trAS(max.)= 10μs is applied to normal functional operation.
- Icc5(max.)= 0.6mA, Icc7 and Icc8 are applied to SL-part only (HYM532120ASLW/ASLTW/ASLWG/ASLTWG).

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## AC CHARACTERISTICS

(TA= 0°C to 70°C, Vcc= 5V± 10%, Vss= 0V, unless otherwise noted.) NOTE : 1, 2, 3

| #  | SYMBOL | PARAMETER                                | HYM532120AW-Series |      |      |      |      |      | UNIT | NOTE    |
|----|--------|------------------------------------------|--------------------|------|------|------|------|------|------|---------|
|    |        |                                          | -60                |      | -70  |      | -80  |      |      |         |
|    |        |                                          | MIN.               | MAX. | MIN. | MAX. | MIN. | MAX. |      |         |
| 1  | tRC    | Random Read or Write Cycle Time          | 110                | -    | 130  | -    | 150  | -    | ns   |         |
| 2  | tRPC   | RAS to CAS Precharge Time                | 5                  | -    | 5    | -    | 5    | -    | ns   |         |
| 3  | tPC    | Fast Page Mode Cycle Time                | 40                 | -    | 40   | -    | 50   | -    | ns   |         |
| 4  | tRHCP  | RAS Hold Time from CAS Precharge         | 40                 | -    | 40   | -    | 50   | -    | ns   |         |
| 5  | tRAC   | Access Time from RAS                     | -                  | 60   | -    | 70   | -    | 80   | ns   | 5,10,11 |
| 6  | tCAC   | Access Time from CAS                     | -                  | 15   | -    | 20   | -    | 20   | ns   | 5,10    |
| 7  | tAA    | Access Time from Column Address          | -                  | 30   | -    | 35   | -    | 40   | ns   | 5,11    |
| 8  | tCPA   | Access Time from CAS Precharge           | -                  | 35   | -    | 35   | -    | 45   | ns   | 5       |
| 9  | tCLZ   | CAS to Output Low Impedance              | 0                  | -    | 0    | -    | 0    | -    | ns   | 5       |
| 10 | tOFF   | Output Buffer Turn-off Delay             | 0                  | 15   | 0    | 15   | 0    | 15   | ns   | 6       |
| 11 | tT     | Transition Time (Rise and Fall)          | 3                  | 50   | 3    | 50   | 3    | 50   | ns   | 4       |
| 12 | tRP    | RAS Precharge Time                       | 40                 | -    | 50   | -    | 60   | -    | ns   |         |
| 13 | tRAS   | RAS Pulse Width                          | 60                 | 10K  | 70   | 10K  | 80   | 10K  | ns   |         |
| 14 | tRASP  | RAS Pulse Width (Fast Page Mode)         | 60                 | 100K | 70   | 100K | 80   | 100K | ns   |         |
| 15 | tRSH   | RAS Hold Time                            | 15                 | -    | 20   | -    | 20   | -    | ns   |         |
| 16 | tCSH   | CAS Hold Time                            | 40                 | -    | 50   | -    | 60   | -    | ns   |         |
| 17 | tCAS   | CAS Pulse Width                          | 15                 | 10K  | 15   | 10K  | 20   | 10K  | ns   |         |
| 18 | tRCD   | RAS to CAS Delay                         | 15                 | 45   | 20   | 50   | 20   | 60   | ns   | 10      |
| 19 | tRAD   | RAS to Column Address Delay Time         | 15                 | 30   | 15   | 35   | 15   | 40   | ns   | 11      |
| 20 | tCRP   | CAS to RAS Precharge Time                | 5                  | -    | 5    | -    | 5    | -    | ns   |         |
| 21 | tCP    | CAS Precharge Time                       | 10                 | -    | 10   | -    | 10   | -    | ns   |         |
| 22 | tASR   | Row Address Set-up Time                  | 0                  | -    | 0    | -    | 0    | -    | ns   |         |
| 23 | tRAH   | Row Address Hold Time                    | 10                 | -    | 10   | -    | 10   | -    | ns   |         |
| 24 | tASC   | Column Address Set-up Time               | 0                  | -    | 0    | -    | 0    | -    | ns   |         |
| 25 | tCAH   | Column Address Hold Time                 | 10                 | -    | 15   | -    | 15   | -    | ns   |         |
| 26 | tAR    | Column Address Hold Time from RAS        | 55                 | -    | 60   | -    | 75   | -    | ns   |         |
| 27 | tRAL   | Column Address to RAS Lead Time          | 30                 | -    | 35   | -    | 40   | -    | ns   |         |
| 28 | tRCS   | Read Command Set-up Time                 | 0                  | -    | 0    | -    | 0    | -    | ns   |         |
| 29 | tRCH   | Read Command Hold Time Referenced to CAS | 0                  | -    | 0    | -    | 0    | -    | ns   | 7       |
| 30 | tRRH   | Read Command Hold Time Referenced to RAS | 0                  | -    | 0    | -    | 0    | -    | ns   | 7       |
| 31 | tWCH   | Write Command Hold Time                  | 15                 | -    | 15   | -    | 15   | -    | ns   |         |
| 32 | tWCR   | Write Command Hold Time from RAS         | 55                 | -    | 60   | -    | 75   | -    | ns   |         |
| 33 | tWP    | Write Command Pulse Width                | 10                 | -    | 10   | -    | 10   | -    | ns   |         |
| 34 | tRWL   | Write Command to RAS Lead Time           | 20                 | -    | 20   | -    | 20   | -    | ns   |         |
| 35 | tCWL   | Write Command to CAS Lead Time           | 20                 | -    | 20   | -    | 20   | -    | ns   |         |
| 36 | tDS    | Data-In Set-up Time                      | 0                  | -    | 0    | -    | 0    | -    | ns   | 8       |
| 37 | tDH    | Data-In Hold Time                        | 15                 | -    | 15   | -    | 15   | -    | ns   | 8       |
| 38 | tDHR   | Data-In Hold Time Referenced to RAS      | 55                 | -    | 60   | -    | 75   | -    | ns   |         |
| 39 | tREF   | Refresh Period (1024 cycles)             | -                  | 16   | -    | 16   | -    | 16   | ms   | 12      |
|    |        | SL-part                                  | -                  | 256  | -    | 256  | -    | 256  |      |         |
| 40 | tWCS   | Write Command Set-up Time                | 0                  | -    | 0    | -    | 0    | -    | ns   | 9       |

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**AC CHARACTERISTICS**

(continued)

(continued)

| #  | SYMBOL | PARAMETER                                  | HYM532120AW-Series |      |      |      |      |      | UNIT | NOTE |
|----|--------|--------------------------------------------|--------------------|------|------|------|------|------|------|------|
|    |        |                                            | -60                |      | -70  |      | -80  |      |      |      |
|    |        |                                            | MIN.               | MAX. | MIN. | MAX. | MIN. | MAX. |      |      |
| 41 | tCSR   | CAS Set-up Time (CBR Cycle)                | 5                  | -    | 5    | -    | 5    | -    | ns   |      |
| 42 | tCHR   | CAS Hold Time (CBR Cycle)                  | 10                 | -    | 10   | -    | 10   | -    | ns   |      |
| 43 | tCPT   | CAS Precharge Time (CBR Counter Test)      | 30                 | -    | 35   | -    | 40   | -    | ns   |      |
| 44 | trPS   | RAS Precharge Time<br>(Self Refresh Cycle) | 110                | -    | 130  | -    | 150  | -    | ns   |      |
| 45 | tCHS   | CAS Hold Time<br>(Self Refresh Cycle)      | -50                | -    | -50  | -    | -50  | -    | ns   |      |
| 46 | trASS  | RAS Pulse Width<br>(Self Refresh Cycle)    | 100                | -    | 100  | -    | 100  | -    | ns   |      |
| 47 | trPS   | RAS Precharge Time<br>(Self Refresh Cycle) | 110                | -    | 130  | -    | 150  | -    | ns   |      |

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NOTE :

1. An initial pause of 200 $\mu$ s is required after power-up followed by 8 RAS cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8 RAS-only refresh cycles are required. The device should be carefully initialized to be prevented from being entered into multi bit test mode.
2. If RAS= Vss during power-up, the HYM532120A could begin an active cycle. This condition results in higher power-up current than necessary demands from the power-up. It is recommended that RAS and CAS track with VCC during power-up or be held at a valid VIH in order to minimize the power-up current.
3. VIH(min.) and VIL(max.) are reference levels for measuring timing of input signals. Transition time is measured between VIH and VIL and assumed to be 5ns for all inputs.
4. Refer to the HY5118160B data sheet for detailed information.
5. Measured with a load equivalent to 2 TTL loads and 100pF.
6. toFF(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. Either tRCH or tRRH must be satisfied for a read cycle.
8. These parameters are referenced to CAS leading edge in early write cycles.
9. twCS is not a restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If twCS  $\geq$  twCS(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle.
10. Operation within the tRCD(max.) limit insures that tRAC(max.) can be met. tRCD(max.) is specified as a reference point only. If tRCD is greater than the specified tRCD(max.) limit, then access time is controlled by tCAC.
11. Operation within the tRAD(max.) limit insures that tRAC(max.) can be met. tRAD(max.) is specified as a reference point only. If tRAD is greater than the specified tRAD(max.) limit, then access time is controlled by tAA.
12. tREF(max.)= 256ms is applied to SL-part only (HYM532120ASLW/ASLTW/ASLWG/ASLTWG).

CAPACITANCE

(TA= 25°C, VCC= 5V $\pm$  10%, VSS= 0V, f= 1MHz, unless otherwise noted.)

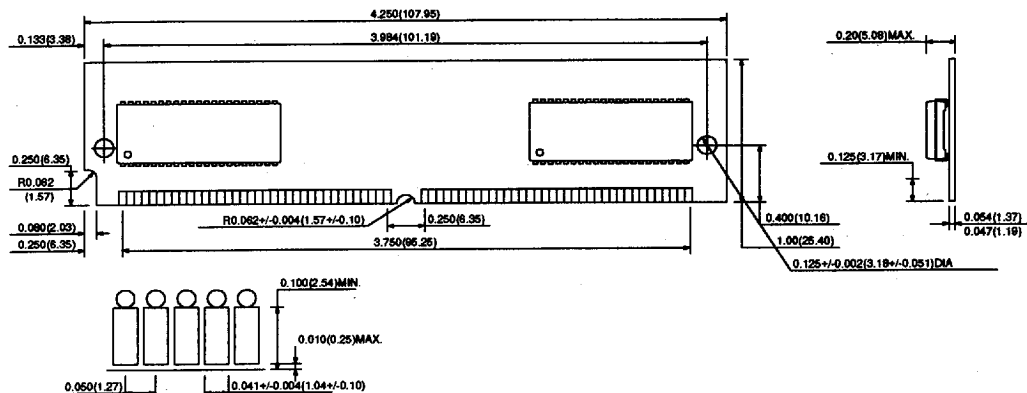
| SYMBOL | PARAMETER                                | TYP. | MAX. | UNIT |
|--------|------------------------------------------|------|------|------|
| CIN1   | Input Capacitance (A0-A9)                | -    | 12   | pF   |
| CIN2   | Input Capacitance (WE)                   | -    | 17   | pF   |
| CIN3   | Input Capacitance (RAS0-RAS2)            | -    | 17   | pF   |
| CIN4   | Input Capacitance (CAS0-CAS3)            | -    | 20   | pF   |
| CDO    | Data Input/Output Capacitance (DQ0-DQ34) | -    | 17   | pF   |

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## PACKAGE INFORMATION

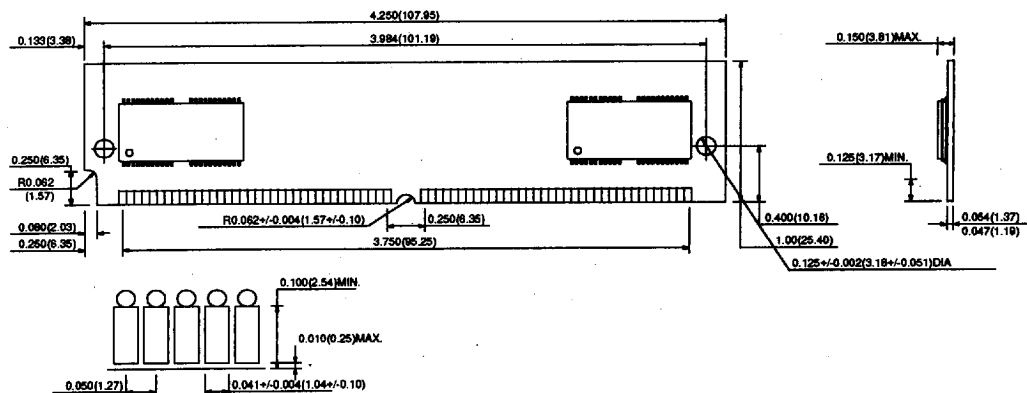
72 pin Single In-line Memory Module (W ; Tin-Lead plated, WG ; Gold plated)  
HYM532120A/ASL (SOJ Mounted)

UNIT : INCH(mm)  
TOLERANCE : +/-0.005(0.13)



HYM532120AT/ASLT (TSOPH Mounted)

UNIT : INCH(mm)  
TOLERANCE : +/-0.005(0.13)



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## ORDERING INFORMATION

| PART NUMBER     | SPEED    | POWER   | PACKAGE | PLATING  |
|-----------------|----------|---------|---------|----------|
| HYM532120AW     | 60/70/80 |         | SIMM    | Tin-Lead |
| HYM532120ASLW   | 60/70/80 | SL-part | SIMM    | Tin-Lead |
| HYM532120ATW    | 60/70/80 |         | SIMM    | Tin-Lead |
| HYM532120ASLTW  | 60/70/80 | SL-part | SIMM    | Tin-Lead |
| HYM532120AWG    | 60/70/80 |         | SIMM    | Gold     |
| HYM532120ASLWG  | 60/70/80 | SL-part | SIMM    | Gold     |
| HYM532120ATWG   | 60/70/80 |         | SIMM    | Gold     |
| HYM532120ASLTWG | 60/70/80 | SL-part | SIMM    | Gold     |

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