

TAA630S

PAL CHROMA DEMODULATOR

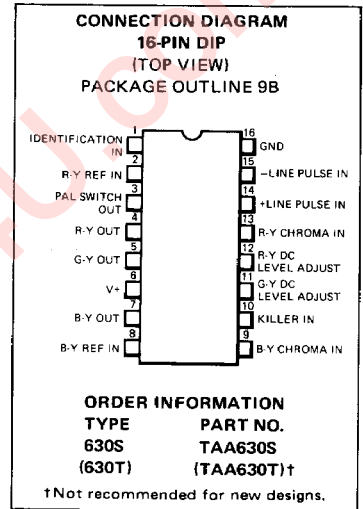
FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The TAA630S is a synchronous demodulator for direct drive of color video output stages. It is constructed on a single silicon chip using the Fairchild Planar[®] epitaxial process. The TAA630S is designed for use in color television receivers operating on the Phase Alternate Line (PAL) system. This circuit consists of two synchronous demodulators, a decoding matrix, a PAL switch with internal multivibrator and a color killer switch.

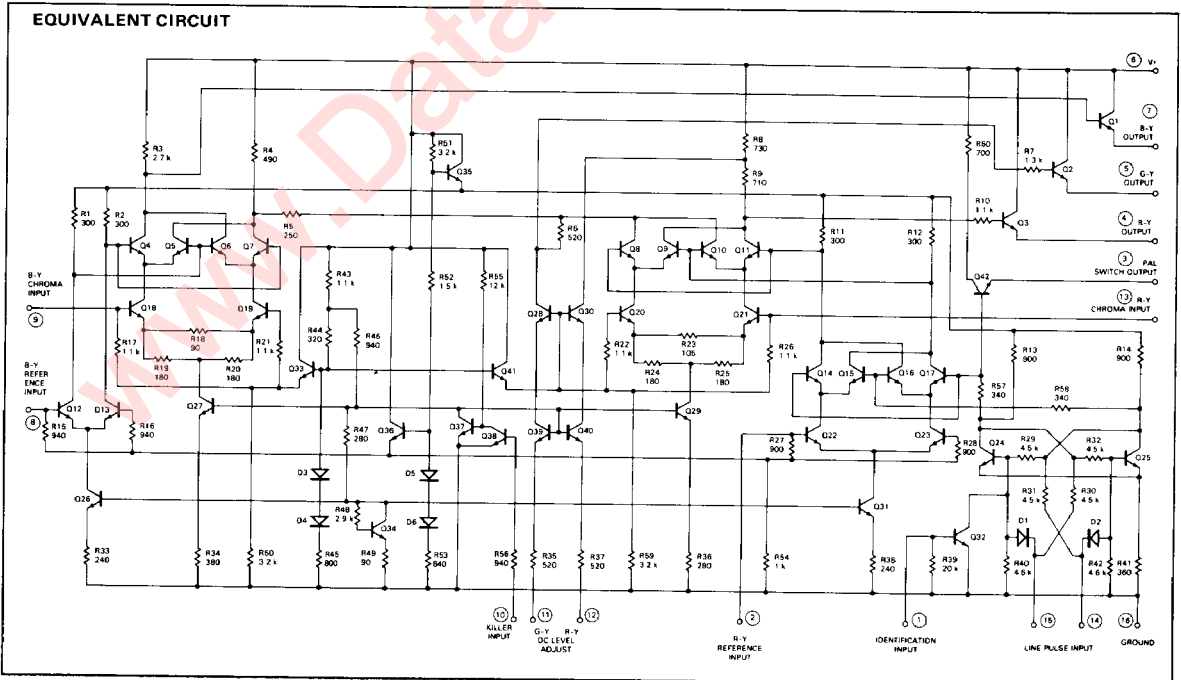
- **DOUBLE BALANCED SYNCHRONOUS DEMODULATOR**
- **INTERNAL DECODING MATRIX**
- **EMITTER FOLLOWER OUTPUTS**
- **INTERNAL PAL SWITCH**
- **INTERNAL COLOR KILLER**
- **PROVISION FOR OUTPUT DC LEVEL MATCHING**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 1)	13.2 V
Internal Power Dissipation (Note 1)	550 mW
Color Difference Output Currents	5.0 mA
Voltage on Identification Input	5.0 V
Current Into Identification Input	1.0 mA
Operating Temperature Range	-20°C to +60°C
Storage Temperature Range	-55°C to +125°C
Pin Temperature (Soldering, 10 s)	260°C



EQUIVALENT CIRCUIT



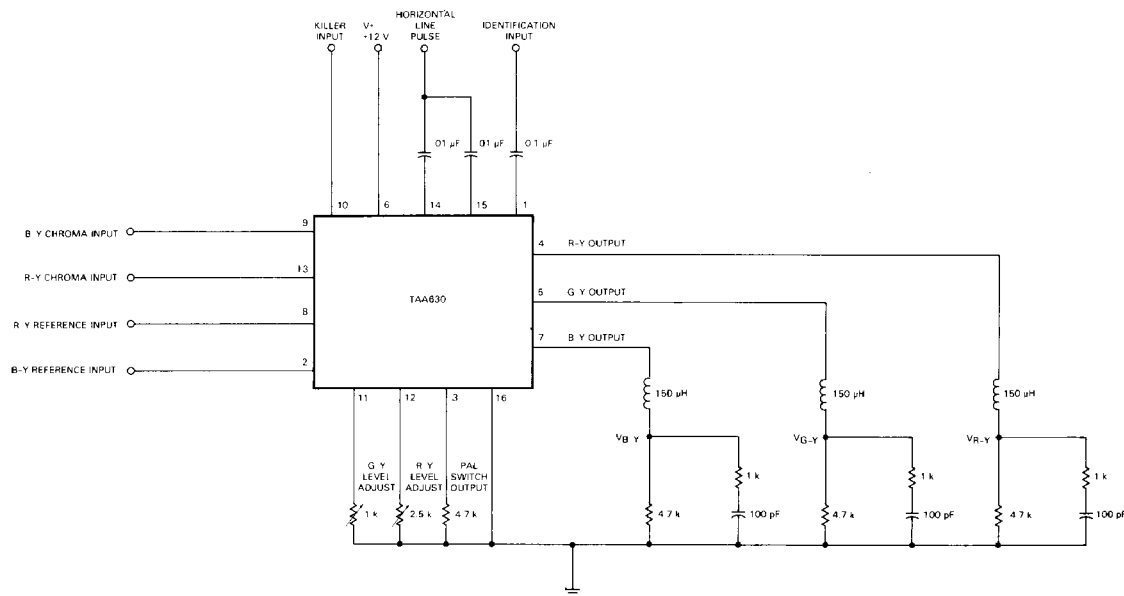
ELECTRICAL CHARACTERISTICS: $T_A = 25^\circ\text{C}$, $V_+ = 12\text{V}$, See Test Circuit, unless otherwise specified.

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current (I_G)			32		mA
Color Difference Gain R-Y Channel B-Y Channel/R-Y Channel G-Y Channel	$V_g = V_{13} = 50\text{ mV p-p}$ $f = 4.4\text{ MHz}$		7.0 1.78 Note 2		
Maximum Color Difference Output Voltage R-Y Output (V_4 p-p) B-Y Output (V_7 p-p) G-Y Output (V_5 p-p)	Notes 3, 4		3.2 4.0 1.8		V_{p-p} V_{p-p} V_{p-p}
Color Difference DC Output Voltage R-Y Output (V_4) B-Y Output (V_7) G-Y Output (V_5)	Note 5 Note 5		Adjustable to V_7 7.4 Adjustable to V_7		V
Input Resistance of Chroma Inputs (R_9, R_{13})	$V_g = V_{13} = 20\text{ mV RMS}$	800			Ω
Input Capacitance of Chroma Inputs (C_9, C_{13})	$f = 4.4\text{ MHz (sinusoidal)}$			10	pF
Output Resistance at Color Difference Terminals (R_4, R_5, R_7)				100	Ω
Input Resistance of Reference Inputs (R_2, R_8)	Note 7	660		1250	Ω
Peak-to-Peak PAL Switch Output Voltage (V_3 p-p)	Note 6		2.5		V_{p-p}
Activation Threshold Voltage (V_1)	Identification circuit is active	0.75			V
Activation Threshold Current (I_1)	Identification circuit is active	80			μA
Deactivation Threshold Voltage (V_1)	Identification circuit is inactive			0.4	V
DC Voltage at Color Killer Input (V_{10}): Color On Color Off		0.9		0.3	V V

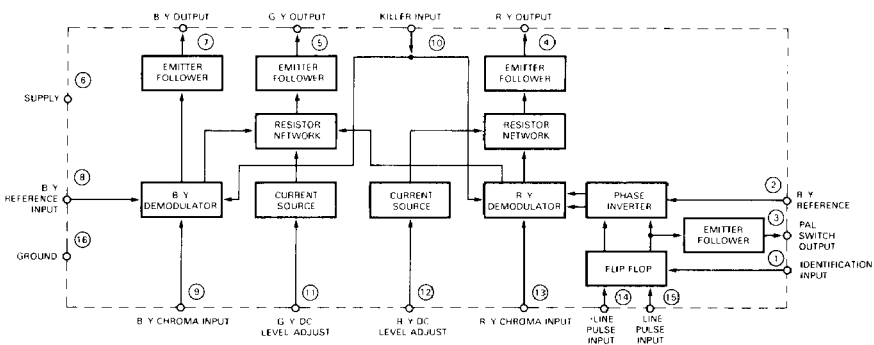
NOTES:

- 16 V is permissible during warm-up.
- G-Y Output is typically equal to -0.51 (R-Y) -0.19 (B-Y).
- Gain is equal to 0.7 of small signal gain.
- Reference input (V_2 p-p and V_8 p-p) range is 0.5 V to 2.0 V.
- To be adjusted with a variable voltage ($V \leq 1.2\text{ V}$) or with resistors connected between pin 11 and ground for G-Y and pin 12 and ground for R-Y.
- $f_{out} = 0.5 \times \text{Line Pulse Frequency}$, $V_{14} = V_{15} = -2.5\text{ V to } -5.0\text{ V (Peak)}$, PAL identification signal required, $V_1 = 2.0$ to 6.0 V p-p .
- $V_2 = V_8 = 400\text{ mV RMS}$, $f = 4.4\text{ MHz (sinusoidal)}$.

TEST CIRCUIT



BLOCK DIAGRAM



TYPICAL APPLICATION

