Features

- **Processor Bus Frequency Up to 66 MHz and 83.3 MHz**
- **64-bit Data Bus and 32-bit Address Bus**
- **L2 Cache Control for 256-Kbyte, 512-Kbyte, 1-Mbyte Sizes**
- **Provides Support for Either Asynchronous SRAM, Burst SRAM or Pipelined Burst SRAM**
- **Compliant with PCI Specification, Revision 2.1**
- **PCI Interface Operates at 20 to 33 MHz, 3.3V/5.0V-compatible**
- **IEEE 1149.1-compliant, JTAG Boundary-scan Interface**
- **P_D Max = 1.7 Watts (66 MHz), Full Operating Conditions**
- **Nap, Doze and Sleep Modes Reduce Power Consumption**
- **Fully Compliant with MIL-STD-883 Class Q or According to Atmel Standards**
- **Upscreenings Based on Atmel Standards**
- **Full Military Temperature Range (-55°C ≤ T_C ≤ +125°C)**
  - **Industrial Temperature Range (-40°C ≤ T_C ≤ +110°C)**
- **V_{CC} = 3.3V ± 5%**
- **Available in a 303-ball CBGA or a 303-ball CBGA with Solder Column Interposer (SCI) (CI-CGA) Package**

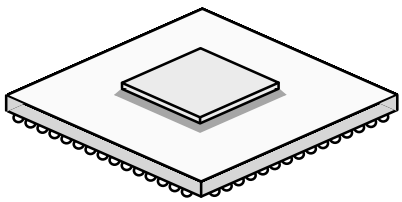
Description

The TSPC106 provides an integrated, high-bandwidth, high-performance, TTL-compatible interface between a 60x processor, a secondary (L2) cache or up to a total of four additional 60x processors, the PCI bus and main memory.

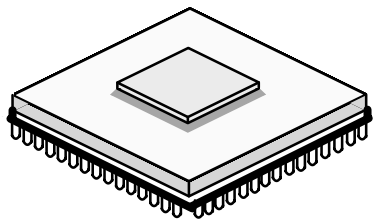
PCI support allows system designers to rapidly design systems using peripherals already designed for PCI.

The TSPC106 uses an advanced 3.3V CMOS-process technology and maintains full interface compatibility with TTL devices.

The TSPC106 integrates system testability and debugging features via JTAG boundary-scan capability.



G suffix
CBGA 303
Ceramic Ball Grid Array



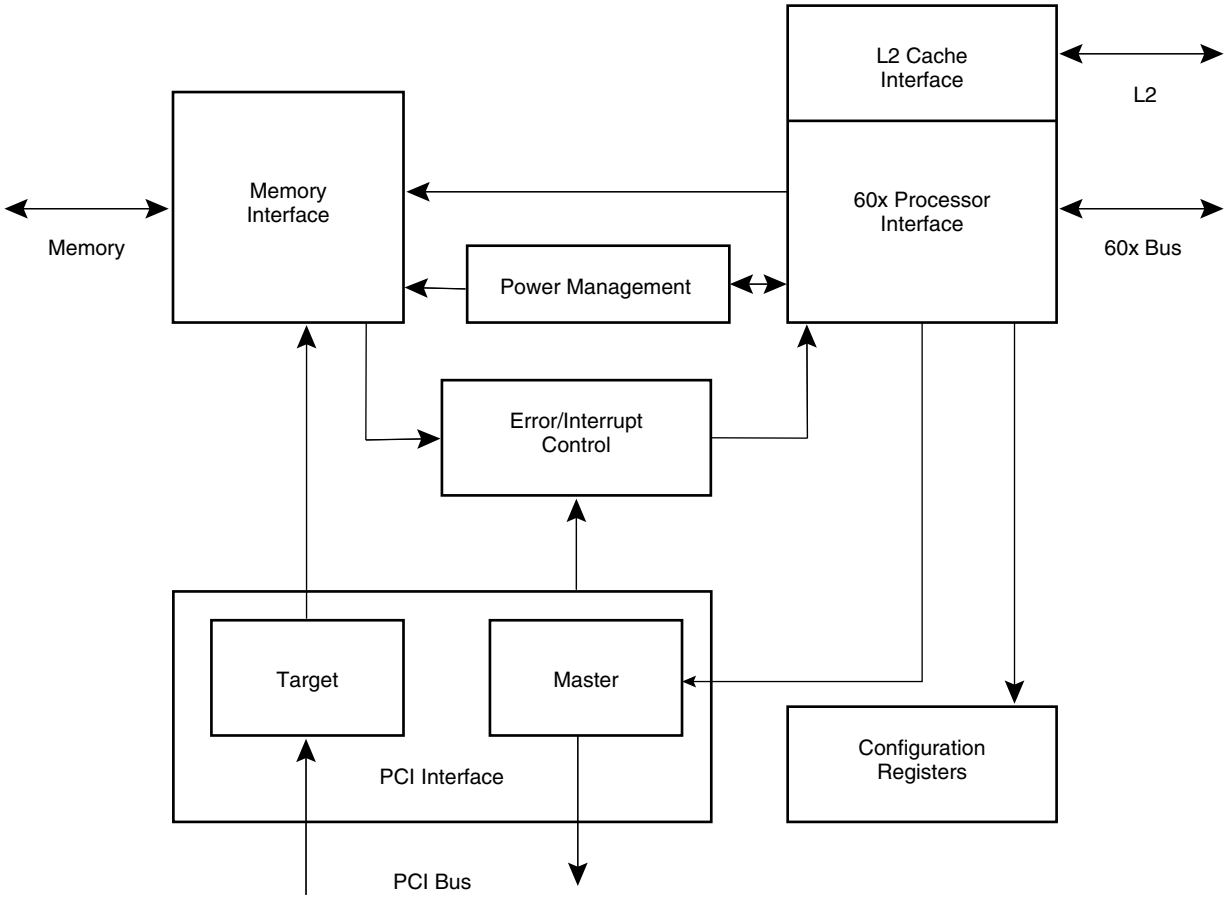
GS suffix
CI±CGA 303
Ceramic Ball Grid Array
with Solder Column Interposer (SCI)

PCI Bridge/ Memory Controller

TSPC106

Rev. 2102B–HIREL–02/02

Figure 1. TSPC106 Block Diagram



Functional Description

The TSPC106 provides a PowerPC® microprocessor CHRP-compliant bridge between the PowerPC microprocessor family and the PCI bus. CHRP is a set of specifications that defines a unified personal computer architecture and brings the combined advantages of the Power Macintosh® platform and the standard PC environment to both system vendors and users. PCI support allows system designers to rapidly design systems using peripherals already designed for PCI and other standard interfaces available in the personal computer hardware environment. These open specifications make it easier for system vendors to design computers capable of running multiple operating systems. The TSPC106 integrates secondary cache control and a high-performance memory controller. The TSPC106 uses an advanced 3.3V CMOS process technology and is fully compatible with TTL devices.

The TSPC106 supports a programmable interface to a variety of PowerPC microprocessors operating at select bus speeds. The 60x address bus is 32 bits wide; the data bus is 64 bits wide. The 60x processor interface of the TSPC106 uses a subset of the 60x bus protocol, supporting single-beat and burst data transfers. The address and data buses are decoupled to support pipelined transactions.

The TSPC106 provides support for the following configurations of 60x processors and L2 cache:

- Up to four 60x processors with no L2 cache
- A single 60x processor plus a direct-mapped, lookaside L2 cache using the internal L2 cache controller of the TSPC106
- Up to four 60x processors plus an externally controlled L2 cache (e.g., the Motorola MPC2604GA integrated L2 lookaside cache)

The memory interface controls processor and PCI interactions to main memory and is capable of supporting a variety of configurations using DRAM, EDO, or SDRAM and ROM or Flash ROM.

The PCI interface of the TSPC106 complies with the PCI local bus specification Revision 2.1 and follows the guidelines in the PCI System Design Guide Revision 1.0 for host bridge architecture. The PCI interface connects the processor and memory buses to the PCI bus to which I/O components are connected. The PCI bus uses a 32-bit multiplexed address/data bus plus various control and error signals.

The PCI interface of the TSPC106 functions as both a master and target device. As a master, the 106 supports read and write operations to the PCI memory space, the PCI I/O space and the PCI configuration space. The TSPC106 also supports PCI special-cycle and interrupt-acknowledge commands. As a target, the TSPC106 supports read and write operations to system memory.

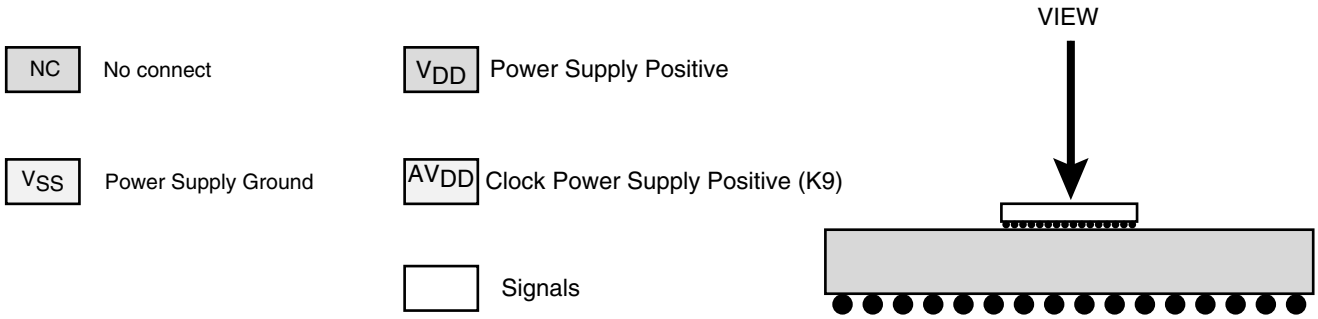
The TSPC106 provides hardware support for four levels of power reduction: doze, nap, sleep and suspend. The design of the TSPC106 is fully static, allowing internal logic states to be preserved during all power saving modes.

Pin Description

Figure 2. TSPC106 in 303-ball CBGA Package

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
W	DL26	DL28	DL30	DH31	DH29	DH27	DH25	DH23	DH21	DH19	DH17	DH15	DH13	DH11	DH9	DH7
V	DL24	DL27	DL29	DL31	DH30	DH28	DH26	DH24	DH20	DH18	DH16	DH14	DH12	DH10	DH8	DL22
U	MA1/ SDBA0/ AR9	DL23	DL25	DL14	PLL2	PLL0	DL12	DL10	DL4	DL2	DL0	$\overline{\text{DOE}}$/ $\overline{\text{DBGL2}}$	$\overline{\text{DBG1}}$	DH6	DL21	DL20
T	MA2/ SDMA2/ AR10	$\overline{\text{WE}}$	DH0	DL15	PLL3	PLL1	DL13	DL11	DL3	DL1	TV/ $\overline{\text{BR2}}$	BA0/ $\overline{\text{BR3}}$	$\overline{\text{HIT}}$	$\overline{\text{DIRTY\_IN}}$/ $\overline{\text{BR1}}$	DL19	$\overline{\text{DCS}}$/ $\overline{\text{BG3}}$
R	MA3/ SDMA3/ AR11	$\overline{\text{RCS0}}$	DH2	DH1	DL16	VSS	VDD	DL9	DL5	VSS	VDD	TWE/ $\overline{\text{BG2}}$	$\overline{\text{DIRTY\_OUT}}$/ $\overline{\text{BG1}}$	$\overline{\text{ADS}}$/ $\overline{\text{DALE}}$/ $\overline{\text{BRL2}}$	A0	TS
P	MA5/ SDMA5/ AR13	MA4/ SDMA4/ AR12	DH4	DH3	VSS	VDD	VSS	DL8	DL6	VDD	VSS	VDD	BA1/ $\overline{\text{BAA}}$ $\overline{\text{BGL2}}$	DWE0/ $\overline{\text{DBG2}}$	A1	XATS/ $\overline{\text{SDMA1}}$
N	MA6/ SDMA6/ AR14	MA0/ SDBA1/ SDMA0/ AR0	DL17	DH5	VDD	VSS	VDD	DL7	DH22	VSS	VDD	VSS	LBCLAIM	CI	A2	TA
M	MA8/ SDMA8/ AR16	MA7/ SDMA7/ AR15	RAS0/ $\overline{\text{CS0}}$	DL18	VSS	VDD	VSS	NC	NC	VDD	VSS	VDD	WT	GBL	A3	TT4
L	$\overline{\text{HRST}}$	MA9/ SDMA9/ AR17	QACK	$\overline{\text{RAS1}}$/ $\overline{\text{CS1}}$	VDD	CKO/ DWE2	RAS5/ $\overline{\text{CS5}}$	VSS	VDD	VSS	SYSCLK	$\overline{\text{DBG0}}$	$\overline{\text{TBST}}$	$\overline{\text{BR0}}$	A4	TT3
K	MA11/ SDMA11/ AR19	MA10/ SDMA10/ AR18	RAS3/ $\overline{\text{CS3}}$	RAS2/ $\overline{\text{CS2}}$	RAS4/ $\overline{\text{CS4}}$	RAS7/ $\overline{\text{CS7}}$	VDD	AVDD	VSS	VDD	A9	A8	A7	$\overline{\text{BG0}}$	A5	TT2
J	MA12/ SDMA12/ AR20	CAS0/ $\overline{\text{DQM0}}$	$\overline{\text{PPEN}}$	RCS1	RAS6/ $\overline{\text{CS6}}$	$\overline{\text{MCP}}$	DBGLB/ CKE	VSS	VDD	VSS	A11	A6	A13	A12	A10	TEA
H	$\overline{\text{QREQ}}$	$\overline{\text{CAS1}}$/ DQM1	$\overline{\text{SUS-}}$ $\overline{\text{PEND}}$	$\overline{\text{TRST}}$	VSS	$\overline{\text{DWE1}}$/ $\overline{\text{DBG3}}$	$\overline{\text{PIRQ}}$/ $\overline{\text{SDRAS}}$	NC	NC	VDD	VSS	VDD	A15	A14	A16	TT1
G	$\overline{\text{CAS2}}$/ DQM2	RTC	$\overline{\text{CAS4}}$/ DQM4	$\overline{\text{CAS5}}$/ DQM5	VDD	LSSD_ MODE	VDD	PAR	$\overline{\text{LOCK}}$	VSS	VDD	VSS	TSIZ1	TSIZ0	A17	TT0
F	BCTL0	$\overline{\text{BCTL1}}$	$\overline{\text{CAS6}}$/ DQM6	TCK	VSS	VDD	VSS	$\overline{\text{PERR}}$	$\overline{\text{DEV-}}$ $\overline{\text{SEL}}$	VDD	VSS	VDD	A21	TSIZ2	$\overline{\text{ARTRY}}$	A18
E	CAS3/ $\overline{\text{DQM3}}$	NMI	CAS7/ $\overline{\text{DQM7}}$	MDLE/ $\overline{\text{SDCAS}}$	TDO	VSS	VDD	$\overline{\text{SERR}}$	$\overline{\text{IRDY}}$	VSS	VDD	A31	A29	A22	A20	A19
D	PAR0/ AR1	PAR1/ AR2	TMS	$\overline{\text{FOE}}$	AD28	AD24	AD21	AD17	AD14	AD10	$\overline{\text{C/BE0}}$	AD4	AD0	A30	$\overline{\text{AACK}}$	A23
C	PAR2/ AR3	PAR3/ AR4	PAR5/ AR6	AD30	AD26	AD23	AD19	$\overline{\text{C/BE2}}$	$\overline{\text{C/BE1}}$	AD12	AD8	AD6	AD2	A27	A25	A24
B	PAR4/ AR5	PAR7/ AR8	AD1	TDI	AD7	AD11	AD15	$\overline{\text{TRDY}}$	AD18	AD22	AD25	AD29	$\overline{\text{REQ}}$	ISA_MASTER/ $\overline{\text{BERR}}$	A28	A26
A	PAR6/ AR7	$\overline{\text{GNT}}$	AD3	AD5	AD9	AD13	$\overline{\text{FRAME}}$	$\overline{\text{STOP}}$	AD16	AD20	$\overline{\text{C/BE3}}$	AD27	AD31	$\overline{\text{FLSHREQ}}$	$\overline{\text{MEMACK}}$	

Figure 3. Pin Assignments Shading Ley



Pinout

Table 1. TSPC106 Pinout in 303-ball CBGA Package

Signal Name	Pin Number	Active	I/O
60x Processor Interface Signals			
A[0:31]	R2, P2, N2, M2, L2, K2, J5, K4, K5, K6, J2, J6, J3, J4, H3, H4, H2, G2, F1, E1, E2, F4, E3, D1, C1, C2, B1, C3, B2, E4, D3, E5	High	I/O
AACK	D2	Low	I/O
ARTRY	F2	Low	I/O
BG0	K3	Low	Output
$\overline{\text{BG1}}$ (DIRTY_OUT)	R4	Low	Output
$\overline{\text{BG2}}$ (TWE)	R5	Low	Output
$\overline{\text{BG3}}$ (DCS)	T1	Low	Output
BR0	L3	Low	Input
$\overline{\text{BR1}}$ (DIRTY_IN)	T3	Low	Input
$\overline{\text{BR2}}$ (TV)	T6	Low	Input
$\overline{\text{BR3}}$ (BA0)	T5	Low	Input
CI	N3	Low	I/O
DBG0	L5	Low	Output
$\overline{\text{DBG1}}$ (TOE)	U4	Low	Output
$\overline{\text{DBG2}}$ (DWE0)	P3	Low	Output
$\overline{\text{DBG3}}$ (DWE1)	H11	Low	Output
$\overline{\text{DBGLB}}$ (CKE)	J10	Low	Output
DH[0:31]	T14, R13, R14, P13, P14, N13, U3, W1, V2, W2, V3, W3, V4, W4, V5, W5, V6, W6, V7, W7, V8, W8, N8, W9, V9, W10, V10, W11, V11, W12, V12, W13	High	I/O
DL[0:31]	U6, T7, U7, T8, U8, R8, P8, N9, P9, R9, U9, T9, U10, T10, U13, T13, R12, N14, M13, T2, U1, U2, V1, U15, V16, U14, W16, V15, W15, V14, W14, V13	High	I/O
GBL	M3	Low	I/O
LBCLAIM	N4	Low	Input

Table 1. TSPC106 Pinout in 303-ball CBGA Package (Continued)

Signal Name	Pin Number	Active	I/O
MCP	J11	Low	Output
TA	N1	Low	I/O
TBST	L4	Low	I/O
TEA	J1	Low	Output
TS	R1	Low	I/O
TSIZ[0:2]	G3, G4, F3	High	I/O
TT[0:4]	G1, H1, K1, L1, M1	High	I/O
WT	M4	Low	I/O
XATS (SDMA1)	P1	Low	Input
L2 Cache Interface Signals			
ADS/DALE/BRL2	R3	Low	Output
BA0 (BR3)	T5	Low	Output
BA1/BAA/BGL2	P4	Low	Output
$\overline{\text{DBGL2}}$/DOE	U5	Low	Output
$\overline{\text{DCS}}$ (BG3)	T1	Low	Output
$\overline{\text{DIRTY\_IN}}$ (BR1)	T3	Low	Input
$\overline{\text{DIRTY\_OUT}}$ (BG1)	R4	Low	Output
$\overline{\text{DWE0}}$ (DBG2)	P3	Low	Output
$\overline{\text{DWE1}}$ (DBG3)	H11	Low	Output
$\overline{\text{DWE2}}$ (CKO)	L11	Low	Output
HIT	T4	Low	Input
$\overline{\text{TOE}}$ (DBG1)	U4	Low	Output
TV (BR2)	T6	High	I/O
TWE (BG2)	R5	Low	Output
Memory Interface Signals			
BCTL [0:1]	F16, F15	Low	Output
BERR ($\overline{\text{ISA\_MASTER}}$)	B3	Low	Input
$\overline{\text{CAS}}$/DQM[0:7]	J15, H15, G16, E16, G14, G13, F14, E14	Low	Output
CKE/$\overline{\text{DBGLB}}$	J10	High	Output
FOE	D13	Low	Output
MA0/SDBA1/SDMA0/AR0	N15	High	Output
SDMA1 (XATS)	P1	High	Output
MA1/SDBA0/AR9	U16	High	Output
MA[2:12]/SDMA[2:12]/AR[10:20]	T16, R16, P15, P16, N16, M15, M16, L15, K15, K16, J16	High	Output
$\overline{\text{MDLE}}$/SDCAS	E13	Low	Output

Table 1. TSPC106 Pinout in 303-ball CBGA Package (Continued)

Signal Name	Pin Number	Active	I/O
PAR[0:7]/AR[1:8]	D16, D15, C16, C15, B16, C14, A16, B15	High	I/O
PPEN	J14	Low	Output
$\overline{RAS}$/$\overline{CS}$[0:7]	M14, L13, K13, K14, K12, L10, J12, K11	Low	Output
RCS0	R15	Low	I/O
RCS1	J13	Low	Output
RTC	G15	High	Input
$\overline{SDRAS}$ (PIRQ)	H10	Low	Output
WE	T15	Low	Output
PCI Interface Signals[2]			
AD[31:0][2]	A4, C13, B5, D12, A5, C12, B6, D11, C11, B7, D10, A7, C10, B8, D9, A8, B10, D8, A11, C7, B11, D7, A12, C6, B12, C5, A13, D5, A14, C4, B14, D4	High	I/O
$\overline{C/BE}$[3:0][2]	A6, C9, C8, D6	Low	I/O
DEVSEL	F8	Low	I/O
FLSHREQ	A3	Low	Input
FRAME	A10	Low	I/O
GNT	A15	Low	Input
IRDY	E8	Low	I/O
$\overline{ISA\_MASTER}$ (BERR)	B3	Low	Input
LOCK	G8	Low	Input
MEMACK	A2	Low	Output
PAR	G9	High	I/O
PERR	F9	Low	I/O
PIRQ (SDRAS)	H10	Low	Output
REQ	B4	Low	Output
SERR	E9	Low	I/O
STOP	A9	Low	I/O
TRDY	B9	Low	I/O
Interrupt, Clock and Power Management Signals			
CK0 ($\overline{DWE2}$)	L11	High	Output
HRST	L16	Low	Input
NMI	E15	High	Input
QACK	L14	Low	Output
QREQ	H16	Low	Input
SYSCLK	L6	Clock	Input
SUSPEND	H14	Low	Input
Test/Configuration Signals			

Table 1. TSPC106 Pinout in 303-ball CBGA Package (Continued)

Signal Name	Pin Number	Active	I/O
PLL[0:3]	U11, T11, U12, T12	High	Input
TCK	F13	Clock	Input
TDI	B13	High	Input
TDO	E12	High	Output
TMS	D14	High	Input
TRST	H13	Low	Input
Power and Ground Signals			
AV_{DD}	K9	High	Clock
LSSD_MODE(3)	G11	Low	Input
V_{DD}	E10, E6, F11, F5, F7, G10, G12, G6, H5, H7, K10, K7, L12, M11, M5, M7, N10, N12, N6, P11, P5, P7, R10, R6, J8, L8	High	Power
V_{SS}	E11, E7, F10, F12, F6, G5, G7, H12, H6, J7, L7, M10, M12, M6, N11, N5, N7, P10, P12, P6, R11, R7, K8, J9, L9	Low	Ground
NC	H8, H9, M8, M9	–	–

Notes: 1. Some signals have dual functions and are shown more than once in this table.
2. All PCI signals are in little-endian bit order.
3. This test signal is for factory use only. It must be pulled up to V_{DD} for normal device operation.

Signal Description

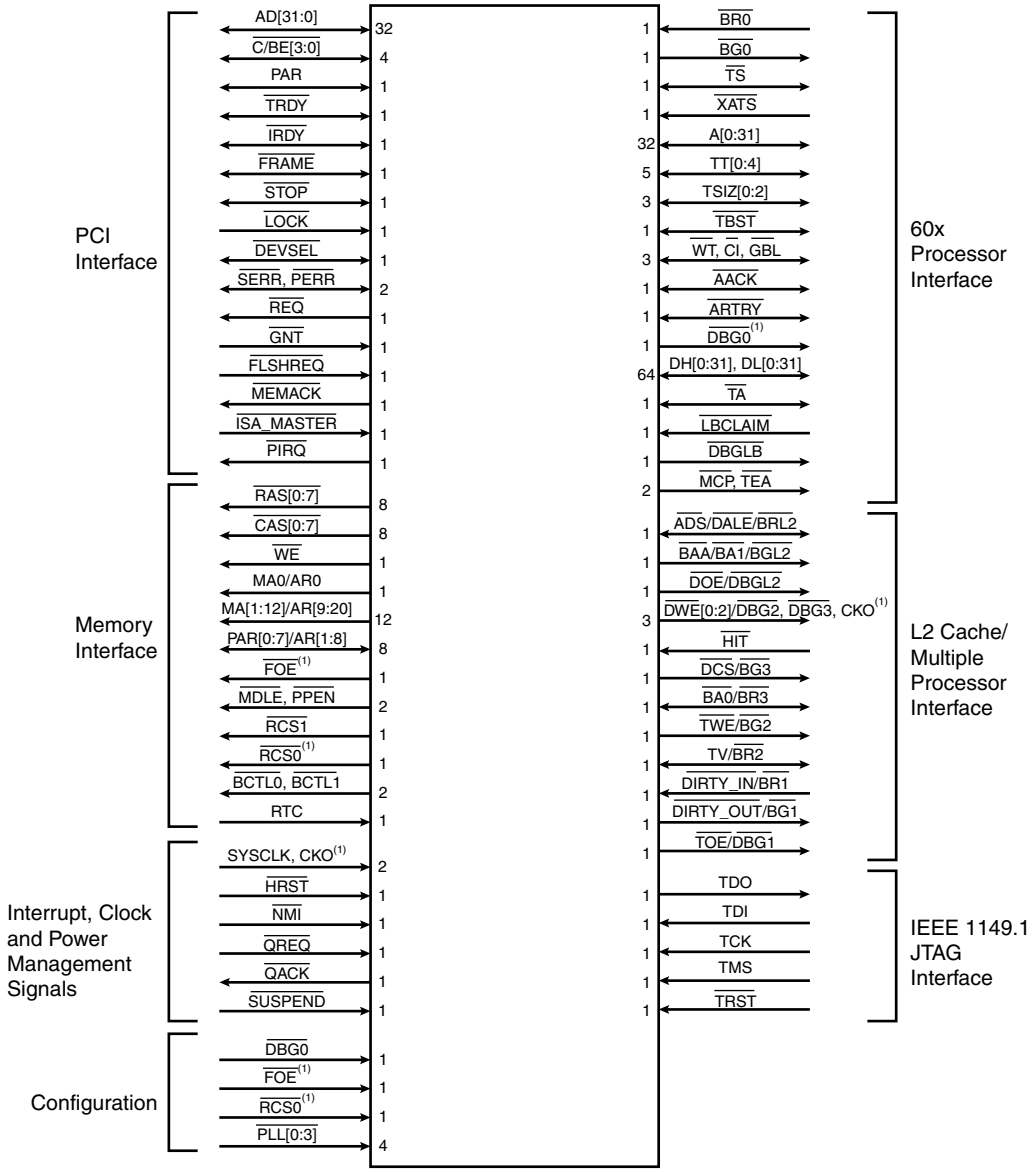
The signals on the TSPC106 are grouped as follows:

- 60x processor interface signals
- L2 cache/multiple processor interface signals
- Memory interface signals
- PCI interface signals
- Interrupt, clock and power management signals
- IEEE 1149.1 interface signals
- Configuration signals

Note: A bar over a signal name indicates that the signal is active low, for example, address retry ($\overline{\text{ARTRY}}$) and transfer start ($\overline{\text{TS}}$). Active-low signals are referred to as asserted (active) when they are low and negated when they are high. Signals that are not active low such as tag valid (TV) and nonmaskable interrupt (NMI) are referred to as asserted when they are high and negated when they are low.

Note: For multiple-function signals, outlined signal names refer to the alternate function(s) of the signal being described. For example, the L2 controller signal, (tag output enable $\overline{\text{TOE}}$), has the alternate function data bus grant 1 ($\overline{\text{DBG1}}$) when the TSPC106 is configured for a second 60x processor.

Figure 4. Symbol



Note: Some signals have dual functions and are shown more than once in this figure.

60x Processor Interface Signals

Table 2. 60x Processor Interface Signals

Signal	Signal Name	Number of Pins	I/O	Signal Description
A[0:31]	Address bus	32	O	Specifies the physical address for 60x bus snooping.
			I	Specifies the physical address of the bus transaction. For burst reads, the address is aligned to the critical double-word address that missed in the instruction or data cache. For burst writes, the address is aligned to the double-word address of the cache line being pushed from the data cache.
AACK	Address acknowledge	1	O	Indicates that the address tenure of a transaction is terminated. On the cycle following the assertion of $\overline{\text{AACK}}$, the bus master releases the address-tenure-related signals to a high impedance state and samples $\overline{\text{ARTRY}}$.
			I	Indicates that an externally-controlled L2 cache is terminating the address tenure. On the cycle following the assertion of $\overline{\text{AACK}}$, the bus master releases the address-tenure-related signals to a high impedance state and samples $\overline{\text{ARTRY}}$.
ARTRY	Address retry	1	O	Indicates that the initiating 60x bus master must retry the current address tenure.
			I	During a snoop operation, indicates that the 60x either requires the current address tenure to be retried due to a pipeline collision or needs to perform a snoop copy-back operation. During normal 60x bus cycles in a multiprocessor system, indicates that the other 60x or external L2 controller requires the address tenure to be retried.
BG0	Bus grant 0	1	O	Indicates that the primary 60x may, with the proper qualification, begin a bus transaction and assume mastership of the address bus.
BR0	Bus request 0	1	I	Indicates that the primary 60x requires the bus for a transaction.
CI	Cache inhibit	1	I/O	Indicates that an access is caching-inhibited.
DBG0	Data bus grant 0	1	O	Indicates that the 60x may, with the proper qualification, assume mastership of the data bus.
DBGLB	Local bus slave data bus grant	1	O	Indicates that the 60x processor is prepared to accept data and the local bus slave should drive the data bus.

Table 2. 60x Processor Interface Signals (Continued)

<table>
<tr><th>Signal</th><th>Signal Name</th><th>Number of Pins</th><th>I/O</th><th>Signal Description</th></tr>
<tr><td>DH[0:31], DL[0:31]</td><td>Data bus</td><td>64</td><td></td><td>The data bus is comprised of two halves - data bus high (DH[0:31]) and data bus low (DL[0:31]). The data bus has the following byte lane assignments:
<table>
<tr><th>Data Byte</th><th>Byte Lane</th></tr>
<tr><td>DH[0:7]</td><td>0</td></tr>
<tr><td>DH[8:15]</td><td>1</td></tr>
<tr><td>DH[16:23]</td><td>2</td></tr>
<tr><td>DH[24:31]</td><td>3</td></tr>
<tr><td>DL[0:7]</td><td>4</td></tr>
<tr><td>DL[8:15]</td><td>5</td></tr>
<tr><td>DL[16:23]</td><td>6</td></tr>
<tr><td>DL[24:31]</td><td>7</td></tr>
</table></td></tr>
<tr><td></td><td></td><td></td><td>O</td><td>Represents the value of data being driven by the TSPC106.</td></tr>
<tr><td></td><td></td><td></td><td>I</td><td>Represents the state of data being driven by a 60x processor, the local bus slave, the L2 cache or the memory subsystem.</td></tr>
<tr><td>GBL</td><td>Global</td><td>1</td><td>I/O</td><td>Indicates that an access is global and hardware needs to enforce coherency.</td></tr>
<tr><td>LBCLAIM</td><td>Local bus slave cycle claim</td><td>1</td><td>I</td><td>Indicates that the local bus slave claims the transaction and is responsible for driving $\overline{TA}$ during the data tenure.</td></tr>
<tr><td>MCP</td><td>Machine check</td><td>1</td><td>O</td><td>Indicates that the TSPC106 detected a catastrophic error and the 60x processor should initiate a machine check exception.</td></tr>
<tr><td>TA</td><td>Transfer acknowledge</td><td>1</td><td>O</td><td>Indicates that the data has been latched for a write operation or that the data is valid for a read operation, thus terminating the current data beat. If it is the last (or only) data beat, this also terminates the data tenure.</td></tr>
<tr><td></td><td></td><td></td><td>I</td><td>Indicates that the external L2 cache or local bus slave has latched data for a write operation or is indicating the data is valid for a read operation. If it is the last (or only) data beat, then the data tenure is terminated.</td></tr>
<tr><td>TBST</td><td>Transfer burst</td><td>1</td><td>O</td><td>Indicates that a burst transfer is in progress.</td></tr>
<tr><td></td><td></td><td></td><td>I</td><td>Indicates that a burst transfer is in progress.</td></tr>
<tr><td>TEA</td><td>Transfer error acknowledge</td><td>1</td><td>O</td><td>Indicates that a bus error has occurred. Assertion of $\overline{TEA}$ terminates the transaction in progress. An unsupported memory transaction, such as a direct-store access or a graphics read or write, causes the assertion of $\overline{TEA}$ (provided $\overline{TEA}$ is enabled).</td></tr>
<tr><td>TS</td><td>Transfer start</td><td>1</td><td>O</td><td>Indicates that the TSPC106 has started a bus transaction and that the address and transfer attribute signals are valid. Note that the TSPC106 only initiates a transaction to broadcast the address of a PCI access to memory for snooping purposes.</td></tr>
<tr><td></td><td></td><td></td><td>I</td><td>Indicates that a 60x bus master has begun a transaction and that the address and transfer attribute signals are valid.</td></tr>
</table>

Table 2. 60x Processor Interface Signals (Continued)

Signal	Signal Name	Number of Pins	I/O	Signal Description
TSIZ[0:2]	Transfer size	3	O	Specifies the data transfer size for the 60x bus transaction.
			I	Specifies the data transfer size for the 60x bus transaction.
TT[0:4]	Transfer type	5	O	Specifies the type of 60x bus transfer in progress.
			I	Specifies the type of 60x bus transfer in progress.
WT	Write-through	1	I/O	Indicates that an access is write-through.
XATS	Extended address transfer start	1	I	Indicates that the 60x has started a direct-store access (using the extended transfer protocol). Since direct-store accesses are not supported by the TSPC106, the TSPC106 automatically asserts when $\overline{\text{TEA}}$ and $\overline{\text{XATS}}$ are asserted (provided $\overline{\text{TEA}}$ is enabled).

L2 Cache/Multiple Processor Interface Signals

The TSPC106 provides support for either an internal L2 cache controller or an external L2 cache controller and/or additional 60x processors.

Internal L2 Controller Signals

Table 3 lists the interface signals for the internal L2 controller and provides a brief description of their functions. The internal L2 controller supports either burst SRAMs or asynchronous SRAMs. Some of the signals perform different functions depending on the SRAM configuration.

Table 3. Internal L2 Controller Signals

Signal	Signal Name	Number of Pins	I/O	Signal Description
$\overline{\text{ADS}}$ $\overline{\text{DALE}}$ $\overline{\text{BRL2}}$	Address strobe	1	O	For a burst SRAM configuration, indicates to the burst SRAM that the address is valid to be latched.
BA0 $\overline{\text{BR3}}$	Burst address 0	1	I/O	For an asynchronous SRAM configuration, indicates bit 0 of the burst address counter.
BA1 $\overline{\text{BAA}}$ $\overline{\text{BGL2}}$	Burst address 1	1	O	For an asynchronous SRAM configuration, indicates bit 1 of the burst address counter.
$\overline{\text{BAA}}$ BA1 $\overline{\text{BGL2}}$	Bus address advance	1	O	For a burst SRAM configuration, indicates that the burst RAMs should increment their internal addresses.
DALE $\overline{\text{ADS}}$ $\overline{\text{BRL2}}$	Data address latch enable	1	O	For an asynchronous SRAM configuration, indicates that the external address latch should latch the current 60x bus address.
DCS BG3	Data RAM chip select	1	O	Enables the L2 data RAMs for a read or write operation.
DIRTY_IN BR1	Dirty in	1	I	Indicates that the selected L2 cache line is modified. The polarity of DIRTY_IN is programmable.
DIRTY_OUT BG1	Dirty out	1	O	Indicates that the L2 cache line should be marked as modified. The polarity of DIRTY_OUT is programmable.

Table 3. Internal L2 Controller Signals (Continued)

Signal	Signal Name	Number of Pins	I/O	Signal Description
DOE DBGL2	Data RAM output enable	1	O	Indicates that the L2 data RAMs should drive the data bus.
DWE[0:2] DBG2 DBG3	Data RAM write enable	3	O	Indicates that a write to the L2 data RAMs is in progress. Multiple pins are provided to reduce loading.
$\overline{\text{HIT}}$	Hit	1	I	Indicates that the L2 cache has detected a hit. The polarity of HIT is programmable.
TOE DBG1	Tag output enable	1	O	Indicates that the tag RAM should drive the L2 tag address onto the address bus.
TV $\overline{\text{BR2}}$	Tag valid	1	I/O	Indicates that the current L2 cache line should be marked valid. The polarity of TV is programmable.
TWE BG2	Tag write enable	1	O	Indicates that the L2 tag address, valid, and dirty bits should be updated.

External L2 Controller Signals When an external L2 cache controller is used instead of the internal L2 cache controller, four signals change their functions.

Table 4. External L2 Controller Signals

Signal	Signal Name	Number of Pins	I/O	Signal Description
$\overline{\text{BGL2}}$ BA1 $\overline{\text{BAA}}$	External L2 bus grant	1	O	Indicates that the external L2 controller has been granted mastership of the 60x address bus.
$\overline{\text{BRL2}}$ $\overline{\text{ADS}}$ DALE	External L2 bus request	1	I	Indicates that the external L2 controller requires mastership of the 60x bus for a transaction.
DBGL2 DOE	External L2 data bus grant	1	O	Indicates that the external L2 controller has been granted mastership of the 60x data bus.
$\overline{\text{HIT}}$	External L2 hit	1	I	Indicates that the current transaction is claimed by the external L2 controller. The external L2 controller will assert AACK and TA for the transaction.

Multiple Processor Signals

When a system implementation uses more than one 60x processor, nine of the internal L2 cache controller signals change their functions.

Note that in a multi-processor system, with the exception of the bus grant, bus request and data bus grant signals, all of the 60x processor interface signals are shared by all 60x processors.

Table 5. Multiple Processor Signals

Signal	Signal Name	Number of Pins	I/O	Signal Description
BG1 DIRTY_OUT	Bus grant 1	1	O	Indicates that processor 1 may, with the proper qualification, begin a 60x bus transaction and assume mastership of the address bus.
BG2 TWE	Bus grant 2	1	O	Indicates that processor 2 may, with the proper qualification, begin a 60x bus transaction and assume mastership of the address bus.
BG3 DCS	Bus grant 3	1	O	Indicates that processor 3 may, with the proper qualification, begin a 60x bus transaction and assume mastership of the address bus.
BR1 DIRTY_IN	Bus request 1	1	I	Indicates that processor 1 requires mastership of the 60x bus for a transaction.
$\overline{\text{BR2}}$ TV	Bus request 2	1	I	Indicates that processor 2 requires mastership of the 60x bus for a transaction.
BR3 BA0	Bus request 3	1	I	Indicates that processor 3 requires mastership of the 60x bus for a transaction.
DBG1 TOE	Data bus grant 1	1	O	Indicates that processor 1 may, with the proper qualification, assume mastership of the 60x data bus.
DBG2 DWE0	Data bus grant 2	1	O	Indicates that processor 2 may, with the proper qualification, assume mastership of the 60x data bus.
DBG3 DWE1	Data bus grant 3	1	O	Indicates that processor 3 may, with the proper qualification, assume mastership of the 60x data bus.

Memory Interface Signals

Table 6 lists the memory interface signals and provides a brief description of their functions. The memory interface supports either standard DRAMs or EDO DRAMs, and either standard ROMs or Flash ROMs. Some of the memory interface signals perform different functions depending on the RAM and ROM configurations.

Table 6. Memory Interface Signals

Signal	Signal Name	Number of Pins	I/O	Signal Description
AR0 MA0	ROM address 0	8	O	Represents address bit 0 of the 8-bit ROM/Flash. Note that AR0 is only supported for ROM bank 0 when configured for an 8-bit ROM/Flash data bus width. The extra address bit allows for up to 2 Mbytes of ROM when using the 8-bit wide data path. Bits 1 - 8 of the ROM address are provided by AR[1:8] and bits 9 - 20 of the ROM address are provided by AR[9:20].
AR[1:8] PAR[0:7]	ROM address 1 - 8	8	O	Represents bits 1 - 8 of the ROM/Flash address. The other ROM address bits are provided by AR0 and AR[9:20].
AR[9:20] MA[1:12]	ROM address 9 - 20	12	O	Represents bits 9 - 20 of the ROM/Flash address (the 12 lowest order bits, with AR20 as the least significant bit (lsb)). Bits 0 - 8 of the ROM address are provided by AR0 and AR[1:8].
$\overline{\text{BCTL}}$[0:1]	Buffer control 0 - 1	2	O	Used to control external data bus buffers (directional control and high-impedance state) between the 60x bus and memory. Note that external data buffers may be optional for lightly loaded data buses, but buffers are required whenever an L2 cache and ROM/Flash (on the 60x/memory bus) are both in the system or when ECC is used.
$\overline{\text{CAS}}$[0:7]	Column address strobe 0 - 7	8	O	Indicates a memory column address is valid and selects one of the columns in the row. $\overline{\text{CAS0}}$ connects to the most significant byte select. $\overline{\text{CAS7}}$ connects to the least significant byte select.
$\overline{\text{FOE}}$	Flash output enable	1	O	Enables Flash output for the current read access.
MA0 MA[1:12] AR0 AR[9:20]	Memory address 0 - 12	13	O	Represents the row/column multiplexed physical address for DRAMs or EDOs (MA0 is the most significant address bit; MA12 is the least significant address bit). Note that MA0 also functions as the ROM address signal AR0 and MA[1:12] function as the ROM address signals AR[9:20].
$\overline{\text{MDLE}}$	Memory data latch enable	1	O	Enables the external, latched data buffer for read operations, if such a buffer is used in the system.
PAR[0:7] AR[1:8]	Data parity/ECC	8	O	Represents the byte parity or ECC being written to memory (PAR0 is the most significant bit).
			I	Represents the byte parity or ECC being read from memory (PAR0 is the most significant bit).
$\overline{\text{PPEN}}$	Parity path read enable	1	O	Enables external parity/ECC bus buffer or latch for memory read operations.
$\overline{\text{RAS}}$[0:7]	Row address strobe 0 - 7	8	O	Indicates a memory row address is valid and selects one of the rows in the bank.
$\overline{\text{RCS0}}$	ROM/Flash bank 0 select	1	O	Selects ROM/Flash bank 0 for a read access or Flash bank 0 for a read or write access.
$\overline{\text{RCS1}}$	ROM/Flash bank 1 select	1	O	Selects ROM/Flash bank 1 for a read access or Flash bank 1 for a read or write access.
RTC	Real-time clock	1	I	External clock source for the memory refresh logic when the TSPC106 is in the suspend power-saving mode.
$\overline{\text{WE}}$	Write enable	1	O	Enables writing to DRAM, EDO or Flash.

PCI Interface Signals

Table 7 lists the PCI interface signals and provides a brief description of their functions. Note that the bits in Table 7 are referenced in little-endian format.

The PCI specification defines a sideband signal as any signal, not part of the PCI specification, that connects two or more PCI-compliant agent, and has meaning only to those agents. The TSPC106 implements four PCI sideband signals -$\overline{\text{FLSHREQ}}$, $\overline{\text{ISA\_MASTER}}$, $\overline{\text{MEMACK}}$ and $\overline{\text{PIRQ}}$.

Table 7. PCI Interface Signals

Signal	Signal Name	Number of Pins	I/O	Signal Description
AD[31:0]	Address/data	32	I/O	Represents the physical address during the address phase of a transaction. During the data phase(s) of a PCI transaction, AD[31:0] contain data. AD[7:0] define the least significant byte and AD[31:24] the most significant byte.
$\overline{\text{C/BE}}$[3:0]	Command/byte enable	4	O	During the address phase, $\overline{\text{C/BE}}$[3:0] define the PCI bus command. During the data phase, $\overline{\text{C/BE}}$[3:0] are used as byte enables. Byte enables determine which byte lanes carry meaningful data. $\overline{\text{C/BE0}}$ applies to the least significant byte.
			I	During the address phase, $\overline{\text{C/BE}}$[3:0] indicates the PCI bus command that another master is sending. During the data phase $\overline{\text{C/BE}}$[3:0] indicate which byte lanes are valid.
$\overline{\text{DEVSEL}}$	Device select	1	O	Indicates that the TSPC106 has decoded the address and is the target of the current access.
			I	Indicates that some PCI agent (other than the TSPC106) has decoded its address as the target of the current access.
$\overline{\text{FLSHREQ}}$	Flush request	1	I	Indicates that a device needs to have the TSPC106 flush all of its current operations.
$\overline{\text{FRAME}}$	Frame	1	O	Indicates that the TSPC106, acting as a PCI master, is initiating a bus transaction.
			I	Indicates that another PCI master is initiating a bus transaction.
$\overline{\text{GNT}}$	PCI bus grant	1	I	Indicates that the TSPC106 has been granted control of the PCI bus. Note that $\overline{\text{GNT}}$ is a point-to-point signal. Every master has its own $\overline{\text{GNT}}$ SIGNAL.
$\overline{\text{IRDY}}$	Initializer ready	1	O	Indicates that the TSPC106, acting as a PCI master, can complete the current data phase of a PCI transaction. During a write, the TSPC106 asserts $\overline{\text{IRDY}}$ to indicate that valid data is present on AD[31:0]. During a read, the TSPC106 asserts $\overline{\text{IRDY}}$ to indicate that it is prepared to accept data.
			I	Indicates another PCI master is able to complete the current data phase of the transaction.
ISA_ MASTER	ISA master	1	I	Indicates that an ISA master is requesting system memory.
$\overline{\text{LOCK}}$	Lock	1	I	Indicates that a master is requesting exclusive access to memory, which may require multiple transactions to complete.
$\overline{\text{MEMACK}}$	Memory acknowledge	1	O	Indicates that the TSPC106 has flushed all of its current operations and has blocked all 60x transfers except snoop copy-back operations. The TSPC106 asserts $\overline{\text{MEMACK}}$ in response to assertion of $\overline{\text{FLSHREQ}}$ after the flush is complete.

Table 7. PCI Interface Signals

Signal	Signal Name	Number of Pins	I/O	Signal Description
PAR	Parity	1	O	Asserted indicates odd parity across the AD[31:0] and $\overline{C/BE}$[3:0] signals during address and data phases. Negated indicates even parity.
			I	Asserted indicates odd parity driven by another PCI master or the PCI target during read data phases. Negated indicates even parity.
$\overline{PERR}$	Parity error	1	O	Indicates that another PCI agent detected a data parity error.
			I	Indicates that another PCI agent detected a data parity error.
$\overline{PIRQ}$	Modified memory interrupt request	1	O	In emulation mode (see “Address Maps” on page 19), indicates that a PCI write has occurred to system memory that has not been recorded by software.
$\overline{REQ}$	PCI bus request	1	O	Indicates that the TSPC106 is requesting control of the PCI bus to perform a transaction. Note that $\overline{REQ}$ is a point-to-point signal. Every master has its own $\overline{REQ}$ signal.
$\overline{SERR}$	System error	1	O	Indicates that an address parity error or some other system error (where the result will be a catastrophic error) was detected.
			I	Indicates that another target has detected a catastrophic error.
$\overline{STOP}$	Stop	1	O	Indicates that the TSPC106, acting as the PCI target, is requesting that the PCI bus master stop the current transaction.
			I	Indicates that some other PCI agent is requesting that the PCI initiator stop the current transaction.
$\overline{TRDY}$	Target ready	1	O	Indicates that the TSPC106, acting as a PCI target, can complete the current data phase of a PCI transaction. During a read, the TSPC106 asserts $\overline{TRDY}$ to indicate that valid data is present on AD[31:0]. During a write, the TSPC106 asserts $\overline{TRDY}$ to indicate that it is prepared to accept data.
			I	Indicates that another PCI target is able to complete the current data phase of a transaction.

Interrupt, Clock and Power Management Signals

The TSPC106 coordinates interrupt, clocking, and power management signals across the memory bus, the PCI bus and the 60x processor bus.

Table 8. Interrupt, Clock and Power Management Signals

Signal	Signal Name	Number of Pins	I/O	Signal Description
CKO $\overline{\text{DWE2}}$	Test clock	1	O	CKO provides a means to monitor the internal PLL output or the bus clock frequency. The CKO clock should be used for testing purposes only. It is not intended as a reference clock signal.
$\overline{\text{HRST}}$	Hard reset	1	I	Initiates a complete hard reset of the TSPC106. During assertion, all bi-directional signals are released to a high-impedance state and all output signals are either in a high impedance or inactive state.
NMI	Nonmaskable interrupt	1	I	Indicates that an external device (typically an interrupt controller) has detected a catastrophic error. In response, the TSPC106 asserts $\overline{\text{MCP}}$ on the 60x processor bus.
$\overline{\text{QACK}}$	Quiesce acknowledge	1	O	Indicates that the TSPC106 is in a low-power state. All bus activity that requires snooping has terminated and the 60x processor may enter a low-power state.
$\overline{\text{QREQ}}$	Quiesce request	1	I	Indicates that a 60x processor is requesting that all bus activity involving snoop operations pause or terminate so that the 60x processor may enter a low-power state.
$\overline{\text{SUSPEND}}$	Suspend	1	I	Activates the suspend power-saving mode.
SYSCLK	System clock	1	I	SYSCLK sets the frequency of operation for the PCI bus and provides a reference clock for the phase-locked loop (PLL) in the TSPC106. SYSCLK is used to synchronize bus operations. Refer to section “Clocking” on page 19 for more information.

IEEE 1149.1 Interface Signals

To facilitate system testing, the TSPC106 provides a JTAG test access port that complies with the IEEE 1149.1 boundary-scan specification.

Table 9. IEEE 1149.1 Interface Signals

Signal	Signal Name	Number of Pins	I/O	Signal Description
TCK	JTAG test clock	1	I	Input signals to the test access port (TAP) are clocked in on the rising edge of TCK. Changes to the TAP output signals occur on the falling edge of TCK. The test logic allows TCK to be stopped.
TDO	JTAG test data output	1	O	The contents of the selected internal instructions or data register are shifted out onto this signal on the falling edge of TCK. TDO will remain in a high-impedance state except when scanning of data is in progress.
TDI	JTAG test data input	1	I	The value presented on this signal on the rising edge of TCK is clocked into the selected JTAG test instruction or data register.
TMS	JTAG test mode select	1	I	This signal is decoded by the internal JTAG TAP controller to distinguish the primary operation of the test support circuitry.
$\overline{\text{TRST}}$	JTAG test reset	1	I	This input causes asynchronous initialization of the internal JTAG TAP controller.

Configuration Signals

The configuration signals select the ROM/Flash options, the clock mode of the TSPC106 and how the TSPC106 responds to addresses on the 60x and PCI buses.

Table 10. Configuration Signals

Signal	Number of Pins	I/O	Configuration
$\overline{\text{DBG0}}$(1)	1	I	High configures the TSPC106 for address map A. Low configures the TSPC106 for address map B.
$\overline{\text{FOE}}$(1)	1	I	High configures ROM bank 0 for an 8-bit data bus width. Low configures ROM bank 0 for an 64-bit data bus width. Note that the data bus width for ROM bank 1 is always 64 bits.
PLL[0:3](2)	4	I	High/Low – configuration for the PLL clock mode.
$\overline{\text{RCS0}}$(1)	1	I	High indicates ROM is located on the 60x processor/memory data bus. Low indicates ROM is located on the PCI bus.

Notes: 1. The TSPC106 samples these signals during a power-on reset or hard reset operation to determine the configuration. Weak pull-up or pull-down resistors should be used to avoid interference with the normal signal operations.
2. The TSPC106 continuously samples the phase-locked loop (PLL) configuration signals to allow the switching of clock modes or the bypass of the PLL without a hard reset operation.

Clocking

The TSPC106 requires a single system clock input, SYSCLK. The frequency of SYSCLK dictates the operating frequency of the PCI bus. An internal PLL on the TSPC106 generates a master clock that is used for all of the internal (core) logic. The master clock provides the core frequency reference and is phase-locked to the SYSCLK input. The 60x processor, L2 cache and memory interfaces operate at the core frequency.

The PLL[0:3] signals configure the core-to-SYSCLK frequency ratio. The TSPC106 supports core-to-SYSCLK frequency ratios of 1:1, 2:1 and 3:1, although not all ratios are supported for all frequencies. The TSPC106 supports changing the clock mode and bypassing the PLL without requiring a hard reset operation, provided the system design allows sufficient time for the PLL to relock.

Address Maps

The TSPC106 supports three address mapping configurations designated address map A, address map B, and emulation mode address map. Address map A conforms to the “PowerPC Reference Platform Specification”. Address map B conforms to the “PowerPC Common Hardware Reference Platform Architecture (CHRP)”. The emulation mode address map is provided to support software emulation fx86 hardware. The configuration signal $\overline{\text{DBG0}}$, sampled during power-on reset, selects between address map A and address map B. After reset, the address map can be changed by a programmable parameter. The emulation mode address map can only be selected by software after reset.

Detailed Specifications

Scope

This drawing describes the specific requirements of the TSPC106 in compliance with MIL-STD-883 class B or manufacturer's standard screening.

Applicable Documents

Documents applicable to the information contained in this datasheet are:

1. MIL-STD-883: Test Methods and Procedures for Electronics
2. MIL-PRF-38535: General Specifications for Microcircuits

Requirements

General

The microcircuits are in accordance with the applicable documents and as specified herein.

Design and Construction

Terminal Connections

The terminal connections are as shown in "Pin Description" on page 4.

Lead Material and Finish

Lead material and finish are as specified in "Package Mechanical Data" on page 37.

Package

The macrocircuits are packaged in 303-pin ceramic ball grid array packages.

The precise package drawings are described at the end of the specification. "CBGA Package Parameters" on page 37 and "CI_CGA Package Parameters" on page 38.

Absolute Maximum Ratings

Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

Table 11. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply Voltage	-0.3	3.6	V
AV_{DD}	PLL Supply Voltage	-0.3	3.6	V
V_{IN}	Input Voltage	-0.3	5.5	V
T_{STG}	Storage Temperature Range	-55	+150	°C

Notes:
1. Functional operating conditions are given in AC and DC electrical specifications. Stresses beyond the absolute maximums listed may affect device reliability or cause permanent damage to the device.
2. Caution: Input voltage must not be greater than the V_{DD} supply voltage by more than 2.5V at all times including during power-on reset.

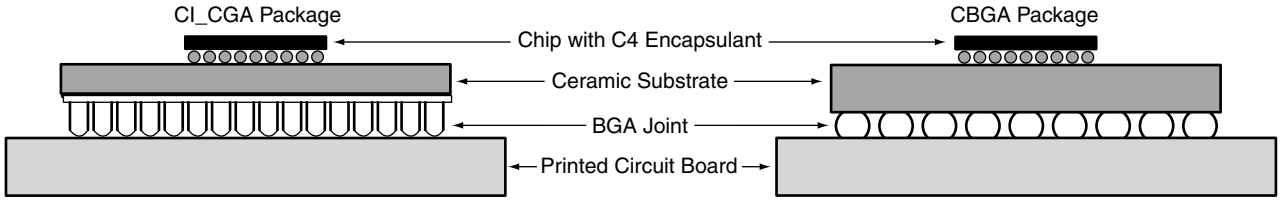
Thermal Characteristics

This section provides thermal management information for the C4/CBGA package. Proper thermal control design is primarily dependent upon the system-level design.

The use of C4 die on CBGA interconnect technology offers significant reduction in both the signal delay and the microelectronic packaging volume. Figure 5 shows the salient features of the C4/CBGA interconnect technology. The C4 interconnection provides both the electrical and the mechanical connections for the die to the ceramic substrate.

After the C4 solder bump is reflowed, epoxy (encapsulant) is under-filled between the die and the substrate. Under-fill material is commonly used on large high-power die; however, this is not a requirement of the C4 technology. The package substrate is a multilayer-co-fired ceramic. The package-to-board interconnection is via an array of orthogonal 90/10 (lead/tin) solder balls on 1.27 mm pitch. During assembly of the C4/CBGA package to the board, the high-melt balls do not collapse.

Figure 5. Exploded Cross-section



Internal Package Conduction Resistance

For the C4/CBGA packaging technology, the intrinsic conduction thermal resistance paths are as follows:

- the die junction-to-case thermal resistance
- the die junction-to-lead thermal resistance

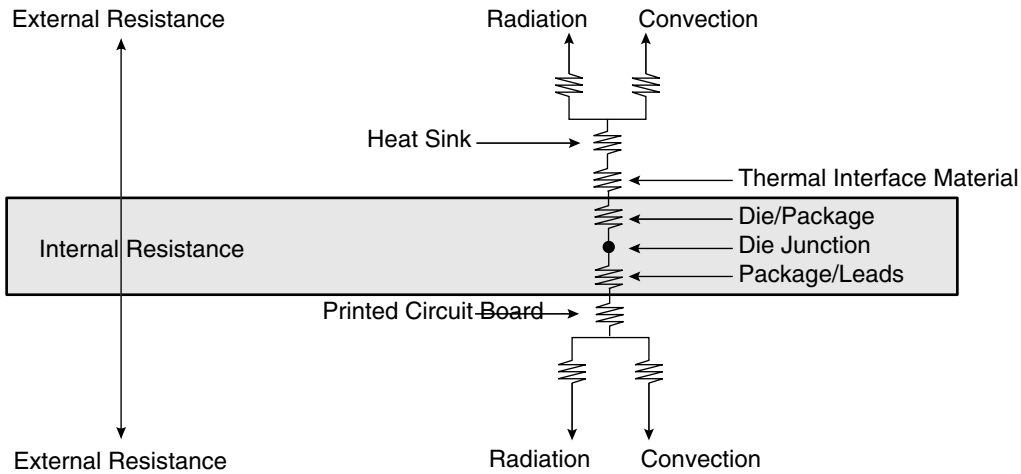
These parameters are shown in Table 12. In the C4/CBGA package, the silicon chip is exposed; therefore, the package case is the top of the silicon.

Table 12. Thermal Resistance

Thermal Metric	Effective Thermal Resistance
Junction-to-case thermal resistance	0.133°C/W
Junction-to-lead (ball) thermal resistance	3.8°C/W (CBGA package)
Junction-to-lead (column) thermal resistance	4.0°C/W (CI_CGA package)

Figure 6 shows a simplified thermal network in which a C4/CBGA package is mounted on a printed-circuit board.

Figure 6. C4/CBGA Package Mounted on a Printed Circuit Board



Note: Internal package resistance differs from external package resistance.

Power Consumption

The TSPC106 provides hardware support for four levels of power reduction – the doze, nap and sleep modes are invoked by register programming and the suspend mode is invoked by assertion of an external signal. The design of the TSPC106 is fully static, allowing internal logic states to be preserved during all power-saving modes. The following sections describe the programmable power modes provided by the TSPC106.

Full-power Mode

This is the default power state of the TSPC106 following a hard reset with all internal functional units fully powered and operating at full clock speed.

Doze Mode

In this power-saving mode, all the TSPC106 functional units are disabled except for PCI address decoding, system RAM refreshing and 60x bus request monitoring (through $\overline{\text{BR}}n$). Once the doze mode is entered, a hard reset, a PCI transaction referenced to system memory or a 60x bus request can bring the TSPC106 out of the doze mode and into the full-on state. If the TSPC106 is awakened for a processor or PCI bus access, the access is completed and the MC106 returns to the doze mode. The TSPC106's doze mode is totally independent of the power saving mode of the processor.

Nap Mode

Nap mode provides further power savings compared to doze mode. In nap mode, both the processor and the TSPC106 are placed in a power reduction mode. In this mode, only the PCI address decoding, system RAM refresh and the processor bus request monitoring are still operating. Hard reset, a PCI bus transaction referenced to system memory or a 60x bus request can bring the TSPC106 out of the nap mode. If the TSPC106 is awakened by a PCI access, the access is completed and the TSPC106 returns to the nap mode. If the TSPC106 is awakened by a processor access, the access is completed but the TSPC106 remains in the full-on state. When in the nap mode, the PLL is required to be running and locked to the system clock (SYSCLK).

Sleep Mode

Sleep mode provides further power saving compared to the nap mode. As in nap mode, both the processor and the TSPC106 are placed in a reduced power mode concurrently. In sleep mode, no functional units are operating except the system RAM refresh logic, which can continue (optionally) to perform the refresh cycles. A hard reset or a bus request wakes the TSPC106 from sleep mode. The PLL and SYSCLK inputs may be disabled by an external power management controller (PMC). For additional power savings, the PLL can be disabled by configuring the PLL[0:3] signals into the PLL-bypass mode. The external PMC must enable the PLL, turn on SYSCLK and allow the PLL time to lock before waking the system from sleep mode.

Suspend Mode

Suspend mode is activated through assertion of the $\overline{\text{SUSPEND}}$ signal. In suspend mode, the TSPC106 may have its clock input and PLL shut down for additional power savings. Memory refresh can be accomplished in two ways, either by using self-refresh mode DRAMs or by using the RTC input on the TSPC106. To exit the suspend mode, the system clock must be turned on in sufficient time to restart the PLL. After this time, $\overline{\text{SUSPEND}}$ may be negated. In suspend mode, all outputs (except memory refresh) are released to a high-impedance state and all inputs, including hard reset ($\overline{\text{HRST}}$), are ignored.

Power Dissipation

Table 13 provides figures on power consumption for the TSPC106.

Table 13. Power Consumption

Mode	SYSCLK/Core33/66 MHz	SYSCLK/Core33/83.3 MHz	Unit
Full-on Mode			
Typical	1.2	2.2	W
Maximum	1.4	2.4	W
Doze Mode			
Typical	1.0	1.1	W
Maximum	1.2	1.4	W
Nap Mode			
Typical	1.0	1.1	W
Maximum	1.2	1.4	W
Sleep Mode			
Typical	260	330	W
Maximum	360	450	W
Suspend Mode			
Typical	140	220	W
Maximum	190	270	W

Notes: 1. Power consumption for common system configurations assuming 50 pF loads.
2. Suspend power saving mode assumes SYSCLK off and PLL in bypass mode.
3. Typical power is an average value measured at $V_{DD} = AV_{DD} = 3.30$ V and $T_A = 25$ °C.
4. Maximum power is measured at $V_{DD} = AV_{DD} = 3.45$ V and $T_A = 25$ °C.

Marking

The documents that define the marking are identified in the related reference documents. Each microcircuit is legibly and permanently marked with the following information as a minimum:

- Manufacturer logo
- Manufacturer part number
- Class B identification (if applicable)
- Date-code of inspection lot
- ESD identifier (if available)
- Country of manufacture

Electrical Characteristics

Table 14. Recommended Operating Conditions

Characteristic	Symbol	Value	Unit	Notes
Supply voltage	V_{DD}	3.3 ± 165 mv	V	
PLL supply voltage	AV_{DD}	Min 2.51 - Max 3.465	V	
Input voltage	V_{in}	0 to 5.5	V	
Die junction temperature	T_j	0 to 105	°C	The extended temperature parts have die junction temperature of -40 to 105°C

General Requirements All static and dynamic electrical characteristics specified for inspection purposes and the relevant measurement conditions are given in Table 15.

Table 15. Clock DC Timing Specifications (V_{DD} = 3.3V ± 5% dc, GND = 0V dc, -55°C ≤ T_C ≤ 125°C)

Symbol	Characteristic	Min	Max	Unit
V_{IH}	Input high voltage (all inputs except SYSCLK)	2	5.5	V
V_{IL}	Input low voltage (all inputs except SYSCLK)	GND	0.8	V
CV_{IH}	SYSCLK input high voltage	2.4	5.5	V
CV_{IL}	SYSCLK input low voltage	GND	0.4	V
I_{in}	Input leakage current, V_{IN} = 3.3V(1)		15.0	µA
I_{TSI}	Hi-Z (off-state) leakage current, V_{IN} = 3.3V(1)		15.0	µA
V_{OH}	Output high voltage, I_{OH} = -7 mA	2.4		V
V_{OL}	Output low voltage, I_{OL} = 7 mA		0.5	V
V_{OH}	PCI 3.3V signaling output high voltage, I_{OH} = -0.5 mA	2.7		V
V_{OL}	PCI 3.3V signaling output low voltage, I_{OL} = 1.5 mA		0.3	V
C_{in}	Capacitance, V_{in} = 0V, f = 1 MHz(2)		7.0	pF

Notes:
1. Excludes test signals (LSSD_MODE and JTAG signals).
2. This value represents worst case 40 Ohm drivers (default value for Processor/L2 control signals $\overline{CI}$, $\overline{WT}$, $\overline{GBL}$, $\overline{TBST}$, TSIZ[0-2], TT[0-4], $\overline{TWE}$, and $\overline{TV}$) only. Other signals have lower default driver impedance and will support larger I_{OH} and I_{OL}. All drivers may optionally be programmed to different driver strengths.
3. Capacitance is periodically sampled rather than 100% tested.

Dynamic Characteristics

This section provides the AC electrical characteristics for the TSPC106. After fabrication, parts are sorted by maximum 60x processor bus frequency as shown in Table 16 and tested for conformance to the AC specifications for that frequency. These specifications are for operation between 16.67 and 33.33 MHz PCI bus (SYSCLK) frequencies. The 60x processor bus frequency is determined by the PCI bus (SYSCLK) frequency and the settings of the PLL[0:3] signals. All timings are specified relative to the rising edge of SYSCLK.

Clock AC Specifications

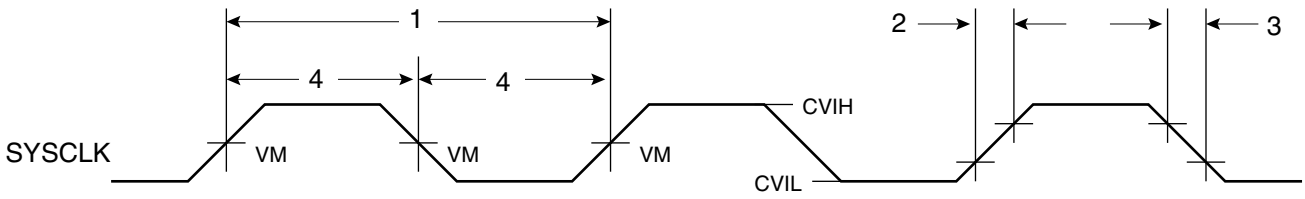
Table 16 provides the clock AC timing specifications as defined in Figure 7.

Table 16. Clock AC Timing Specifications (V_{DD} = 3.3V ± 5% dc, GND = 0V dc, -55°C ≤ T_C ≤ 125°C)

Ref	Characteristic	SYSCLK/Core 33/66 MHz		SYSCLK/Core 33/83.3 MHz		Unit
		Min	Max	Min	Max	
	60x processor bus (core) frequency(1)	16.67	66	16.67	83.3	MHz
	VCO frequency(1)	150	400	150	400	MHz
	SYSCLK frequency(1)	16.67	33.33	16.67	33.33	MHz
1	SYSCLK cycle time	30.0	60.0	30.0	60.0	ns
2, 3	SYSCLK rise and fall time(2)		2.0		2.0	ns
4	SYSCLK duty cycle measured at 1.4V(3)	40	60	40	60	%
	SYSCLK jitter(4)		±200		±200	ps
	106 internal PLL relock time(3, 5)		100		100	µs

Notes:
1. The SYSCLK frequency and PLL[0:3] settings must be chosen so that the resulting SYSCLK (bus) frequency, CPU (core) frequency and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL[0:3] signal description in “System Design Information” on page 33 for valid PLL[0:3] settings.
2. Rise and fall times for the SYSCLK input are measured from 0.4V to 2.4V.
3. Timing is guaranteed by design and characterization and is not tested.
4. The total input jitter (short-term and long-term combined) must be under ±200 ps.
5. PLL-relock time is the maximum time required for PLL lock after a stable V_{DD}, AV_{DD}, and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently reenabled during the sleep and suspend power-saving modes. Also note that $\overline{\text{HRST}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time (100 ms) during the power-on reset sequence.

Figure 7. SYSCLK Input Timing Diagram



Note: VM = Midpoint Voltage (1.4V)

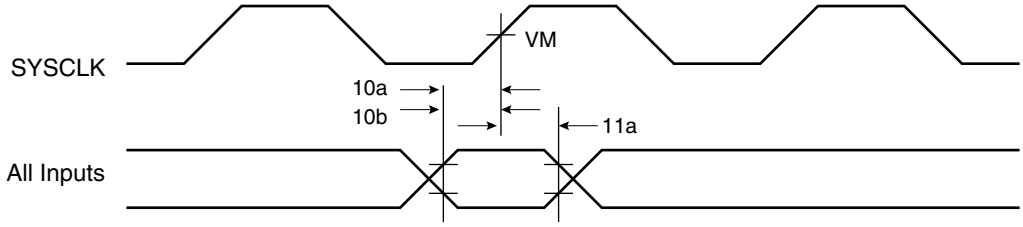
Input AC Specifications Table 17 provides the input AC timing specifications as shown in Figure 8 and Figure 9.

Table 17. Input AC Timing Specifications (V_{DD} = 3.3V ± 5% dc, GND = 0V dc, C_L = 50 pF, -55°C ≤ T_C ≤ 125°C)

		66 MHz		83.3 MHz		
Ref	**Characteristic**	**Min**	**Max**	**Min**	**Max**	**Unit**
10a	Group I input signals valid to SYSCLK (input setup)(1, 2, 3)	4.0		3.5		ns
10a	Group II input signals valid to SYSCLK (input setup)(1, 2, 4)	3.5		3.5		ns
10a	Group III input signals valid to SYSCLK (input setup)(1, 2, 5)	3.0		2.5		ns
10a	Group IV input signals valid to SYSCLK (input setup)(1, 2, 6)	5.0		4.0		ns
10b	Group V input signals valid to SYSCLK (input setup)(7, 8)	7.0		7.0		ns
10b	Group VI input signals valid to SYSCLK (input setup)(7, 9)	7.0		7.0		ns
11a	60x Bus Clock to group I - IV inputs invalid (input hold)(3, 4, 5, 6)	0		0		ns
11b	SYSCLK to group V - VI inputs invalid (input hold)(8, 9)	-0.5		-0.5		ns
	$\overline{\text{HRST}}$ pulse width	255 x t_{SYSCLK} +100 µs		255 x t_{SYSCLK} +100 µs		
10c	Mode select inputs valid to $\overline{\text{HRST}}$ (input setup)(10, 11, 12)	3 x t_{SYSCLK}		3 x t_{SYSCLK}		ns
11c	$\overline{\text{HRST}}$ to mode select input invalid (input hold)(10, 12)	1.0		1.0		ns

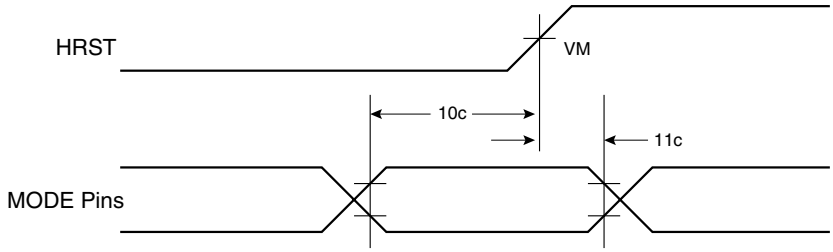
Notes:
1. Input specifications are measured from the TTL level (0.8 or 2.0V) of the signal in question to the 1.4V of the rising edge of the input SYSCLK. Input and output timings are measured at the pin.
2. Processor and memory interface signals are specified from the rising edge of the 60x bus clock.
3. Group I input signals include the following processor, L2 and memory interface signals: A[0:31], PAR[0:7]/AR[1:8],$\overline{\text{BR}}$[0:4], $\overline{\text{BRL2}}$, $\overline{\text{XATS}}$, $\overline{\text{LBCLAIM}}$, $\overline{\text{ADS}}$, BA0, TV and $\overline{\text{HIT}}$ (when configured for external L2).
4. Group II input signals include the following processor and memory interface signals: $\overline{\text{TBST}}$, TT[0:4], TSIZ[0:2], $\overline{\text{WT}}$, $\overline{\text{CI}}$, $\overline{\text{GBL}}$, $\overline{\text{AACK}}$ and $\overline{\text{TA}}$.
5. Group III input signals include the following processor and memory interface signals: DL[0:31] and DH[0:31].
6. Group IV input signals include the following processor and L2 interface signals: $\overline{\text{TS}}$, $\overline{\text{ARTRY}}$, $\overline{\text{DIRTY\_IN}}$ and $\overline{\text{HIT}}$ (when configured for internal L2 controller).
7. PCI 3.3 V signaling environment signals are measured from 1.65V (V_{DD}÷ 2) on the rising edge of SYSCLK to V_{OH} = 3.0V or V_{OL} = 0.3V.
   PCI 5V signaling environment signals are measured from 1.65V (V_{DD}÷ 2) on the rising edge of SYSCLK to V_{OH} = 2.4V or V_{OL} = 0.55V.
8. Group V input signals include the following bussed PCI interface signals: $\overline{\text{FRAME}}$, $\overline{\text{C/BE}}$[0:3], AD[0:31], $\overline{\text{DEVSEL}}$, $\overline{\text{IRDY}}$, $\overline{\text{TRDY}}$, $\overline{\text{STOP}}$, $\overline{\text{PAR}}$, $\overline{\text{PERR}}$, $\overline{\text{SERR}}$, $\overline{\text{LOCK}}$, $\overline{\text{FLSHREQ}}$, and $\overline{\text{ISA\_MASTER}}$.
9. Group VI input signal is the point-to-point PCI $\overline{\text{GNT}}$ input signal.
10. The setup and hold time is with respect to the rising edge of $\overline{\text{HRST}}$. Mode select inputs include the $\overline{\text{RCS0}}$, $\overline{\text{FOE}}$ and $\overline{\text{DBG0}}$ configuration inputs.
11. t_{SYSCLK} is the period of the external clock (SYSCLK) in nanoseconds (ns). When the unit is given as t_{SYSCLK} the numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in nanoseconds) of the parameter in question.
12. These values are guaranteed by design and are not tested.

Figure 8. Input Timing Diagram



Note: VM = Midpoint Voltage (1.4V)

Figure 9. Mode Select Input Timing Diagram



Note: VM = Midpoint Voltage (1.4V)

Output AC Specifications

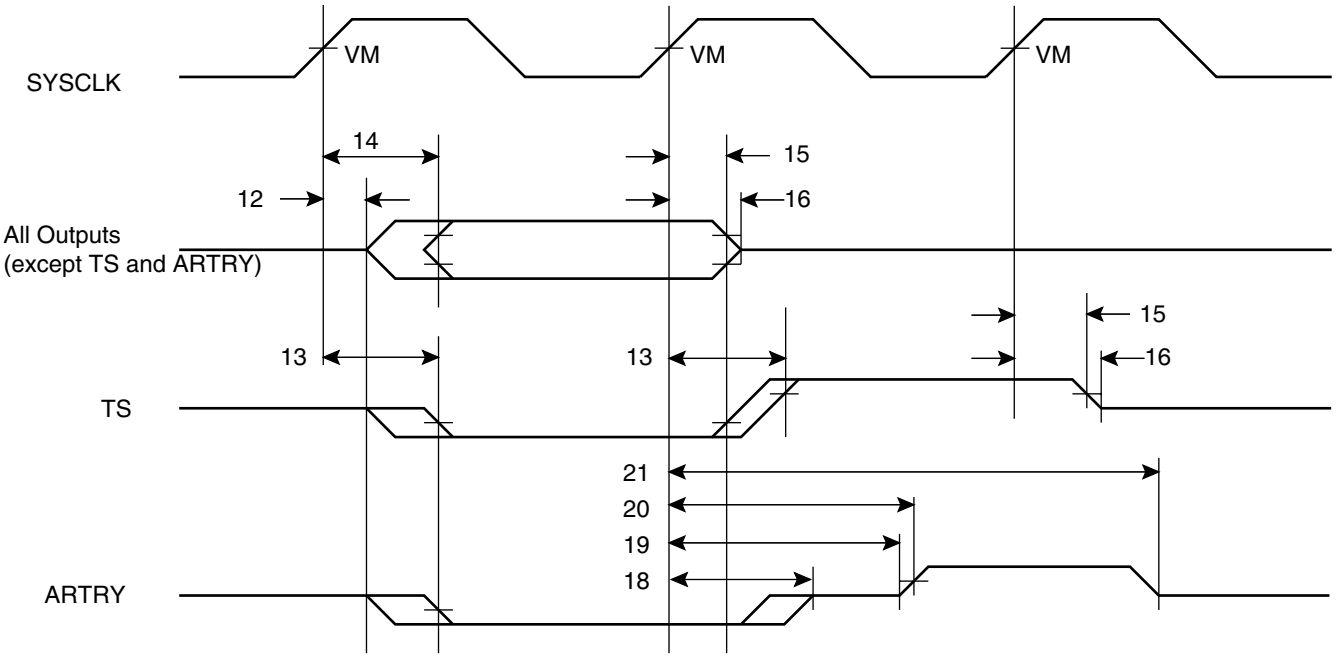
Table 18 provides the output AC timing specifications as shown in Figure 10.

Table 18. Output AC Timing Specifications (V_{DD} = 3.3V ± 5% dc, GND = 0V dc, C_L = 50 pF, -55°C ≤ T_C ≤ 125°C)

Ref	Characteristic	66 MHz		83.3 MHz		Unit
		Min	Max	Min	Max	
12	SYSCLK to output driven (output enable time)(9)	2.0		2.0		ns
13a	SYSCLK to output valid (for $\overline{TS}$ and $\overline{ARTRY}$)(1, 2, 3, 4)		7.0		6.0	ns
13b	SYSCLK to output valid (for all non-PCI signals except $\overline{TS}$, $\overline{ARTRY}$, $\overline{RAS}$[0:7] and $\overline{CAS}$[0:7]) and DWE[0:2](1, 2, 3, 5)		7.0		6.0	ns
14a	SYSCLK to output valid (for RAS[0:7] and CAS[0:7])(1, 2, 3)		7.0		6.0	ns
14b	SYSCLK to output valid (for PCI signals)(3, 6)		11.0		11.0	ns
15a	SYSCLK to output invalid for all non-PCI signals (output hold)(7, 10)	1.0		1.0		ns
15b	SYSCLK to output valid for PCI signals (output hold)(7)	1.0		1.0		ns
18	SYSCLK to $\overline{ARTRY}$ high impedance before precharge (output hold)(9)		8.0		8.0	ns
19	SYSCLK to $\overline{ARTRY}$ precharge enable(8, 9)	(0.4 x t_{SYSCLK}) + 2.0		(0.4 x t_{SYSCLK}) + 2.0		ns
21	SYSCLK to $\overline{ARTRY}$ high impedance after precharge(8, 9)		(1.5 x t_{SYSCLK}) + 8.0		(1.5 x t_{SYSCLK}) + 8.0	ns

Notes:
1. Processor and memory interface signals are specified from the rising edge of the 60x bus clock.
2. Output specifications are measured from 1.4V on the rising edge of SYSCLK to the TTL level (0.8V or 2.0V) of the signal in question. Both input and output timings are measured at the pin.
3. The maximum timing specification assumes C_L = 50 pF.
4. The shared outputs TS and ARTRY require pull-up resistors to hold them negated when there is no bus master driving them.
5. When the TSPC106 is configured for asynchronous L2 cache SRAMs, the DWE[0:2] signals have a maximum SYSCLK to output valid time of (0.5 x t_{PROC}) + 8.0 ns (where t_{PROC} is the 60x bus clock cycle time).
6. PCI 3.3V signaling environment signals are measured from 1.65V (V_{DD}÷ 2) on the rising edge of SYSCLK to V_{OH} = 3.0V or V_{OL} = 0.3V.
7. The minimum timing specification assumes C_L = 50 pF.
8. t_{SYSCLK} is the period of the external bus clock (SYSCLK) in nanoseconds (ns). When the unit is given as t_{SYSCLK}, the numbers given in the table must be multiplied by the period of SYSCLK to compute the actual duration in nanoseconds of the parameter in question.
9. These values are guaranteed by design and are not tested.
10. PCI devices which require more than the PCI-specified hold time of T_H = 0 ns or systems where clock skew approaches the PCI-specified allowance of 2 ns may not work with the TSPC106. For workarounds, see Motorola application note “Designing PCI 2.1-compliant MPC106 Systems” (order number AN1727/D).

Figure 10. Output Timing Diagram



Note: VM = Midpoint Voltage (1.4V)

Table 19. JTAG AC Timing Specifications (Independent of SYSCLK) (V_{DD} = 3.3V ± 5% dc, GND = 0V dc,C_L = 50 pF, -55°C ≤ T_C ≤ 125°C)

Ref	Characteristic	Min	Max	Unit
	TCK frequency of operation	0	25	MHz
1	TCK cycle time	40		ns
2	TCK clock pulse width measured at 1.4 V	20		ns
3	TCK rise and fall times	0	3	ns
4	TRST setup time to TCK rising edge(1)	10		ns
5	TRST assert time	10		ns
6	Boundary-scan input data setup time(2)	5		ns
7	Boundary-scan input data hold time(2)	15		ns
8	TCK to output data valid(3)	0	30	ns
9	TCK to output high impedance(3)	0	30	ns
10	TMS, TDI data setup time	5		ns
11	TMS, TDI data hold time	15		ns
12	TCK to TDO data valid	0	15	ns
13	TCK to TDO high impedance	0	15	ns

Notes:
1. These values are guaranteed by design, and are not tested.
2. TRST is an asynchronous signal. The setup time is for test purposes only.
3. Non-test signal input timing with respect to TCK.
4. Non-test signal output timing with respect to TCK.

Figure 11. JTAG Clock Input Timing Diagram

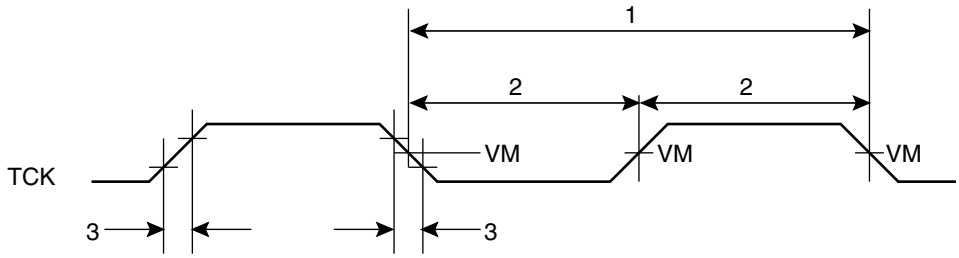


Figure 12. TRST Timing Diagram

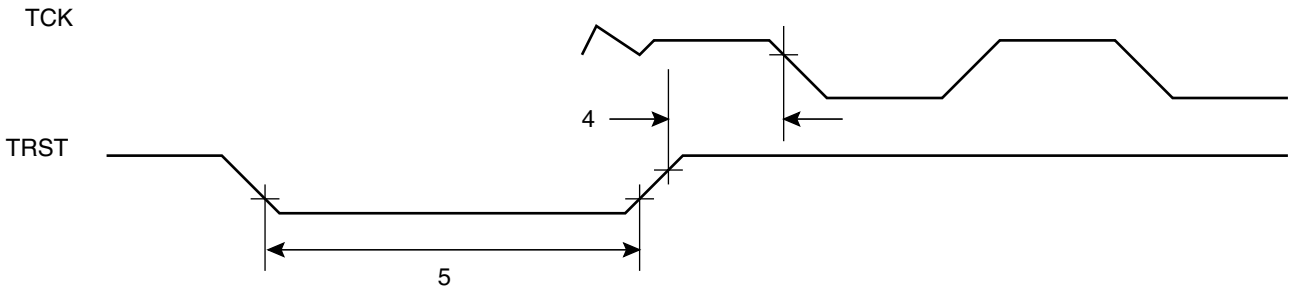


Figure 13. Boundary-scan Timing Diagram

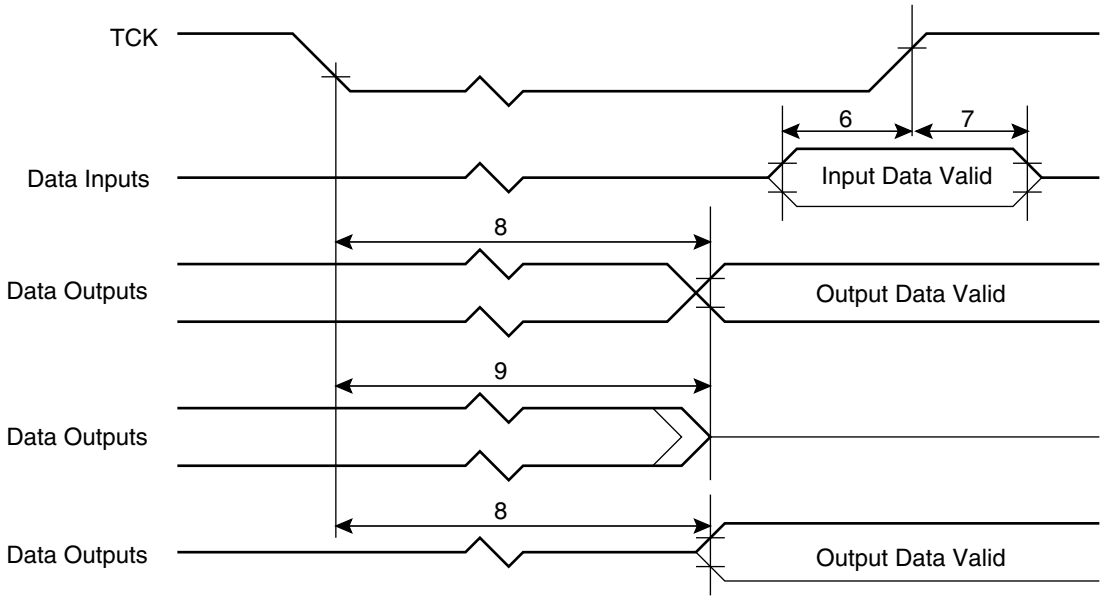
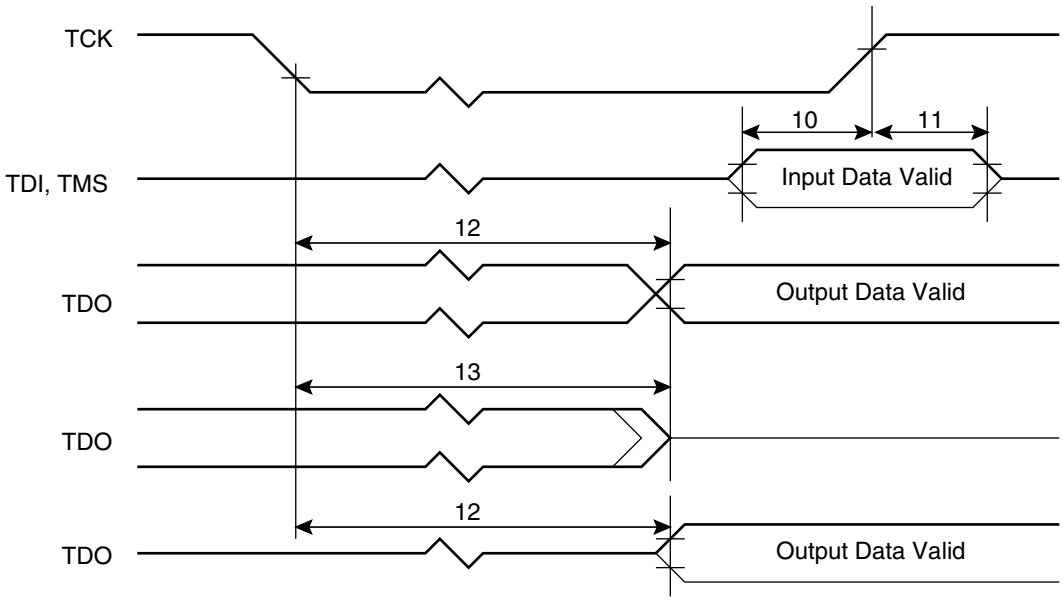


Figure 14. Test Access Port Timing Diagram



Architectural Overview

60x Processor Interface

The TSPC106 supports a programmable interface to a variety of PowerPC microprocessors operating at select bus speeds.The address bus is 32 bits wide and the data bus is 64 bits wide. The 60x processor interface of the TSPC106 uses a subset of the 60x bus protocol, supporting single-beat and burst data transfers. The address and data buses are decoupled to support pipelined transactions.

Two signals on the TSPC106, local bus slave claim ($\overline{\text{LBCLAIM}}$) and data bus grant local bus slave ($\overline{\text{DBGLB}}$), are provided for an optional local bus slave. However, the local bus slave must be capable of generating the transfer acknowledge ($\overline{\text{TA}}$) signal to interact with the 60x processor(s).

Depending on the system implementation, the processor bus may operate at the PCI bus clock rate or at two or three times the PCI bus clock rate. The 60x processor bus is synchronous with all timing relative to the rising edge of the 60x bus clock.

Secondary (L2) Cache/Multiple Processor Interface

The 106 provides support for the following configurations of 60x processors and L2 cache:

- Up to four 60x processors with no L2 cache
- A single 60x processor plus a direct-mapped, lookaside, L2 cache using the internal L2 cache controller of the TSPC106
- Up to four 60x processors plus an externally-controlled L2 cache

The internal L2 cache controller generates the arbitration and support signals necessary to maintain a write-through or write-back L2 cache. The internal L2 cache controller supports either asynchronous SRAMs, pipelined burst SRAMs or synchronous burst SRAMs, using byte parity for data error detection.

When more than one 60x processor is used, nine signals of the L2 interface change their functions (to $\overline{BR}$[1:3], $\overline{BG}$[1:3] and $\overline{DBG}$[1:3]) to allow for arbitration between the 60x processors. The 60x processors share all 60x interface signals of the TSPC106, except the bus request ($\overline{BR}$), bus grant ($\overline{BG}$) and the data bus grant ($\overline{DBG}$) signals.

When an external L2 controller (or integrated L2 cache module) is used, three signals of the L2 interface change their functions (to $\overline{BRL2}$, $\overline{BGL2}$ and $\overline{DBGL2}$) to allow the TSPC106 to arbitrate between the external cache and the 60x processor(s).

Memory Interface

The memory interface controls processor and PCI interactions to main memory. It is capable of supporting a variety of DRAM or extended data out (EDO) DRAM and ROM or Flash ROM configurations as main memory. The maximum supported memory size is 1-Gbyte of DRAM or EDO DRAM, with 16M bytes of ROM or Flash ROM. The memory controller of the TSPC106 supports the various memory sizes through software initialization of on-chip configuration registers. Parity or ECC is provided for error detection.

The TSPC106 controls the 64-bit data path to main memory (72-bit data path with parity or ECC). To reduce loading on the data bus, system designers must implement buffers between the 60x bus and memory. The TSPC106 features configurable data/parity buffer control logic to accommodate several buffer types.

The TSPC106 is capable of supporting a variety of DRAM/EDO configurations. DRAM/EDO banks can be built of SIMMS, DIMMs or directly-attached memory devices. Thirteen multiplexed address signals provide for device densities up to 16 Mbits. Eight row address strobe ($\overline{RAS}$[0:7]) signals support up to eight banks of memory. The TSPC106 supports bank sizes from 2M bytes to 128M bytes. Eight column address strobe ($\overline{CAS}$[0:7]) signals are used to provided byte selection for memory bank access (note that all $\overline{CAS}$ signals are driven in ECC mode).

The TSPC106 provides parity checking and generation in two forms, normal parity and read-modify-write (RMW) parity. As an alternative to simple parity, the TSPC106tspc106 supports error checking and correction (ECC) for system memory. Using ECC, the TSPC106 detects and corrects all single-bit errors and detects all double-bit errors and all errors within a nibble (i.e., four bits or one-half byte).

For ROM/Flash support, the TSPC106 provides 20 address bits (21 address bits for the 8-bit wide ROM interface), two bank selects, one output enable, and one Flash ROM write enable. The 16-Mbyte ROM space is subdivided into two 8-Mbyte banks. Bank 0 (selected by $\overline{RCS0}$) is addressed from 0xFF80_0000 to 0xFFFF_FFFF. Bank 1 (selected by $\overline{RCS1}$) is addressed from 0xFF00_0000 to 0xFF7F_FFFF. A configuration signal, flash output enable ($\overline{FOE}$) sampled at reset, determines the bus width of the ROM or Flash device (8-bit or 64-bit) in bank 0. The data bus width for ROM bank 1 is always 64 bits. For systems using the 8-bit interface to bank 0, the ROM/Flash device must be connected to the most-significant byte lane of the data bus (DH[0:7]).

The TSPC106 also supports a mixed ROM system configuration. That is, the system can have the upper 8M bytes (bank 0) of ROM space located on the PCI bus and the lower 8M bytes (bank 1) of ROM located on the 60x/memory bus.

PCI Interface

The TSPC106's PCI interface is compliant with the PCI Local Bus Specification, Revision 2.1, and follows the guidelines in the PCI System Design Guide, Revision 1.0 for host bridge architecture. The PCI interface connects the processor and memory buses to the PCI bus, to which I/O components are connected. The PCI bus uses a 32-bit multiplexed address/data plus various control and error signals.

The PCI interface of the TSPC106 functions as both a master and target device. As a master, the TSPC106 supports read and write operations to the PCI memory space, the PCI I/O space, and the PCI configuration space. The TSPC106 also supports PCI special-cycle and interrupt-acknowledge commands. As a target, the TSPC106 supports read and write operations to system memory. Mode selectable big-endian to little-endian conversion is supplied at the PCI interface.

Internal buffers are provided for I/O operation between the PCI bus and the 60x processor or memory. Processor read and write operations each have a 32-byte buffer and memory operation has one 32-byte read buffer and two 32-byte write buffers.

System Design Information

This section provides electrical and thermal design recommendations for successful application of the TSPC106.

PLL Configuration

The TSPC106 requires a single system clock input, SYSCLK. The SYSCLK frequency dictates the frequency of operation for the PCI bus. An internal PLL on the TSPC106 generates a master clock that is used for all of the internal (core) logic. The master clock provides the core frequency reference and is phase-locked to the SYSCLK input. The 60x processor, L2 cache and memory interfaces operate at the core frequency. In the 5:2 clock mode (Rev. 4.0 only), the TSPC106 needs to sample the 60x bus clock (on the $\overline{\text{LBCLAIM}}$ configuration input) to resolve clock phasing with the PCI bus clock (SYSCLK).

The PLL is configured by the PLL[0:3] signals. For a given SYSCLK (PCI bus) frequency, the clock mode configuration signals (PLL[0:3]) set the core frequency (and the frequency of the VCO controlling the PLL lock). The supported core and VCO frequencies and the corresponding PLL[0:3] settings are provided in Table 19.

Table 20. Core/VCO Frequencies and PLL Settings

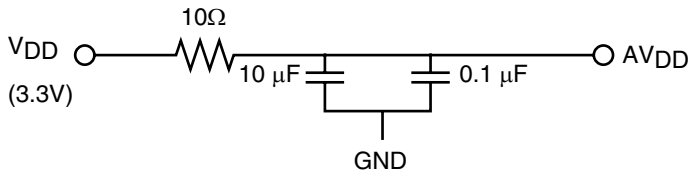
PLL[0:3](1)	Core/SYSCL Ratio	VCO Multiplier	Core Frequency (VCO Frequency) in MHz			
			PCI Bus 16.6 MHz	PCI Bus 20 MHz	PCI Bus 25 MHz	PCI Bus 33.3 MHz
0010	1:1	x8				33.3 (266)
0101	2:1	x4		40 (160)	50 (200)	66.6 (266)
0110	5:2(2)	x2				83.3 (166)
0111	5:2(2)	x4	41.6 (166)	50 (200)	62,5 (250)	83,3 (333)
1000	3:1	x2			75 (150)	
1001	3:1	x4		60 (240)	75 (300)	
0011	PLL Bypass(3)		PLL off SYSCLK clocks core circuitry directly 1 x core/SYSCLK ratio implied			
1111	Clock off(4)		PLL off No core clocking occurs			

Notes:
1. PLL[0:3] settings not listed are reserved. Some PLL configurations may select bus, CPU or VCO frequencies which are not useful, not supported or not tested. See “Input AC Specifications” on page 26 for valid SYSCLK and VCO frequencies.
2. 5:2 clock modes are only supported by TSPC106 Rev 4.0; earlier revisions do not support 5:2 clock modes. The 5:2 modes require a 60x bus clock applied to the 60x clock phase ($\overline{\text{LBCLAIM}}$) configuration input signal during power-on reset, hard reset and coming out of sleep and suspend power saving modes.
3. In PLL-bypass mode, the SYSCLK input signal clocks the internal circuitry directly, the PLL is disabled and the core/SYSCLK ratio is set for 1:1 mode operation. This mode is intended for factory use only.
   Note: The AC timing specifications given in this document do not apply in PLL-bypass mode.
4. In clock-off mode, no clocking occurs inside the TSPC106 regardless of the SYSCLK input.
5. PLL[0:3] = 0010 (1:1 Core/SYSCLK Ratio; X8 VCO Multiplier) exists on the chip but will fail to lock 50% of the time. Therefore this configuration should not be used and 1:1 modes between 16 and 25 MHz are not supported.

PLL Power Supply Filtering

The AV_{DD} power signal is provided on the 106 to provide power to the clock generation phase-locked loop. To ensure stability of the internal clock, the power supplied to the AV_{DD} input signal should be filtered using a circuit similar to the one shown in Figure 15. The circuit should be placed as close as possible to the AV_{DD} pin to ensure it filters out as much noise as possible.

Figure 15. PLL Power Supply Filter Circuit



Decoupling Recommendations

Due to the TSPC106's large address and data buses, and high operating frequencies, the TSPC106 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the system, and the TSPC106 itself requires a clean, tightly regulated source of power.

It is strongly recommended that the system design include six to eight 0.1 µF (ceramic) and 10 µF (tantalum) decoupling capacitors to provide both high- and low-frequency filtering. These capacitors should be placed closely around the perimeter of the TSPC106 package (or on the underside of the PCB). It is also recommended that these decoupling capacitors receive their power from separate V_{DD} and GND power planes in the PCB, utilizing short traces to minimize inductance. Only SMT (surface mount technology) capacitors should be used to minimize lead inductance.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} plane, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors are 100 µF (AVX TPS tantalum) or 330 µF (AVX TPS tantalum).

Connection Recommendations

To ensure reliable operation, it is recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied (using pull-up resistors) to V_{DD}. Unused active high inputs should be tied (using pull-down resistors) to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, AV_{DD} and GND pins of the TSPC106.

Pull-up Resistor Recommendations

The TSPC106 requires pull-up (or pull-down) resistors on several control signals of the 60x and PCI buses to maintain the control signals in the negated state after they have been actively negated and released by the TSPC106 or other bus masters. The JTAG test reset signal, $\overline{\text{TRST}}$, should be pulled down during normal system operation. Also, as indicated in Table 21, the factory test signal, $\overline{\text{LSSD\_MODE}}$, must be pulled up for normal device operation.

During inactive periods on the bus, the address and transfer attributes on the bus (A[0:31], TT[0:4], $\overline{\text{TBST}}$, $\overline{\text{WT}}$, $\overline{\text{CI}}$ and $\overline{\text{GBL}}$) are not driven by any master and may float in the high-impedance state for relatively long periods of time. Since the TSPC106 must continually monitor these signals, this float condition may cause excessive power draw by the input receivers on the TSPC106 or by other receivers in the system. It is recommended that these signals be pulled up or restored in some manner by the system.

The 60x data bus input receivers on the TSPC106 do not require pull-up resistors on the data bus signals (DH[0:31], DL[0:31] and PAR[0:7]). However, other data bus receivers in the system may require pull-up resistors on these signals.

In general, the 60x address and control signals are pulled up to 3.3 Vdc and the PCI control signals are pulled up to 5 Vdc through weak (2 - 10 kΩ) resistors. Resistor values may need to be adjusted stronger to reduce induced noise on specific board designs. Table 21 summarizes the pull-up/pull-down recommendations for the TSPC106.

Table 21. Pull-up/Pull-down Recommendations

Signal Type	Signals	Pull-up/Pull-down
60x bus control	$\overline{\text{BR}}$n, $\overline{\text{TS}}$, $\overline{\text{XATS}}$, $\overline{\text{AACK}}$, $\overline{\text{ARTRY}}$, $\overline{\text{TA}}$	Pull-up to 3.3V dc
60x bus address/transfer attributes	A[0:31], TT[0:4], $\overline{\text{TBST}}$, $\overline{\text{WT}}$, $\overline{\text{CI}}$, $\overline{\text{GBL}}$	Pull-up to 3.3V dc
Cache control	ADS	Pull-up to 3.3V dc
	HIT, TV	Pull-up to 3.3V dc or pull-down to GND depending on programmed polarity
PCI bus control	$\overline{\text{REQ}}$, $\overline{\text{FRAME}}$, $\overline{\text{IRDY}}$, $\overline{\text{DEVSEL}}$, $\overline{\text{TRDY}}$, $\overline{\text{STOP}}$, $\overline{\text{SERR}}$, $\overline{\text{PERR}}$, $\overline{\text{LOCK}}$, $\overline{\text{FLSHREQ}}$, $\overline{\text{ISA\_MASTER}}$	Pull-up to 5V dc Note: For closed systems not requiring 5V power, these may be pulled up to 3.3 VDC.
JTAG	TRST	Pull-down to GND (during normal system operation)
Factory test	LSSD_MODE	Pull-up to 3.3V dc

Preparation for Delivery

Packaging

Microcircuits are prepared for delivery in accordance with MIL-PRF-38535.

Certificate of Compliance

Atmel offers a certificate of compliance with each shipment of parts, confirming that the products are in compliance with MIL-STD-883 and guaranteeing the parameters not tested at temperature extremes for the entire temperature range.

Handling

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended:

- Devices should be handled on benches with conductive and grounded surfaces.
- Ground test equipment, tools and operator.
- Do not handle devices by the leads.
- Store devices in conductive foam or carriers.
- Avoid use of plastic, rubber or silk in MOS areas.
- Maintain relative humidity above 50% if practical.

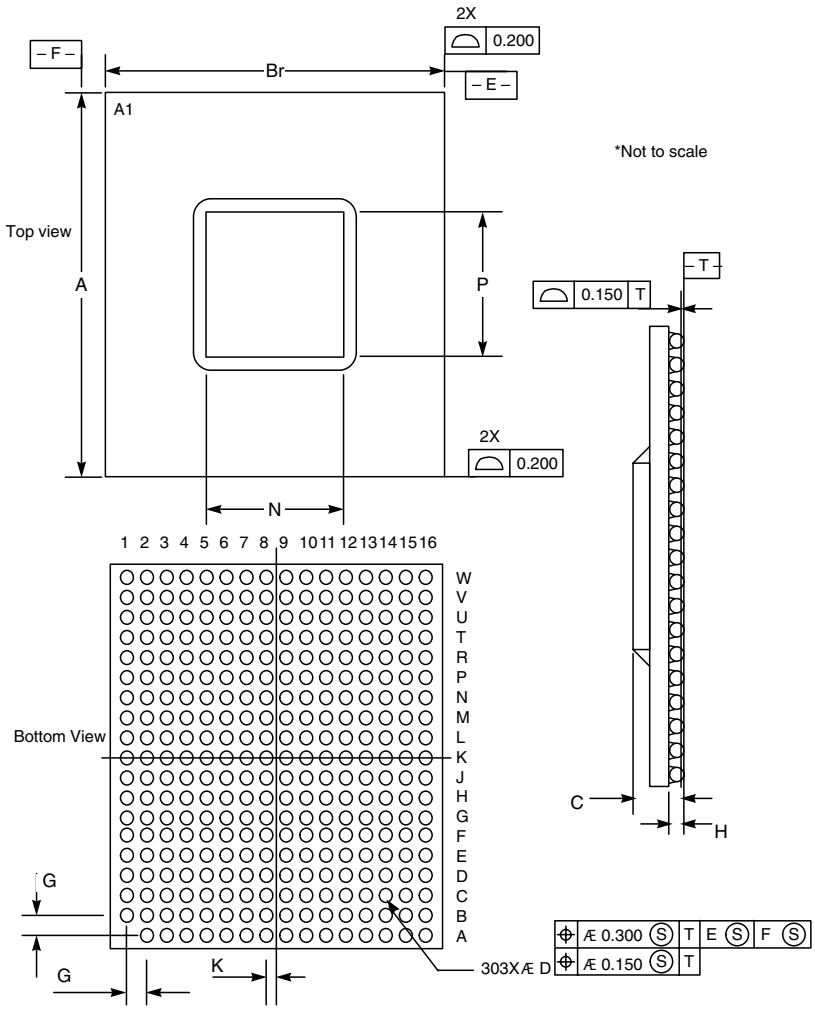
Package Mechanical Data

CBGA Package Parameters

Table 22. CBGA Package Parameters

Parameter	Min	Max	Parameter	Min	Max
Package outline	21 mm x 25 mm		A	25.0 ± 0.2	
Interconnects	303 (16 x 19 ball array minus one)		B	21.0 ± 0.2	
Pitch	1.27 mm		C	2.3	3.16
Solder attach	63/37 Sn/Pb		D	0.82	0.93
Solder balls	10/90 Sn/Pb, 0.89 mm diameter		G	1.27 BASIC	
Maximum module height	3.16 mm		H	0.79	0.99
Co-planarity specification	0.15 mm		K	0.635 BASIC	
			N	5.8	6.0
			P	7.2	7.4

Figure 16. CBGA Mechanical Drawing

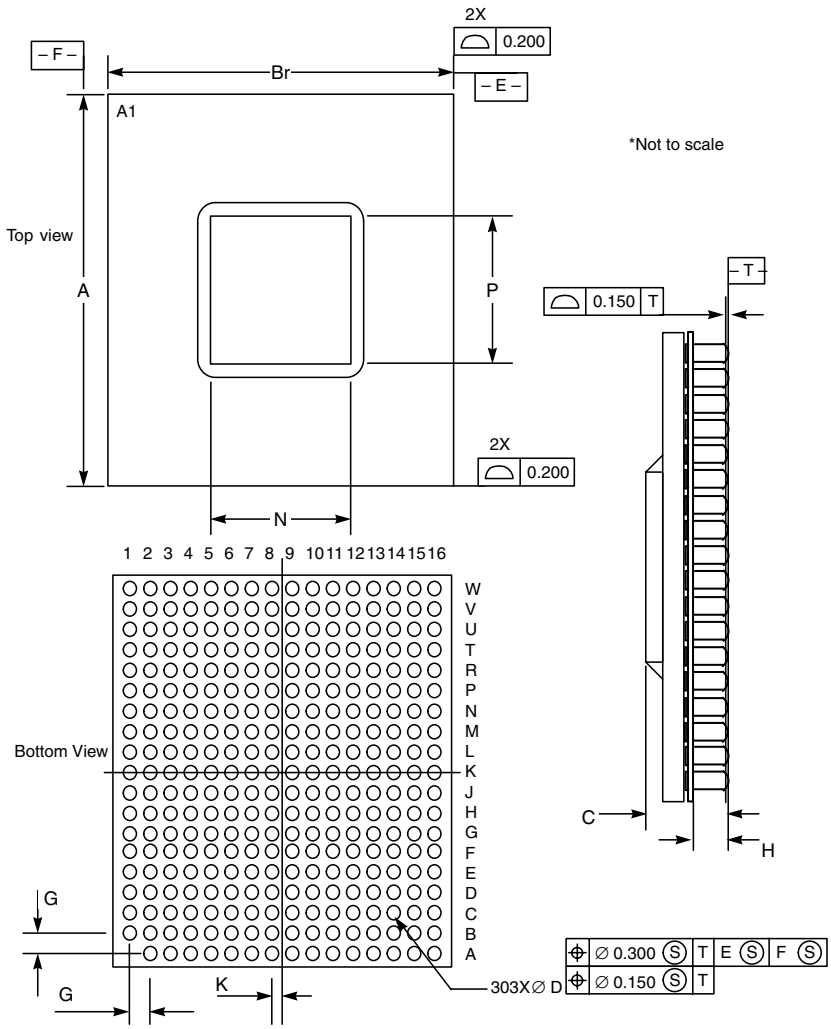


CI_CGA Package Parameters

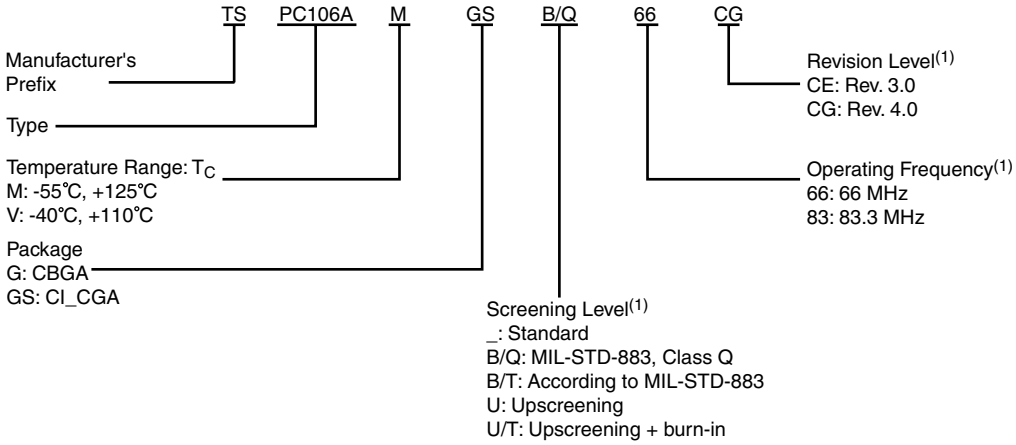
Table 23. CI-CGA Package Parameters

Parameter	Min	Max	Parameter	Min	Max
Package outline	21 mm x 25 mm		A	25.0 BASIC	
Interconnects	303 (16 x 19 ball array minus one)		B	21.0 BASIC	
Pitch	1.27 mm		C	3.84 BASIC	
Solder attach	63/37 Sn/Pb		D	0.79	0.99
Solder balls	10/90 Sn/Pb, 0.89 mm diameter		G	1.27 BASIC	
Maximum module height	3.84 mm		H	1.545	1.695
Co-planarity specification	0.15 mm		K	0.635 BASIC	
			N	6.2 BASIC	
			P	7.6 BASIC	

Figure 17. CI_CGA Mechanical Drawing



Ordering Information



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