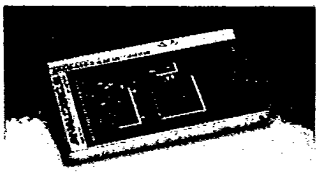

ANALOGIC

# ADAM-826-3

**16-Bit, 1.5 μs Unbuffered A/D Converter**

## Description T-51-10-16

The 1.5 μs A/D Converter itself is available for those applications where the signal has already been conditioned and only the A/D conversion function is required. In this configuration, as depicted in the Block Diagram of Figure 12, the duplication of circuitry and errors associated with an internal buffer amplifier or S/H are eliminated.

To preserve the full performance capability inherent in the A/D, whether configured for ± 10V bipolar or 0V to + 10V unipolar signals, care must be exercised in its implementation in the system. The input impedance of the unbuffered A/D is 1.4 kΩ unipolar or 2.8 kΩ bipolar. The pc etch that connects the A/D input to the signal source(s) must be carefully routed to avoid other etches carrying digital signals to prevent coupling of digital noise into the analog input. In addition, the physical dimensions (length and width) of this etch must be controlled to reduce the effects of temperature on the overall gain specification of the ADAM-826-3. For example, for 2 ounce copper-clad pc board, and an etch width of 0.025", the etch will have a dc resistance of 0.010Ω per inch. If we assume a six inch etch length, the total dc resistance of this etch is 0.060Ω. This etch, which forms a resistive divider with the A/D Converter input impedance, has a temperature coefficient of 0.39%/°C. For a temperature rise of 35°C from 25°C to 60°C, the etch resistance will change by a sufficient amount to cause the gain to change by 0.4 LSB at the 16-bit level. This example illustrates the effects on conversion accuracy of typical pc etch dimensions found in many data acquisition systems. Wherever possible pc etch lengths should be kept as short as absolutely necessary to reduce these errors.

The maximum frequency of the signal at the input to the ADAM-826-3 can be determined by the timing relationships as shown in the Typical Timing Diagram of Figure 13. As shown, the actual conversion requires only 1.5 μs while the last 225 ns is used to complete the internal conversion process and to transfer the resulting data word into the internal data register. As long as the signal does not change during the first 1.5 μs of the conversion cycle, no errors will be introduced from this source.

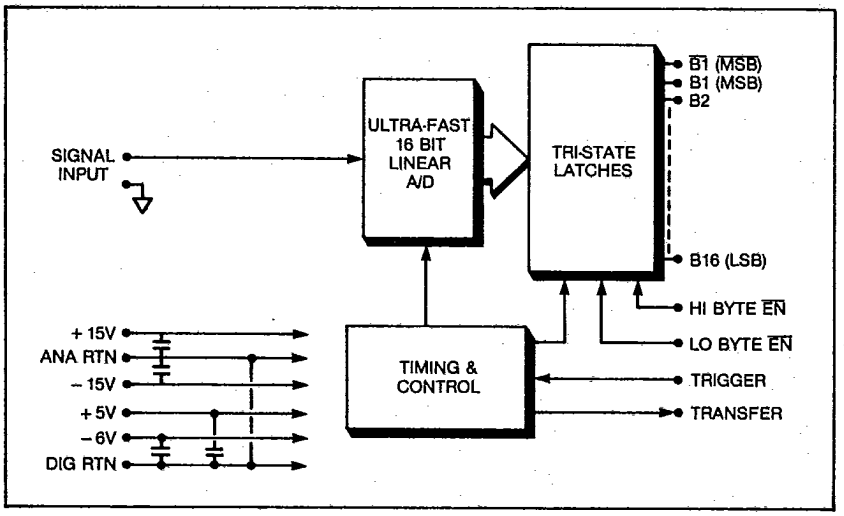


**Figure 12. Block Diagram — ADAM-826-3.**

## SPECIFICATIONS T-51-10-16

(All Specifications are guaranteed at 25°C and nominal power supply voltages unless otherwise noted)

### ANALOG INPUT

**Input Voltage**
0V to +10V Unipolar
−10V to +10V Bipolar
Factory configured

**Input Impedance**
1.4 kΩ Unipolar
2.8 kΩ Bipolar

### ACCURACY

**Resolution**
16-bits

**Differential Non-linearity**
±1/4 LSB typical,
±3/4 LSB maximum

**Monotonicity**
Guaranteed; no missing codes

**Quantization Error**
±1/2 LSB

**Relative Accuracy**
±0.0015% FSR maximum

**Absolute Accuracy**
±0.003% FSR maximum

**Noise (Including Ref.)**
Unipolar: 30 μV rms, maximum
Bipolar: 60 μV rms, maximum

### STABILITY

**Differential Non-linearity Tempco**
±1 ppm/°C maximum

**Offset Tempco**
Unipolar: ±2.5 ppm/°C maximum
Bipolar: ±4.5 ppm/°C maximum

**Gain Tempco**
±5 ppm FSR/°C maximum

**Power Supply Sensitivity Gain**
±10 ppm/Δ1% each supply, maximum

**Offset**
±10 ppm/Δ1% each supply, maximum

**Warmup Time**
10 minutes to specified accuracy

**Recommended Recalibration Interval**
6 months

### THROUGHPUT

**Conversion Time**
1.725 μs maximum

### DIGITAL INPUTS/OUTPUTS

**INPUTS**

**Please refer to ADAM-826-2**

**Trigger**
Negative edge triggered; 1 LSTTL load; 100 ns pulse width minimum, 200 ns maximum; CMOS and 74 LSTTL Compatible

**Tri-state Control**
**HI Byte Enable**
Logic 1 produces high impedance

**LO Byte Enable**
Logic 1 produces high impedance CMOS and 74LSTTL Compatible

### OUTPUTS

**Data**
16 bits data plus B1; Offset Binary or two's complement; See Coding Table; Tri-state CMOS latch (Silicon gate)

**Data Output Loading**
1 LSTTL load

**Transfer (XFER)**
Positive edge loads output data latches; data ready after 50 ns delay

**Transfer (XFER) Loading**
1 LSTTL Load

### POWER REQUIREMENTS

**+15V ±0.5V**
45 mA, typical

**−15V ±0.5V**
70 mA, typical

**+5V ±0.25V**
95 mA, typical

**−6V ±0.25V**
140 mA, typical (See Note 2.)

**Note:**
At power on, a 200 mA maximum current surge on the ±15V supply lines will occur, and will last for no more than 5 seconds. This surge is caused by the Reference heater circuit when starting "cold".

**Note:**
The ±15V power supplies must have no more than 5 mV p-p ripple.

### ENVIRONMENTAL AND MECHANICAL

**Operating Temperature Range**
0°C to +60°C

**Storage Temperature Range**
−25°C to +60°C

**Relative Humidity**
0 to 85%, non condensing

**Dimensions and Shielding Modupac®**
3.00" x 5.00" x 0.44"
(76.2 x 127.0 x 11.17 mm)
RFI 6 sides, EMI 5 sides

**Note 1:** Time for internal reference heater to stabilize.

**Note 2:** −6V may be readily derived from the −15V power supply using a 7906-type three-terminal regulator. See Figure 1.

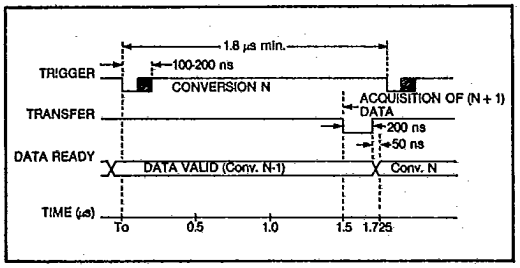


**Figure 13. Typical Timing — ADAM-826-3.**

T-51-10-16

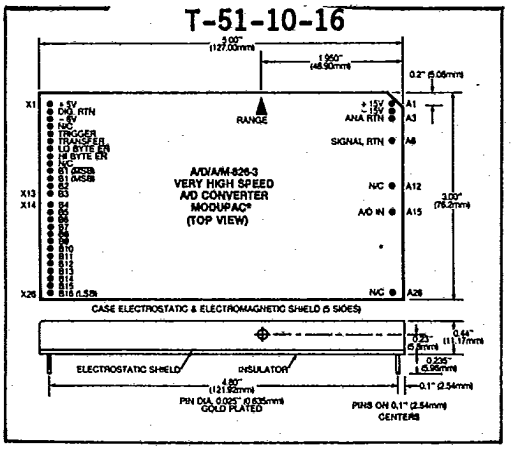


**Figure 14. ADAM-826-3 Mechanical & Pinout.**