National Semiconductor

PRELIMINARY

T-52-09-00

DM74ALS1242A/DM74ALS1243A Quad Bidirectional Bus Driver

General Description

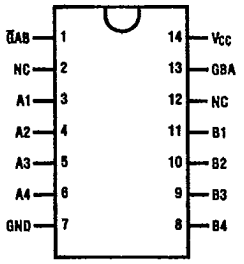
These octal TRI-STATE® bus drivers are designed to provide the designer with flexibility in implementing a bus interface with memory, microprocessor, or communication systems, and are low power dissipation versions of the 'ALS242 and 'ALS243. The 'ALS1242 has inverting buffers, while the 'ALS1243A has non-inverting buffers. The direction enable gating is configured with separate control over either buffer direction and the two control buffers are complementary. Connecting these control inputs to one common line implements single line direction control, while individual control can put both buffer directions into TRI-STATE simultaneously (disabled state) or put both buffer directions into the active state (data latch state). The TRI-STATE circuitry contains a feature that maintains the buffer outputs in TRI-STATE (high impedance state) during power supply ramp-up or ramp-down. This eliminates bus glitching problems that arise during power-up and power-down.

Features

- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Switching response specified into 500Ω and 50 pF load
- Switching response specifications guaranteed over full temperature and V_{CC} supply range
- PNP input design reduces input loading
- Low power dissipation version of the DM54/74ALS242, 243
- Low level drive current: 74ALS = 16 mA

Connection Diagram

Dual-In-Line Package



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Top View

Order Number DM74ALS1242AM, DM74ALS1243AM, DM74ALS1242AN or DM74ALS1243AN
See NS Package Number M14A or N14A

Function Table

Inputs		ALS1242A	ALS1243A
$\overline{G}AB$	GBA		
L	L	$\overline{A}$ to B	A to B
H	H	$\overline{B}$ to A	B to A
H	L	Isolation	Isolation
L	H	Latch A and B ($A = \overline{B}$)	Latch A and B ($A = B$)

This document contains information on a product under development. NSC reserves the right to change or discontinue this product without notice.

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Absolute Maximum Ratings

Supply Voltage, V_{CC}	7V
Input Voltage	
Dedicated Inputs	7V
I/O Ports	5.5V
Operating Free Air Temperature Range	
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Typical θ_{JA}	
N Package	78.0°C/W
M Package	111.5°C/W

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM74ALS1242A DM74ALS1243A			Units
		Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−15	mA
I_{OL}	Low Level Output Current			16	mA
T_A	Operating Free-Air Temperature	0		70	°C

Electrical Characteristics over recommended operating free-air temperature (unless otherwise specified)

Symbol	Parameter	Conditions		DM74ALS1242A DM74ALS1243A			Units
				Min	Typ	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V	I_{OH} = −0.4 mA	V_{CC} − 2			V
		V_{CC} = 4.5V	I_{OH} = −3 mA	2.4			V
			I_{OH} = Max	2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	I_{OL} = Max		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_I = 7V (V_I = 5.5V for A or B Ports)				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V, ALS1242 Active Outputs High			8	12	mA
		Active Outputs Low			10	15	mA
		Outputs TRI-STATE			9	14	mA
		V_{CC} = 5.5V, ALS1243 Active Outputs High			9	14	mA
		Active Outputs Low			10	16	mA
		Outputs TRI-STATE			11	17	mA

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'ALS1242A Switching Characteristics

over recommended operating free-air temperature range (see Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R1 = 500Ω, R2 = 500Ω, T_A = Min to Max		Units
			74ALS1242A		
			Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	A or B to B or A	2	12	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A or B to B or A	2	10	ns
t_{PZH}	Output Enable Time to High Level Output	$\overline{G}$AB to B	4	17	ns
t_{PZL}	Output Enable Time to Low Level Output	$\overline{G}$AB to B	5	21	ns
t_{PHZ}	Output Disable Time from High Level Output	$\overline{G}$AB to B	2	10	ns
t_{PLZ}	Output Disable Time from Low Level Output	$\overline{G}$AB to B	2	10	ns
t_{PZH}	Output Enable Time to High Level Output	GBA to A	5	20	ns
t_{PZL}	Output Enable Time to Low Level Output	GBA to A	6	23	ns
t_{PHZ}	Output Disable Time from High Level Output	GBA to A	2	10	ns
t_{PLZ}	Output Disable Time from Low Level Output	GBA to A	2	16	ns

'ALS1243A Switching Characteristics

over recommended operating free-air temperature range (see Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R1 = 500Ω, R2 = 500Ω, T_A = Min to Max		Units
			74ALS1243A		
			Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	A or B to B or A	2	11	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A or B to B or A	2	12	ns
t_{PZH}	Output Enable Time to High Level Output	$\overline{G}$AB to B	4	21	ns
t_{PZL}	Output Enable Time to Low Level Output	$\overline{G}$AB to B	5	21	ns
t_{PHZ}	Output Disable Time from High Level Output	$\overline{G}$AB to B	2	8	ns
t_{PLZ}	Output Disable Time from Low Level Output	$\overline{G}$AB to B	2	12	ns
t_{PZH}	Output Enable Time to High Level Output	GBA to A	5	21	ns
t_{PZL}	Output Enable Time to Low Level Output	GBA to A	6	21	ns
t_{PHZ}	Output Disable Time from High Level Output	GBA to A	2	11	ns
t_{PLZ}	Output Disable Time from Low Level Output	GBA to A	2	16	ns

Logic Diagrams

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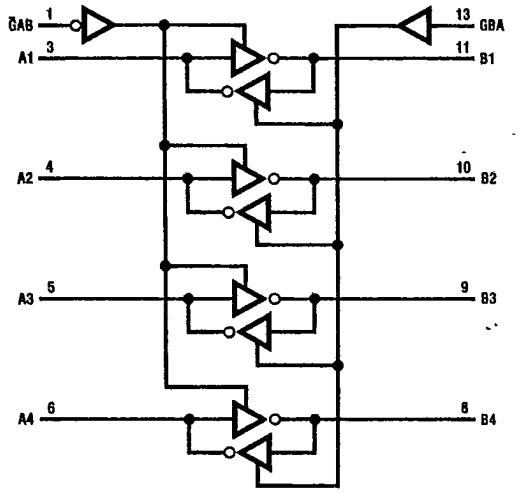
ALS1242A



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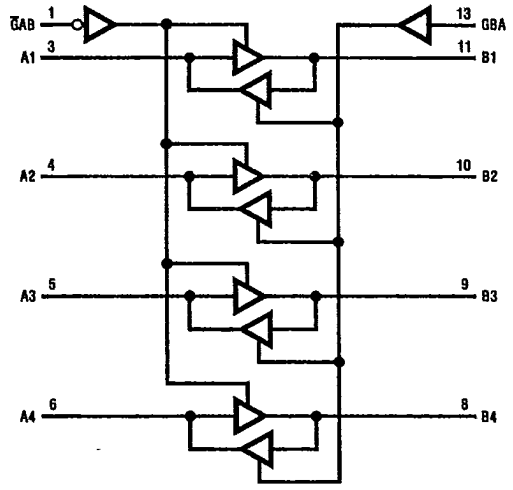
ALS1243A



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