DENSE-PAC MICROSYSTEMS

8 Megabit High Speed CMOS SRAM

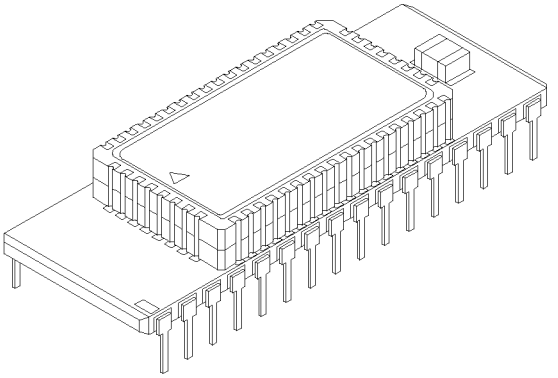
DPS1MX8MKN3

DESCRIPTION:

The DPS1MX8MKN3 High Speed SRAM "STACK" devices are a revolutionary new memory subsystem using Dense-Pac Microsystems' ceramic Stackable Leadless Chip Carriers (SLCC) mounted on a co-fired ceramic substrate having side-brazed leads. The device packs 8-Megabits of low-power CMOS static RAM in a 600-mil-wide, 32-pin dual-in-line package.

The DPS1MX8MKN3 STACK devices contain two 512K x 8 SRAM die, each packaged in a hermetically sealed SLCC, making the devices suitable for commercial, industrial and military applications.

By using SLCCs, the "Stack" family of devices offer a higher board density of memory than available with conventional through-hole, surface mount or hybrid techniques.



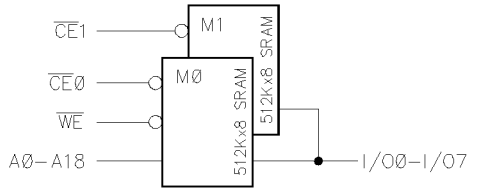
FEATURES:

- Organizations Available: 1Meg x 8
- Access Times:
  20*, 25, 30, 35, 45ns
- Fully Static Operation
  - No clock or refresh required
- Single +5V Power Supply, ±10% Tolerance
- TTL Compatible
- Common Data Inputs and Outputs
- Low Data Retention Voltage: 2.0V min.
- Package Available:
  32 Pin DIP

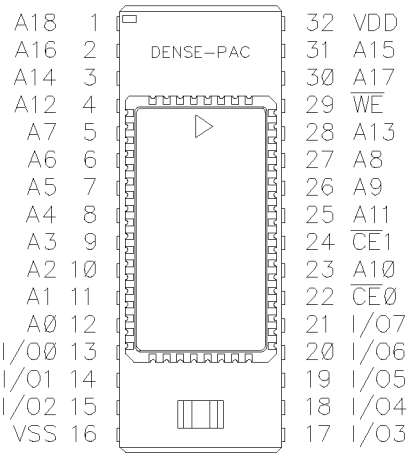
* Commercial and Industrial Grade only.

PIN NAMES	
A0 - A18	Address Inputs
I/O0 - I/O7	Data Input/Output
$\overline{CE0}$, $\overline{CE1}$	Low Chip Enables
$\overline{WE}$	Write Enable
V_{DD}	Power (+5V)
V_{SS}	Ground

FUNCTIONAL BLOCK DIAGRAM



PIN-OUT DIAGRAM



TRUTH TABLE				
Mode	$\overline{CE}$	$\overline{WE}$	I/O Pin	Supply Current
Not Selected	H	X	High-Z	Standby
Read	L	H	D_{OUT}	Active
Write	L	L	D_{IN}	Active

H = HIGH L = LOW X = Don't Care

ABSOLUTE MAXIMUM RATINGS [3]			
Symbol	Parameter	Value	Unit
T_{STC}	Storage Temperature	-65 to +150	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
V_{DD}	Supply Voltage [1]	-0.5 to +7.0	°C
$V_{I/O}$	Input/Output Voltage [1]	-0.5 to V_{DD}+0.5	V

CAPACITANCE [4]: TA = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C_{ADR}	Address Input	18	pF	V_{IN} [2] = 0V
C_{CE}	Chip Enable	12		
C_{WE}	Write Enable	18		
$C_{I/O}$	Data Input/Output	22		

DC OUTPUT CHARACTERISTICS					
Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{OH}	HIGH Voltage	I_{OH} = -4.0mA	2.4		V
V_{OL}	LOW Voltage	I_{OL} = 8.0mA		0.4	V

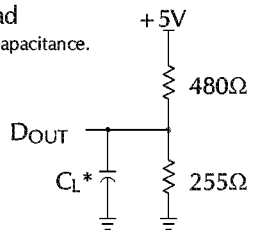
RECOMMENDED OPERATING RANGE [3]						
Symbol	Characteristic		Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage		2.2		V_{DD}+0.3	V
V_{IL}	Input LOW Voltage		-0.5[2]		0.8	V
T_A	Operating Temperature	M/B	-55	+25	+125	°C
		I	-40	+25	+85	
		C	0	+25	+70	

AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V

OUTPUT LOAD		
Load	C_L	Parameters Measured
1	100pF	except t_{LZ}, t_{HZ}, and t_{WHZ}
2	5pF	t_{LZ}, t_{HZ}, and t_{WHZ}

Figure 1. Output Load

* Including Probe and Jig Capacitance.



DC OPERATING CHARACTERISTICS: Over operating ranges									
Symbol	Characteristics	Test Conditions	Typ. (†)	C		I		M/B		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
I_{IN}	Input Leakage Current	V_{IN} = 0V to V_{DD}	-	-10	+10	-10	+10	-10	+10	µA
I_{OUT}	Output Leakage Current	$V_{I/O}$ = 0V to V_{DD}, $\overline{CE}$ = V_{IH}, or $\overline{WE}$ = V_{IL}	-	-20	+20	-20	+20	-20	+20	µA
I_{CC}	Operating Supply Current	Cycle = min., Duty = 100% I_{OUT} = 0mA	145		230		240		240	mA
I_{SB1}	Full Standby Supply Current	$V_{IN} \geq V_{DD}$ -0.2V or $V_{IN} \leq V_{SS}$ +0.2V	2		20		20		30	mA
I_{SB2}	Standby Current (TTL)	$\overline{CE}$ = V_{IH}	40		120		120		120	mA
I_{DR3}	Data Retention Supply Current (3.0V)	V_{DR} = 3V, $\overline{CE} \geq V_{DR}$ -0.2V	300		1000		2000		4000	µA
I_{DR2}	Data Retention Supply Current (2.0V)	V_{DR} = 2V, $\overline{CE} \geq V_{DR}$ -0.2V	200		600		1600		3600	µA
V_{OL}	Output Low Voltage	I_{OUT} = 8.0mA	-		0.4		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OUT} = -4.0mA	-	2.4		2.4		2.4		V

† Typical measurements made at +25°C, Cycle = min., V_{DD} = 5.0V.

Data Retention AC Characteristics [8]						
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DR}	V_{DD} for Data Retention	$\overline{CE} \geq V_{DR}$ -0.2V	2.0	-	-	V
V_{CDR}	Chip Disable to Data Retention Time	See Data Retention Waveform	0	-	-	ns
t_R	Operation Recovery Time	See Data Retention Waveform	5	-	-	ms

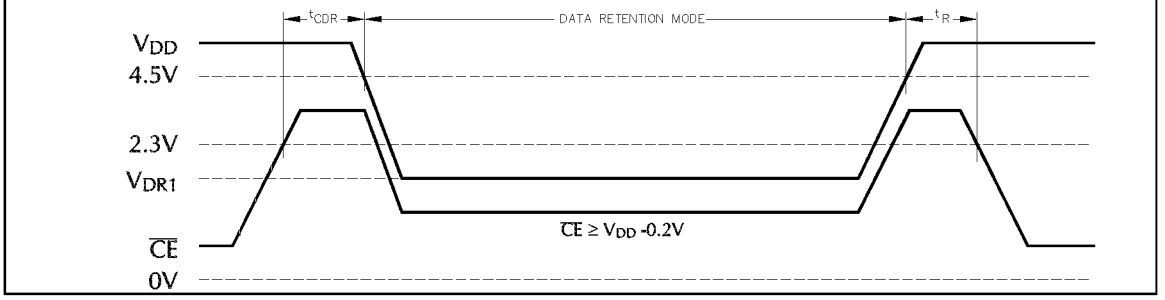
AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges													
No.	Symbol	Parameter	20ns*		25ns		30ns		35ns		45ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	20		25		30		35		45		ns
2	t_{AA}	Address Access Time		20		25		30		35		45	ns
3	t_{CO}	$\overline{CE}$ to Output Valid		20		25		30		35		45	ns
4	t_{LZ}	$\overline{CE}$ to Output in LOW-Z [4, 5]	3		3		3		3		3		ns
5	t_{HZ}	$\overline{CE}$ to Output in HIGH-Z [4, 5]		8		10		15		20		25	ns
6	t_{OH}	Output Hold from Address Change	4		5		5		5		5		ns

AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE [6, 7]: Over operating ranges													
No.	Symbol	Parameter	20ns*		25ns		30ns		35ns		45ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
7	t_{WC}	Write Cycle Time	20		25		30		35		45		ns
8	t_{AW}	Address Valid to End of Write	13		15		20		25		35		ns
9	t_{CW}	Chip Enable to End of Write	13		15		20		25		35		ns
10	t_{AS}	Address Set-Up Time **	0		0		0		0		0		ns
11	t_{WP}	Write Pulse Width	13		15		20		25		35		ns
12	t_{WR}	Write Recovery Time	0		0		0		0		0		ns
13	t_{WHZ}	Write Enable to Output in HIGH-Z [4, 5]	0	8	0	10	0	12	0	15	0	20	ns
14	t_{DW}	Data to Write Time Overlap	9		10		12		15		20		ns
15	t_{DH}	Data Hold from Write Time	0		0		0		0		0		ns
16	t_{OW}	Output Active from End of Write	3		3		3		3		3		ns

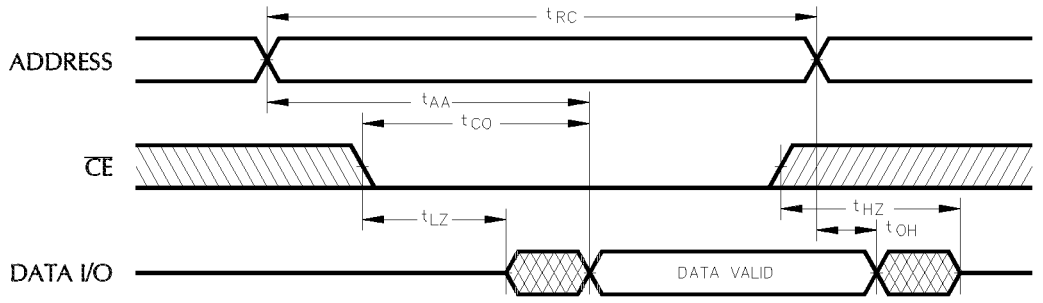
* Available in Commercial and Industrial Grade Only.

** Valid for both Read and Write Cycles.

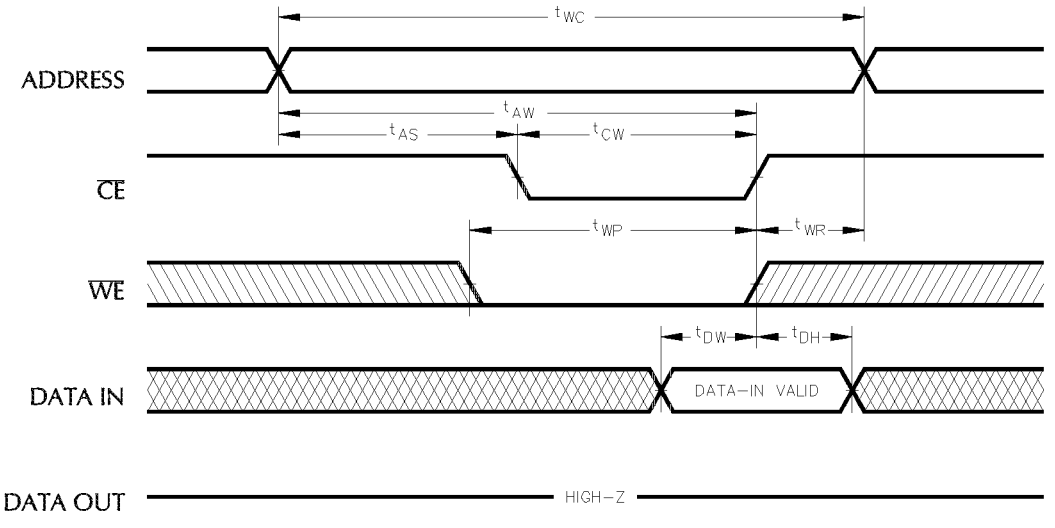
DATA RETENTION WAVEFORM: $\overline{CE}$ Controlled.



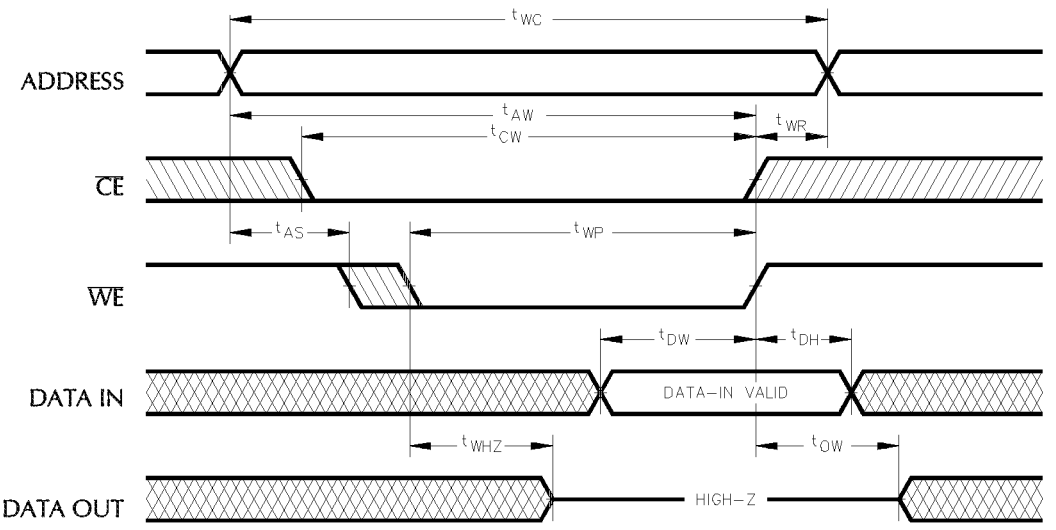
READ CYCLE



WRITE CYCLE 1: $\overline{CE}$ Controlled.



WRITE CYCLE 2: $\overline{WE}$ Controlled. [8]



NOTES:

1. All voltages are with respect to V_{SS}.
2. -2.0V min. for pulse width less than 20ns (V_{IL} min. = -0.5V at DC level).
3. Stresses greater than those under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guaranteed and not 100% tested.
5. Transition is measured at the point of ±500mV from steady state voltage.
6. When $\overline{CE}$ is LOW and $\overline{WE}$ is HIGH, I/O pins are in the output state,and input signals of opposite phase to the outputs must not be applied.
7. The outputs are in a high impedance state when $\overline{WE}$ is LOW.
8. $\overline{CE}$ and $\overline{WE}$ can initiate and terminate WRITE Cycle.

WAVEFORM KEY

Data Valid	Transition from HIGH to LOW	Transition from LOW to HIGH	Data Undefined or Don't Care

ORDERING INFORMATION

DP S 1M X 8 MK N3 – XX X

PREFIX		
TYPE		
MEMORY DEPTH		
DESIG		
MEMORY WIDTH		
DESIG.		
PACKAGE		
SPEED		
GRADE		

GRADE:
- C COMMERCIAL 0°C to +70°C
- I INDUSTRIAL −40°C to +85°C
- M MILITARY −55°C to +125°C
- B MIL−PROCESSED −55°C to +125°C

SPEED:
- 20 20ns ("C" & " I" GRADE ONLY)
- 25 25ns
- 30 30ns
- 35 35ns
- 45 45ns

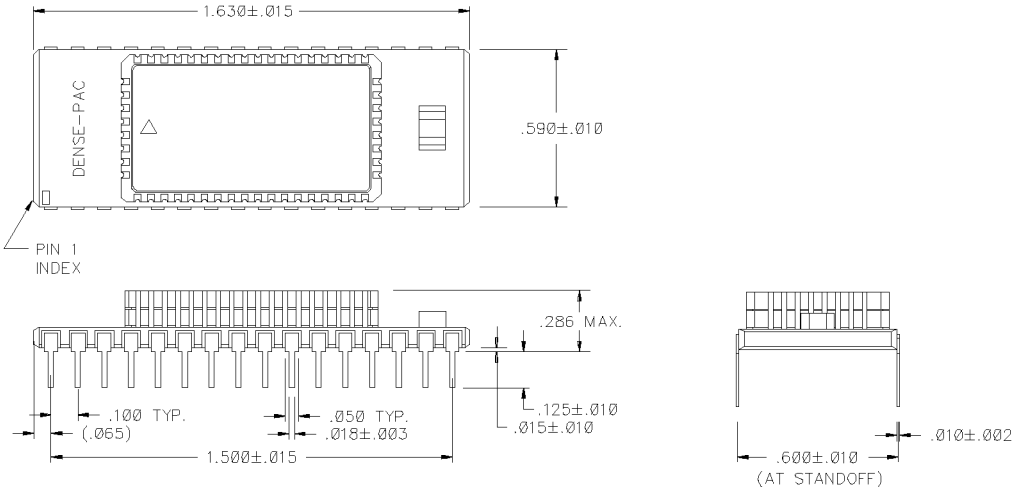
PACKAGE: CERAMIC DIP WITH STACK DEVICE

DESIG.: 4 MEGABIT BASED / 52−PIN PACKAGE

MEMORY WIDTH: MODULE WITHOUT SUPPORT LOGIC

TYPE: CMOS SRAM DEVICES

MECHANICAL DRAWING



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