MV65401/2/3/4

64-WORD x 4/5-BIT FIRST-IN FIRST-OUT MEMORIES

(SUPERSEDES MARCH 1987 EDITION)

The MV65401/2/3/4 are asynchronous first-in first-out memories, organised as 64 by 4 or 5-bit words. Each device accepts a 4/5-bit parallel word, D0 - D4, under control of the shift in (SI) input. Multiple devices can be used to satisfy wider data requirements. Data entered into the FIFO ripples through the device to the outputs Q0 - Q4. Up to 64 words may be entered before any words are read from the memory. The stored words stack up at the output in the order in which they were entered.

Activating the shift out control (SO) causes the next to the last word of data to move to the output and all data shifts one place down the stack. Input ready (IR) and output ready (OR) signals respectively indicate that the device can accept new data or that the output contains valid data. If the input ready output remains inactive, the device is full. If the output ready signal remains inactive, the device is empty.

Since reading and writing operations are completely independent, the device can be used as a buffer between two digital systems operating asynchronously and with widely differing clock frequencies.

The MV65401/2 are respectively four and five bit devices with TTL compatible outputs. The MV65403/4 have the additional feature of tri-state outputs.

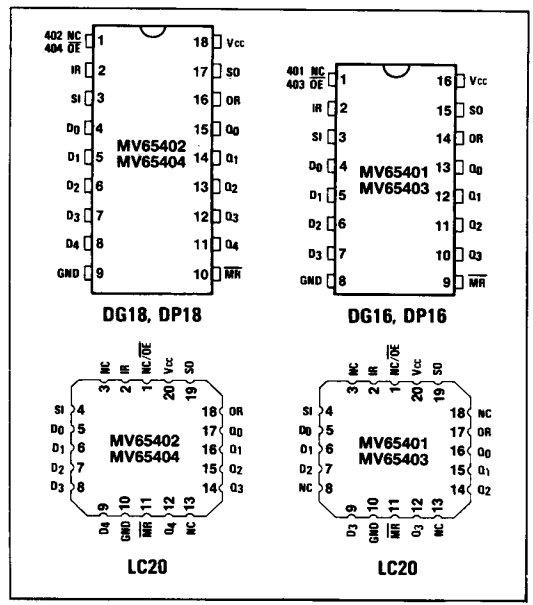

Fig.1 Pin connections - top view

- 35MHz Guaranteed Data Rate, 40MHz Typical (MV65401/2/3/4-35)
- < 200mW at 40MHz
- < 55mW Standby
- Operating Temperature Range:
  -40°C to +85°C Industrial
  -55°C to +125°C Military
- Single 5V Supply, ±10% Tolerance
- Tri-State Outputs on the MV65403/4

APPLICATIONS

- Asynchronous Buffer between Digital Systems
- I/O Formatting in DSP Systems
- Video Time Base Correction
- Printer Buffers
- Disk or Tape Interfaces

ASSOCIATED PRODUCTS

MV66401/2/3/4 64 by 4/5, Bistate/Tristate Cascadable FIFOs
MV66030 64 by 9, Tristate Cascadable FIFO
MV65030 64 by 9, Tristate Stand-alone FIFO
MV61901/2/3 1K by 9 FIFOs

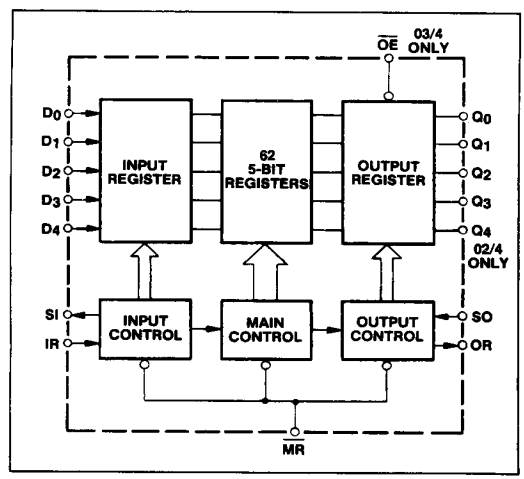

Fig.2 Block diagram

FIFO OPERATION

The MV65401/2/3/4 FIFOs contain 64 four or five bit data registers. Data is initially loaded from the data inputs D0 - D4 by applying a low to high transition on the shift in (SI) input. IR goes low indicating that data has been entered into the first data register and the input is now 'busy' unable to accept more data. When SI next goes low the fall-through process begins, (assuming that at least the second location is empty). The data in the first register is copied into the second and the IR goes high indicating the inputs are available for another data word.

The data falling through the registers stacks up at the output end. A high on OR indicates there is valid data on the data outputs Q0 - Q4. A shift out (SO) can then be used to shift the data out of the FIFO. A low to high transition on SO causes OR to go low, indicating that the data on the outputs may no longer be valid. When SO goes low, the data in the next to last register position moves into the last register position and on to the outputs. If the memory is emptied by reading out all of the data, then, when the last word is being read out and SO goes high, OR will go low as before. When SO next goes low however, there is no data to move into the last location so OR will remain low until more data is entered. Similarly, when the memory is full, data written into the first location will not shift into the second when SI goes low, and IR will remain low instead of returning to a high state.

The data word can be extended in width by using more than one FIFO as shown in Fig.10. The status flags must be gated as shown to allow for possible delay variations between devices.

An overriding master reset ($\overline{MR}$) is used to reset all control register bits and remove the data from the output (i.e. reset the output to all low).

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	-0.5V to 7.0V
Input voltage V_{IN} (see Note 3)	-0.9V to V_{CC} +0.9V
DC voltage applied to output when high impedance	-0.5V to 7.0V
Clamp diode current per pin (see Note 2)	+18mA
Storage temperature T_S	-65°C to +150°C
Ambient temperature with power applied T_{amb}	-55°C to +125°C
Package power dissipation DP	450mW
DG	1000mW
LC	1000mW

NOTES
1. Exceeding these ratings may cause permanent damage. Functional operaton under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.
3. Input voltages more negative than -0.9V cause clamp diode current to flow. The maximum negative voltage depends on the source impedance.

RECOMMENDED OPERATING CONDITIONS

Supply voltage V_{CC}	5V ± 10%
Min. input high level V_{IH}	+2V
Max. input low level V_{IL}	+0.8V
Ambient temperature	
Industrial	-40°C to 85°C
Military	-55°C to 125°C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Under Recommended operating conditions

DC Characteristics

Characteristic	Symbol	INDUSTRIAL				MILITARY		Unit	Conditions
		MV6540X-25		MV6540X-35					
		Min.	Max.	Min.	Max.	Min.	Max.		
Output high level $V_{IN} = V_{IH}$ or V_{IL}, $I_{OH} = -1mA$	V_{OH}	2.4		2.4				V	
Output low level $V_{IN} = V_{IH}$ or V_{IL}, $I_{OL} = 8mA$	V_{OL}		0.5		0.5			V	
Input leakage $V_{IN} = V_{IH}$ or V_{IL}	I_{IN}	-10	+10	-10	+10			μA	
Output leakage GND ≤ V_{OUT} ≤ V_{CC} $V_{CC} = V_{CC}$ max.	I_{OZ}	-50	+50	-50	+50			μA	
Short circuit current	I_{OS}		80		80			mA	Note 2
Supply current	I_{CC}		30		40			mA	V_{CC} = max. T_{amb} = 85°C I_{LOAD} = 0mA
Standby current			10		10			mA	V_{CC} = max. I_{LOAD} = 0mA All inputs at V_{IL}

AC Characteristics - Using test circuit

Characteristic	Symbol	INDUSTRIAL				MILITARY		Unit	Condition
		MV6540X-25		MV6540X-35					
		Min.	Max.	Min.	Max.	Min.	Max.		
Maximum operating frequency	f_O	25		35				MHz	Note 4
SI HIGH time	t_{PHSI}	15		10				ns	
SI LOW time	t_{PLSI}	20		15				ns	
Data setup to SI	t_{SSI}	0		0				ns	Note 5
Data hold from SI	$t_{HSI\ (a)}$	30		20				ns	Note 5,6
	$t_{HSI\ (b)}$	t_{PHSI} +5		t_{PHSI} +5				ns	
Delay, SI HIGH to IR LOW	t_{DLIR}		21		15			ns	
Delay, SI LOW to IR HIGH	t_{DHIR}		25		18			ns	
SO HIGH time	t_{PHSO}	15		8				ns	
SO LOW time	t_{PLSO}	20		15				ns	
Delay, SO HIGH to OR LOW	t_{DLOR}		21		15			ns	
Delay, SO LOW to OR HIGH	t_{DHOR}		25		20			ns	
Data setup to OR HIGH	t_{SOR}	-15		-12				ns	
Data hold from SO LOW	t_{HSO}	8		5				ns	
Bubble through time	t_{BT}		1200		1000			ns	
$\overline{MR}$ pulse width	t_{PMR}	50		30				ns	
$\overline{MR}$ HIGH to SI HIGH	t_{DSI}	50		30				ns	
$\overline{MR}$ LOW to OR LOW	t_{DOR}		50		30			ns	
$\overline{MR}$ LOW to IR HIGH	t_{DIR}		50		30			ns	
$\overline{MR}$ LOW to output LOW	t_{LZMR}		50		30			ns	Note 7
Output valid from $\overline{OE}$ LOW	t_{OOE}		40		28			ns	
Output HIGH-Z from $\overline{OE}$ HIGH	t_{HZOE}		40		28			ns	

NOTES
4. $1/f_O > t_{PHSI} + t_{DHIR}$, $1/f_O > t_{PHSO} = t_{DHOR}$.
5. t_{SSI} and t_{HSI} apply when memory is not full.
6. Hold time is the lesser of the two parameters (a) and (b).
7. All data outputs will be at LOW level after reset goes high until data is entered into the FIFO.

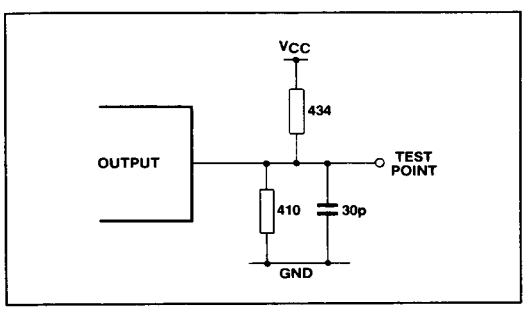

Fig.3 Test circuit

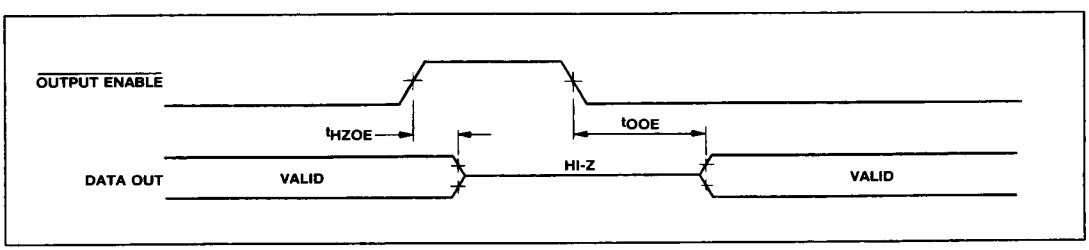

Fig.4 Output enable timing

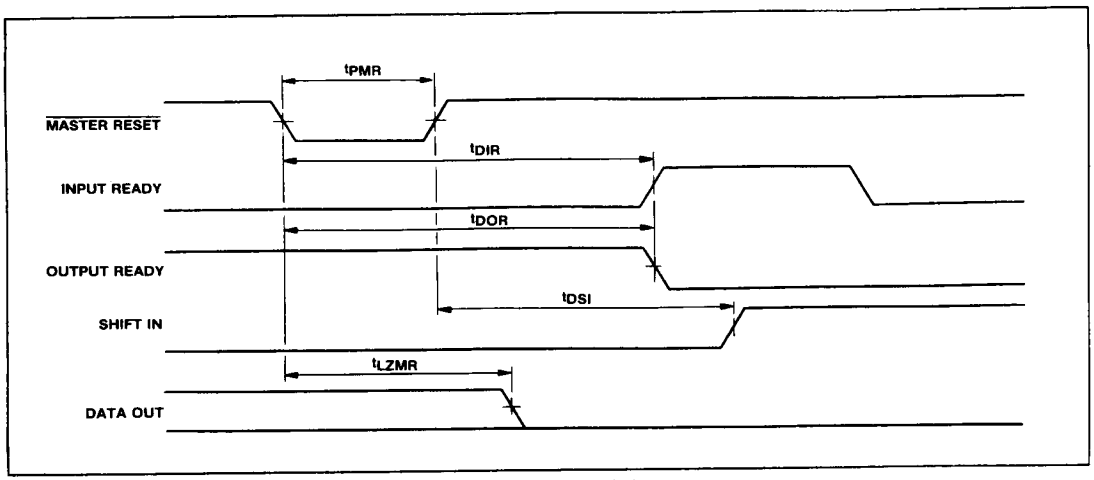

Fig.5 Master reset timing

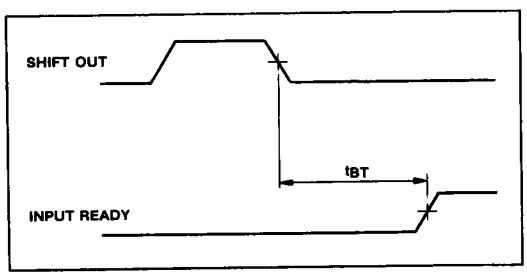

Fig.6 Bubble through time - device full

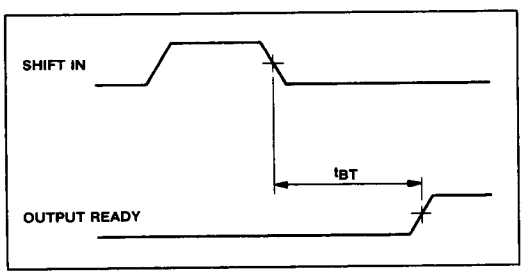

Fig.7 Fall through time - device empty

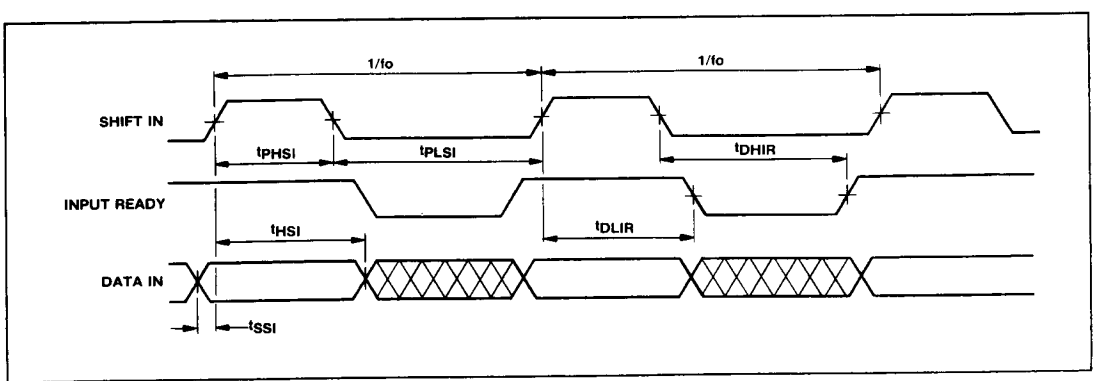

Fig.8 Switching waveforms - Data In timing

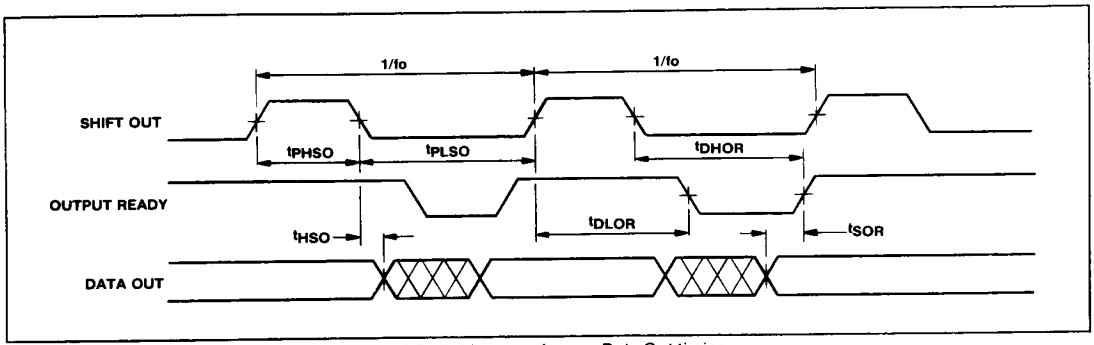

Fig.9 Switching waveforms - Data Out timing

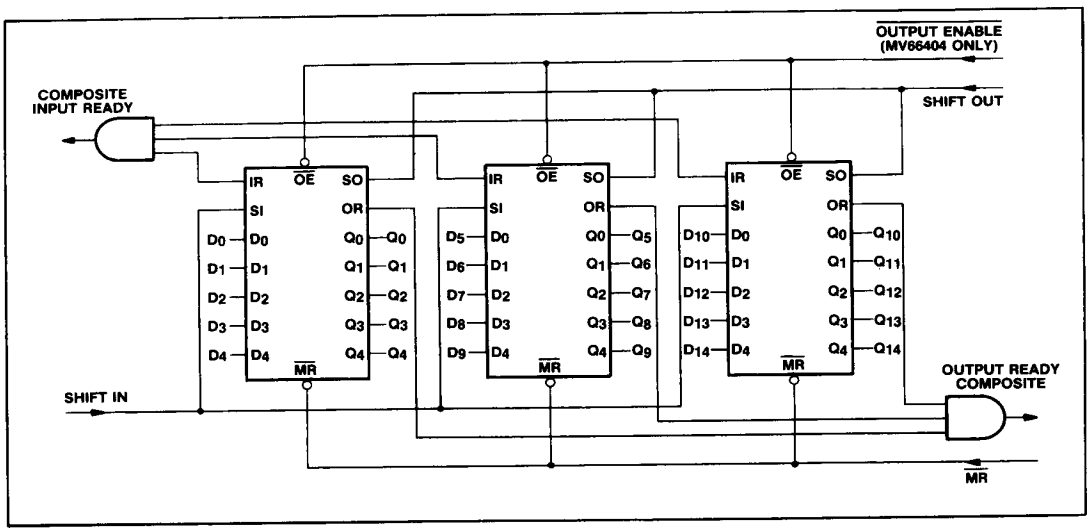

Fig.10 64 x 15 application (MV65402/MV65404)

USER NOTES

1. When the memory is *empty the last word read will remain on the outputs* until the master reset is strobed or a new data word falls through to the output. However, OR will remain LOW, indicating data at the output is not valid.
2. When the output changes as a result of a pulse on SO, the OR signal always goes LOW before there is any change in output data.
3. If SO is held HIGH while the memory is empty and a word is written into the input, that word will ripple through the memory to the output. OR will go HIGH for one internal cycle and then go back LOW again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until SO has been brought LOW.
4. When the master reset is brought LOW, the outputs are cleared to LOW, IR goes HIGH and OR goes LOW. If SI is HIGH when the master reset goes HIGH then the data on the inputs will be written into the memory and IR will return to the LOW state until SI is brought LOW. If SI is LOW when the master reset is ended, the IR will go HIGH, but the data on the inputs will not enter the memory until SI goes HIGH.

TYPICAL CHARACTERISTICS

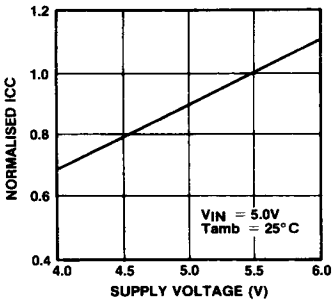

Fig.11 Normalised supply current vs. supply voltage

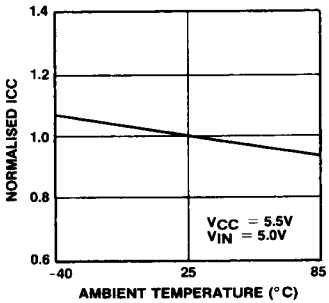

Fig.12 Normalised supply current vs. ambient temperature

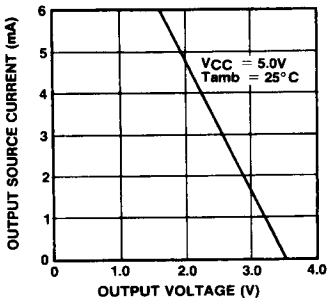

Fig.13 Output source current vs. output voltage

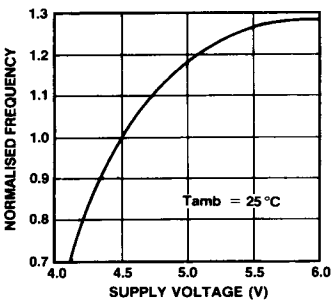

Fig.14 Normalised frequency vs. supply voltage

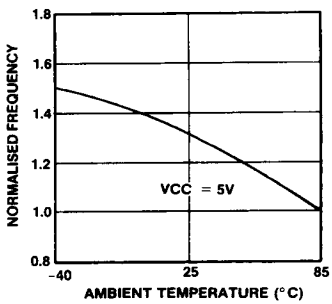

Fig.15 Normalised frequency vs. ambient temperature

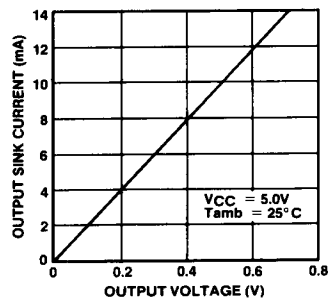

Fig.16 Output sink current vs. output voltage

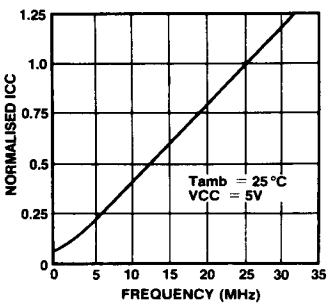

Fig.17 Normalised Icc vs. frequency

ORDERING INFORMATION

Industrial

MV65401-25 B0 DG (Industrial - Ceramic DIL package)
MV65401-35 B0 DG (Industrial - Ceramic DIL package)
MV65402-25 B0 DG (Industrial - Ceramic DIL package)
MV65402-35 B0 DG (Industrial - Ceramic DIL package)
MV65403-25 B0 DG (Industrial - Ceramic DIL package)
MV65403-35 B0 DG (Industrial - Ceramic DIL package)
MV65404-25 B0 DG (Industrial - Ceramic DIL package)
MV65404-35 B0 DG (Industrial - Ceramic DIL package)
MV65401-25 B0 DP (Industrial - Plastic DIL package)
MV65401-35 B0 DP (Industrial - Plastic DIL package)
MV65402-25 B0 DP (Industrial - Plastic DIL package)
MV65402-35 B0 DP (Industrial - Plastic DIL package)
MV65403-25 B0 DP (Industrial - Plastic DIL package)
MV65403-35 B0 DP (Industrial - Plastic DIL package)
MV65404-25 B0 DP (Industrial - Plastic DIL package)
MV65404-35 B0 DP (Industrial - Plastic DIL package)
MV65401-25 B0 LC (Industrial - LCC package)
MV65401-35 B0 LC (Industrial - LCC package)
MV65402-25 B0 LC (Industrial - LCC package)
MV65402-35 B0 LC (Industrial - LCC package)
MV65403-25 B0 LC (Industrial - LCC package)
MV65403-35 B0 LC (Industrial - LCC package)
MV65404-25 B0 LC (Industrial - LCC package)
MV65404-35 B0 LC (Industrial - LCC package)

Military

MV65401 A0 DG (Military - Ceramic DIL package)
MV65402 A0 DG (Military - Ceramic DIL package)
MV65403 A0 DG (Military - Ceramic DIL package)
MV65404 A0 DG (Military - Ceramic DIL package)
MV65401 A0 LC (Military - LCC package)
MV65402 A0 LC (Military - LCC package)
MV65403 A0 LC (Military - LCC package)
MV65404 A0 LC (Military - LCC package)

Call for availability on High Reliability parts and MIL 883C screening.