PAS302BCW-22S CMOS VGA DIGITAL IMAGE SENSOR

General Description

The PAS302BCW-22S is a highly integrated CMOS active-pixel image sensor that has a VGA resolution of 644H x 484V. The PAS302BCW-22S outputs 8-bit RGB raw data through a parallel data bus and is available in 22-pin CSP package.

The PAS302BCW-22S can be programmed to set the exposure time for different luminance condition via I^2C^{TM} serial control bus. By programming the internal register sets, it can perform on-chip frame rate adjustment, offset correction DAC and programmable gain control.

Features

- **VGA(644 x 484 pixels) resolution, ~1/4" Lens**
- **Bayer-RGB color filter array**
- **Output format: 8-bit parallel RGB raw data**
- **On-chip 10-bit pipelined A/D converter**
- **On-chip programmable gain amplifier**
  - **4-bit color gain amplifier (x1~x2)**
  - **4-bit global gain amplifier (x1~x2)**
- **Digital gain stage**
- **Continuous variable frame time(1/2sec~1/30sec)**
- **Continuous variable exposure time**
- **I^2C^{TM} Interface**
- **Support flash light timing**
- **Single 2.5V / 3.3V supply voltage**
- **< 15mA(~30 fps) power dissipation**
- **2μA power dissipation when power down mode**
- **Window-Of-Interest (WOI)**
- **Sub-sampling**
- **Defect compensation**
- **Pin-to-pin compatible to OV7648**

Key Specification

Supply Voltage	2.5V ~ 3.3V
Resolution	644(H) x 484(V)
Array diagonal	4.5mm (~1/4"Optic)
Pixel Size	5.6μmx5.6μm
Chief Ray Angle	20° ~ 22°
Frame rate	~30 fps
System clock	Up to 48 MHz
Pixel clock	Up to 12MHz
Sensitivity	1.56 V/Lux-Sec
Color filter	RGB Bayer Pattern
Exposure Time	~ Frame time to Line time
Scan Mode	Progressive
S/N Ratio	> 45 dB
Package	22-pin lead-free CSP

Note1: Only two decoupling capacitors needed
Note2: Good sensitivity compared to competitors

1. Pin Assignment

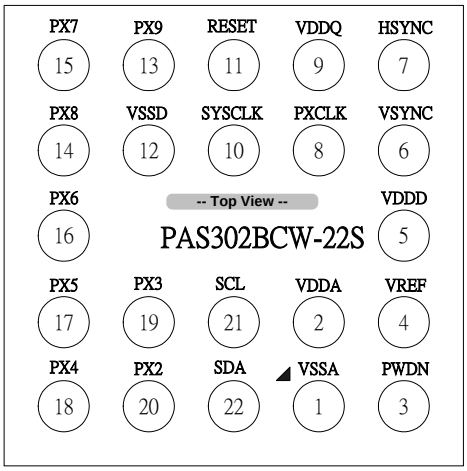


Figure 1.1. PAS302BCW-22S pin assignment

Pin No.	Name	Type	Description
1	VSSA	GND	Analog ground
2	VDDA	PWR	Analog VDD.
3	PWDN	IN	Power Down (chip power down when high)
4	VREF	IN	Internal voltage reference
5	VDDD	PWR	Digital VDD.
6	VSYNC	OUT	Vertical synchronization signal
7	HSYNC	OUT	Horizontal synchronization signal
8	PXCLK	OUT	Pixel clock output
9	VDDQ	PWR	Sensor VDD, 2.5V ~ 3.3V
10	SYSCLK	IN	Master clock input
11	RESET	IN	Resets all registers to their default values (chip reset when high)
12	VSSD	GND	Digital ground
13	PX9	OUT	Digital data out
14	PX8	OUT	Digital data out
15	PX7	OUT	Digital data out
16	PX6	OUT	Digital data out
17	PX5	OUT	Digital data out
18	PX4	OUT	Digital data out
19	PX3	OUT	Digital data out
20	PX2	OUT	Digital data out
21	SCL	IN	I^2C^{TM} clock.
22	SDA	I/O	I^2C^{TM} data. Internal pull high resister is 10KΩ.

2. Block Diagram

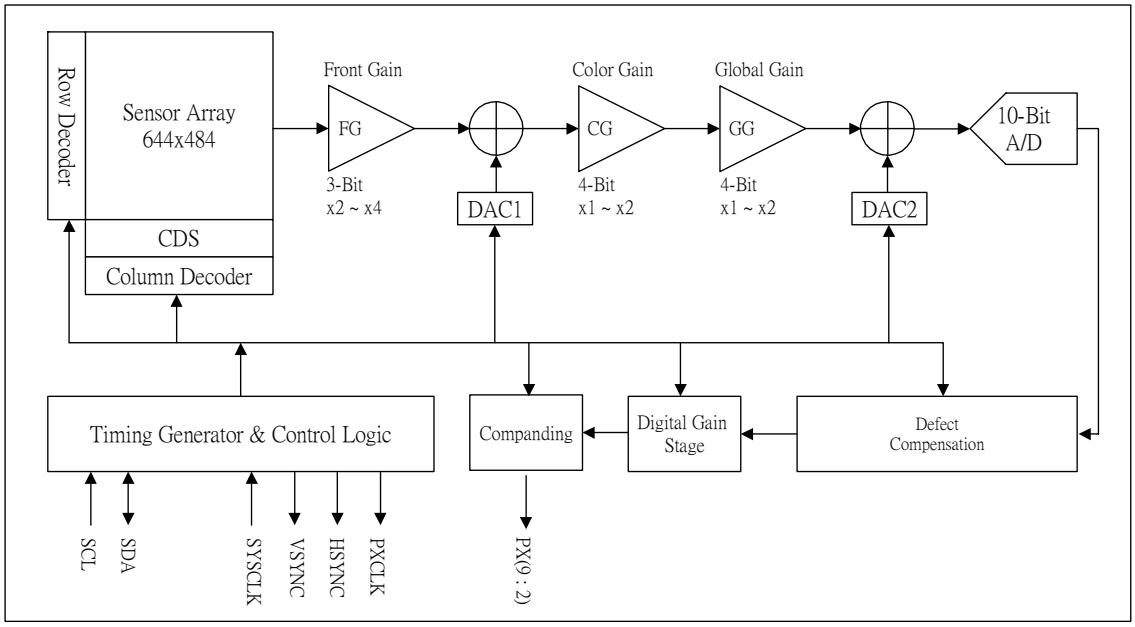


Figure 2.1. PAS302BCW-22S sensor block diagram

The PAS302BCW-22S is a 1/4" CMOS imaging sensor with 644x488 physical pixels. The active region of sensor array is 644x484 as shown in Fig. 2.1. The sensor array is covered with Bayer pattern color filters and micro-lens. The first pixel location <0,0> is programmable in 2 direction (X and Y) and the default value is at the left-down side of sensor array.

After a programmable exposure time, the signals of image are sampled first with CDS (Correlated Double Sampling) block to improve S/N ratio and reduce fixed pattern noise.

Three analog gain stages are implemented before signals are transferred to 10-Bit ADC. The front gain stage (FG) can be programmed to fit the saturation level of sensor to the full-range input of ADC. The programmable color gain stage (CG) is used to balance the luminance response difference between B, G and R color. The global gain stage (GG) is programmed to adapt the gain to the image luminance.

After three gain stages, the signals will be digitized by the on-chip 10-Bit ADC. After the image data have been digitized, further adjustment to the signal can be applied before the data is output to next stage.

3. Function Description

3.1 Defect Compensation

The Defect Compensation block can detect the possible defect pixel and replace it with average output of like-colored pixels from near side of defect pixel. There is no limitation capability of defect pixel number. This function can be programmed to enable/disable by user.

3.2 Companding Curves

The companding function which means compressing and expanding is used to simulate the gamma curve and do non-linear transformation before the data is output. There are 4 curves selected by setting Register Compand_Sel as shown in Fig. 3.1. This function can be programmed to enable/disable by user.

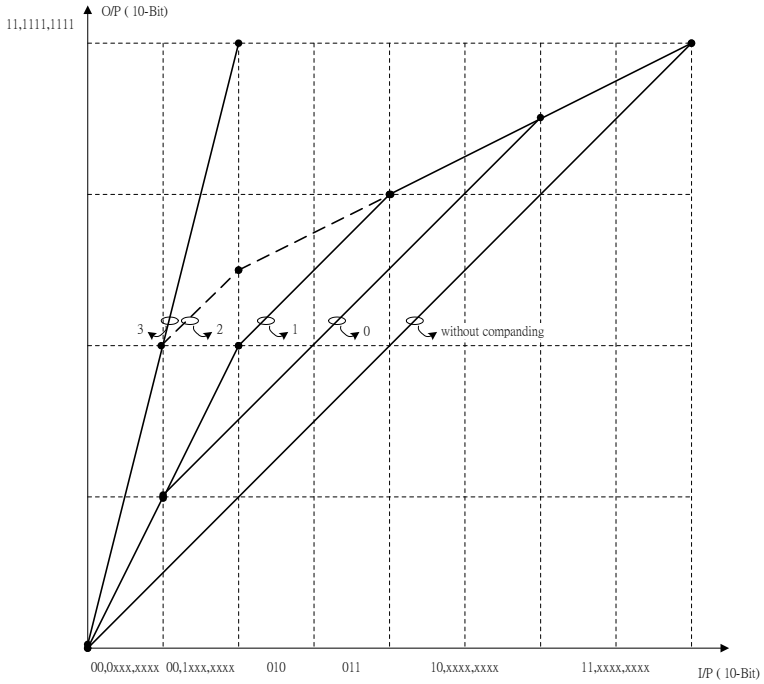


Figure 3.1 Companding curves programmed by Compand_EnH and Compand_Sel.

3.3 Power Down Mode

The PAS302BCW-22S can be powered down by setting register “Sw_PwrDn” = 1 or by enable Pwdn pin. The register value will sustain in the power down mode. PAS302BCW-22S supports 2 power down modes:

- Software power down：Set register “Sw_PwrDn” = 1 to power down all the internal block except I^2C^{TM}.
- Hardware power down：Pull Pwdn pin to high to power down the chip. The chip will go into standby mode.

3.4 Reset Mode

The PAS302BCW-22S can be reseted by setting register “Sw_Reset” = 1 or by enable Reset pin. PAS302BCW-22S supports 2 reset modes:

- Software reset：Set register “Sw_Reset” = 1 to reset all the I^2C^{TM} registers.
- Hardware reset：Pull Reset pin to high to reset the full chip.

4. Output Format

4.1 Physical Sensor Array

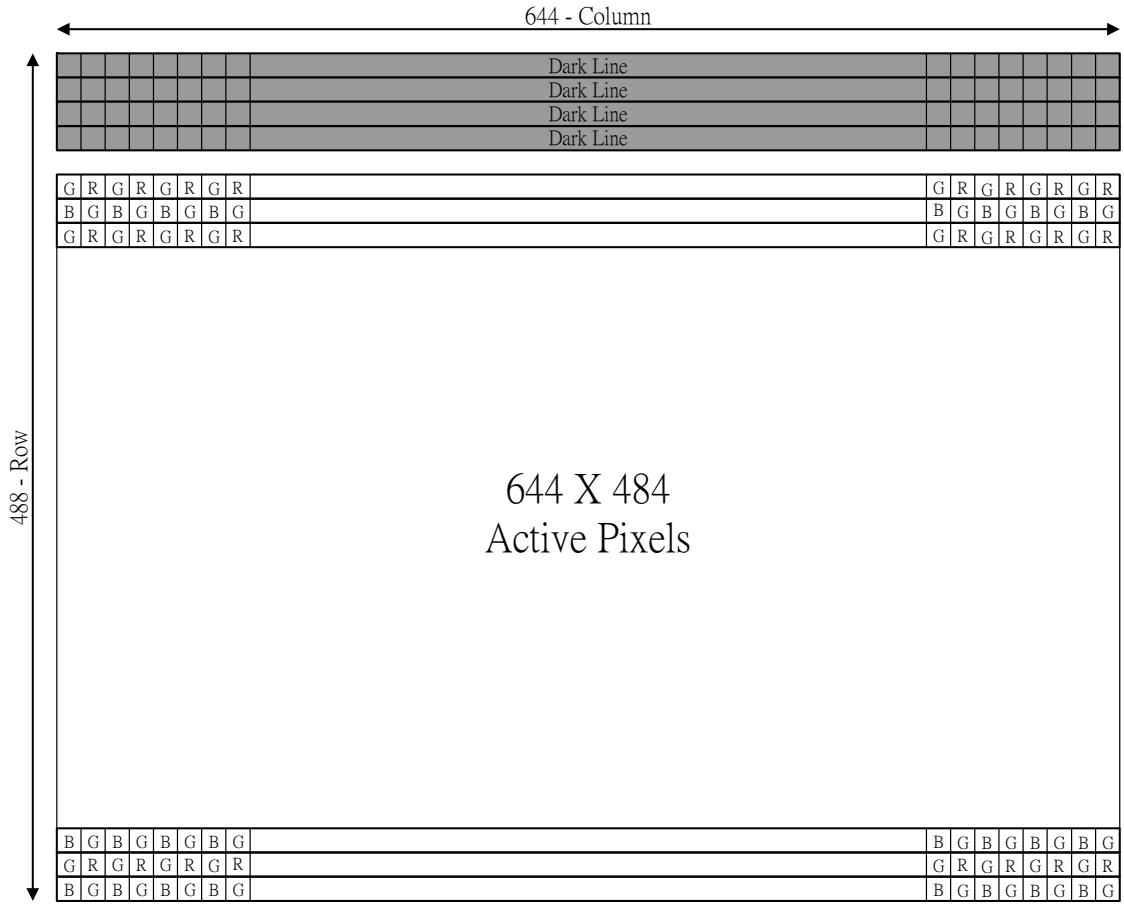


Figure 4.1 Physical Sensor Array

4.2 Output Timing

VGA mode (644 x 488) pixel readout:

H_Start[9:0] = 0, V_Start[8:0] = 0, H_Size[9:0] = 643, V_Size[8:0]= 487, Nov_By2[7:0] = 87,

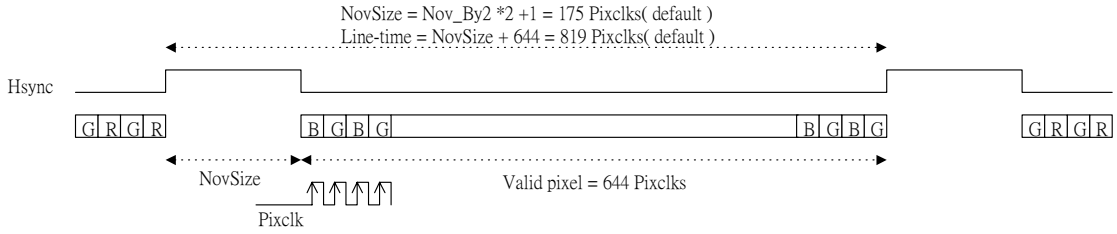


Figure 4.2 Inter-line timing (default)

If Mask_Dark[3] = 0,

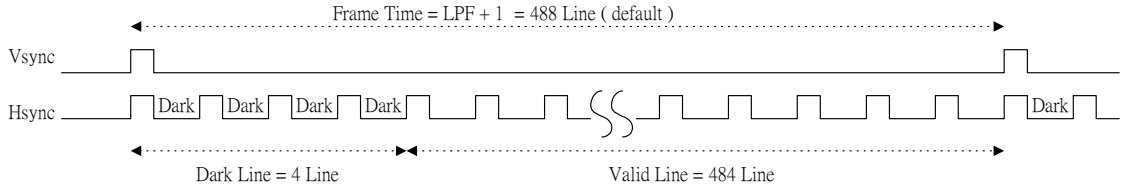


Figure 4.3 Inter-frame timing (LPF default setting = 487, Mask_Dark[3] =0)

If Mask_Dark[3] = 1,

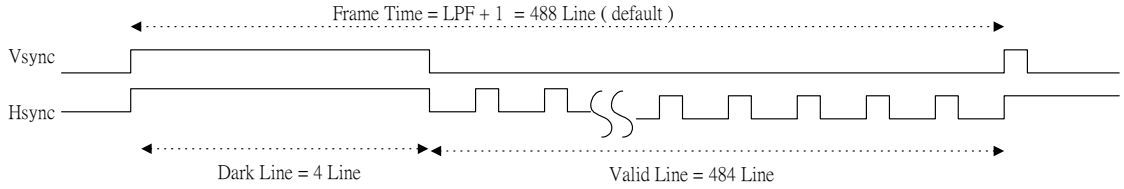


Figure 4.4 Inter-frame timing (LPF default setting = 487, Mask_Dark[3] =1)

4.3 Hardware Windowing

Users are allowed to define window size as well as window location in PAS302BCW-22S, Window size can range from 20x14 to 644x484. The location of window can be anywhere in the sensor array. Window location and size is defined by register H_Start, V_Start, H_Size and V_Size; the H_Start defines the starting column while V_Start defines the starting row of the window; the H_Size define the column width of the window and V_Start define the row depth of the window.

4.4 Sub-sampling

PAS302BCW-22S can be programmed to output image in QVGA and QQVGA size by setting Registers Skip_Digital or Skip_Analog. In QVGA sub-sampling mode, both vertical and horizontal pixels are sub-sampling at 1/2, while in QQVGA sub-sampling mode, both vertical and horizontal pixels are sub-sampling at 1/4. The maximum sub-sampling rate is 1/16.

5. I^2C^{TM} Bus

PAS302BCW-22S supports I^2C^{TM} bus transfer protocol and acts as slave device. The 7 bits unique slave address is 1000000 and the bus supports receiving / transmitting speed up to 400kHz.

5.1 I^2C^{TM} Bus Overview

There are only two lines SDA (serial data) and SCL (serial clock) carry information between the devices which are connected by I^2C^{TM} bus. Normally both SDA and SCL lines are open collector structure and pulled high by external pull-up resistors.
Only the master can initiate a transfer (start), generate clock signals, and terminate a transfer (stop).
Start Condition :
A high to low transition of the SDA line while SCL is high defines a start condition.

Stop Condition :
A low to high transition of the SDA line while SCL is high defines a stop condition.

Valid Data:
The data on the SDA line must be stable during the high period of the SCL clock. Within each byte, MSB is always transferred first. Read/write control bit is the LSB of the first byte.
Both the master and slave can transmit and receive data from the bus.

Acknowledge :
The receiving device should pull down the SDA line during high period of the SCL clock line when a byte was transferred completely by transmitter. When in the case of that a master received data from a slave, the master does not generate an acknowledgment on the last byte to indicate the end of a master read cycle.

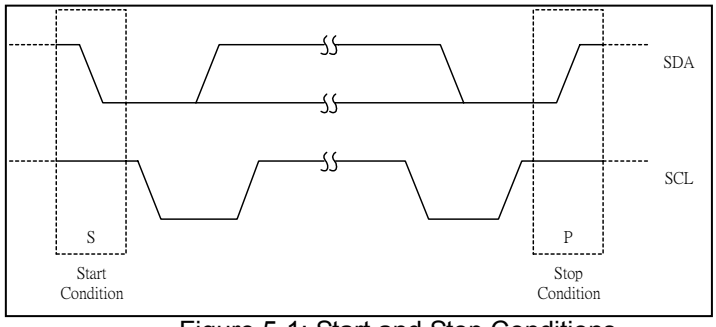


Figure 5-1: Start and Stop Conditions

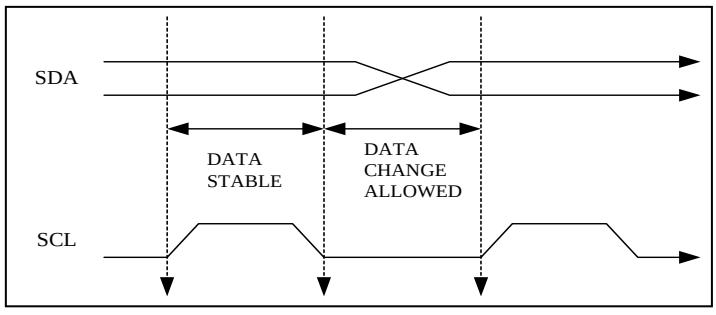
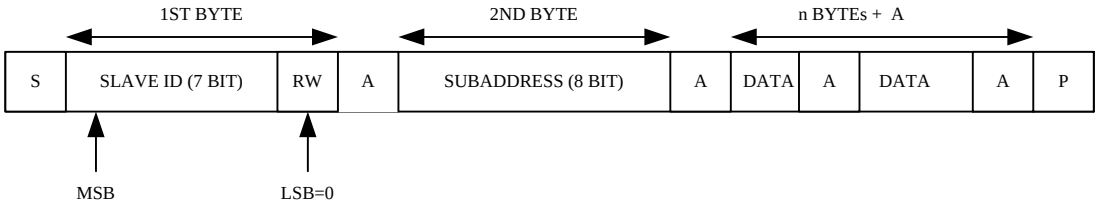


Figure 5-2: Valid Data

5.2 Data Transfer Format

5.2.1 Master transmits data to slave (write cycle)

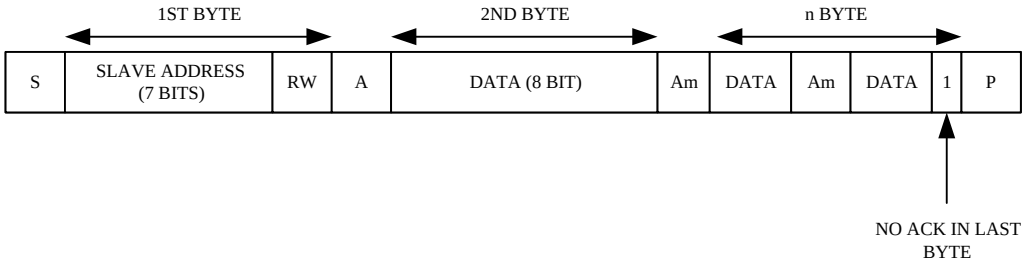
- S : Start
- A : Acknowledge by slave
- P : Stop
- RW : The LSB of 1st byte to decide whether current cycle is read or write cycle. If RW=1 that means read cycle, if RW=0 that means write cycle.
- SUBADDRESS : The address values of PAS302BCW-22S internal control registers (Please refer to PAS302BCW-22S register description)



During the write cycle, the master generates start condition and then places the 1st byte data that combined slave address (7 bits) with a read/write control bit on SDA line. After slave(PAS302BCW-22S) issues acknowledgment, the master places 2nd byte (sub-address) data on SDA line. And then following the slave's(PAS302BCW-22S) acknowledgment, the master places the 8 bits data on SDA line and transmit to PAS302BCW-22S control register (address was assigned by 2nd byte). After PAS302BCW-22S issue acknowledgment, the master can generate a stop condition to end this write cycle. In the condition of multi-byte write, the PAS302BCW-22S sub-address will be increased automatically after each DATA byte has been transferred. The Data and A cycles are repeated until last byte write. Every control registers value inside PAS302BCW-22S can be programming via this way. (Please refer to Figure 5.3.)

5.2.2 Slave transmits data to master (read cycle)

- The sub-address was assigned by previous write cycle
- The sub-address is automatically increased after each byte read
- Am : Acknowledged by master
- Note: there is no acknowledgment from master after last byte read



During read cycle, the master generates start condition and then place the 1st byte data that combine slave address (7 bits) with a read/write control bit to SDA line. After slave issue acknowledgment, 8 bits DATA was placed on SDA line by PAS302BCW-22S. The 8 bit data was read from PAS302BCW-22S internal control register that address was assigned by previous write cycle. Following the master acknowledgment, the PAS302BCW-22S place the next 8 bits data (address is increased automatically) on SDA line and then transfer to master serially. The

DATA and Am cycles are repeated until the last byte read. After last byte read, Am is no longer generated by master but instead of keeping SDA line as high. The slave (PAS302BCW-22S) must releases SDA line back to master to generate STOP condition. (Please refer to Figure 5.3.)

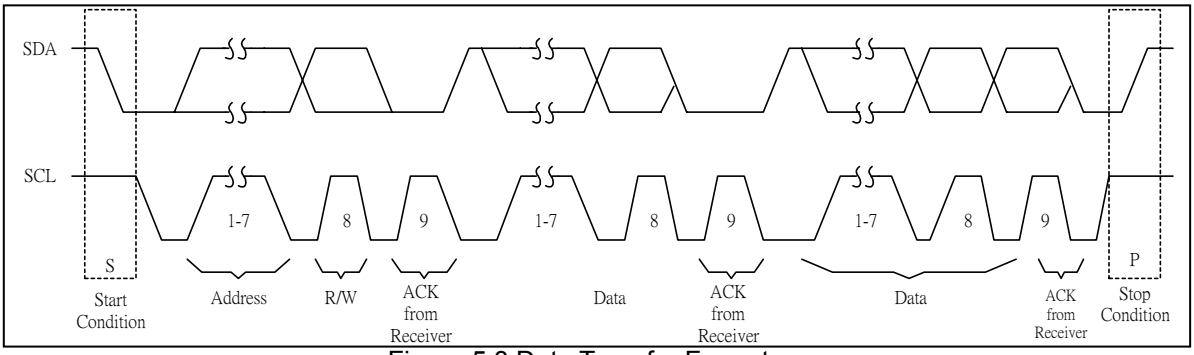


Figure 5.3 Data Transfer Format

5.3 I^2C^{TM} Bus Timing

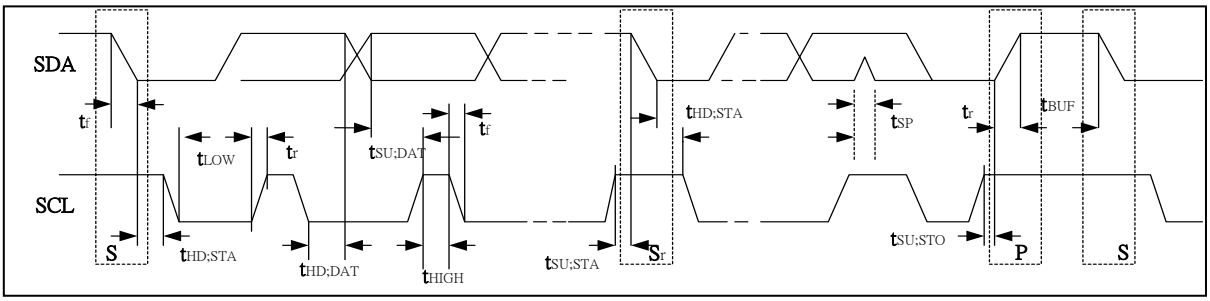


Figure 5.4 I^2C^{TM} Bus Timing

5.4 I^2C^{TM} Bus Timing Specification

PARAMETER	SYMBOL	STANDARD-MODE		UNIT
		MIN.	MAX.	
SCL clock frequency	f_{scl}	10	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	$t_{HD:STA}$	4.0	-	μs
Low period of the SCL clock	t_{LOW}	4.7	-	μs
HIGH period of the SCL clock	t_{HIGH}	0.75	-	μs
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	-	μs
Data hold time. For I^2C^{TM} bus device	$t_{HD;DAT}$	0	3.45	μs
Data set-up time	$t_{SU;DAT}$	250	-	ns
Rise time of both SDA and SCL signals(note)	t_r	30	N.D.	ns
Fall time of both SDA and SCL signals(note)	t_f	30	N.D.	ns
Set-up time for STOP condition	$t_{SU;STO}$	4.0	-	μs
Bus free time between a STOP and START	t_{BUF}	4.7	-	μs
Capacitive load for each bus line	C_b	1	15	pF

Noise margin at LOW level for each connected device (including hysteresis)	V_{nL}	0.1 VDD	-	V
Noise margin at HIGH level for each connected device (including hysteresis)	V_{nH}	0.2 VDD	-	V

Note: It depends on the "high" period time of SCL.

6. Electrical Characteristics

Absolute Maximum Ratings

Ambient Storage Temperature		-40℃ ~ +125℃
Supply Voltages (with respect to Ground)	V_{DDD}	3V
	V_{DDA}	3V
	V_{DDMA}	4V
	V_{DDQ}	4V
All Input / Output Voltages (with respect to Ground)		-0.3V to V_{DDQ} + 1V
Lead Temperature, Surface-mount process		+230℃
ESD Rating, Human Body model		2000V

DC Electrical Characteristics (VDD = 2.5V ± 4% , Ta = 0℃ ~ 70℃)

Symbol	Parameter	Min.	Typ.	Max.	Unit
Type :PWR					
V_{DDA}	DC Supply voltage – Analog	2.4	2.5	2.6	V
V_{DDD}	DC Supply voltage – Digital	2.4	2.5	2.6	V
V_{DDQ}	DC Supply voltage – I/O	2.4	-	3.3	V
I_{DD}	Operating Current		15		mA
I_{PWDN}	Power Down current		2		μA
Type :IN & I/O Reset and SYSCLK					
V_{IH}	Input voltage HIGH	0.7 x V_{DDQ}			V
V_{IL}	Input voltage LOW			0.3 x V_{DDQ}	V
C_{IN}	Input capacitor			10	pF
Type : OUT & I/O for PXD0:7, PXCK, H/VSYNC & SDA, load 10pf, 1.2kΩ,2.5volts					
V_{OH}	Output voltage HIGH	0.9 x V_{DDQ}			V
V_{OL}	Output voltage LOW			0.1 x V_{DDQ}	V

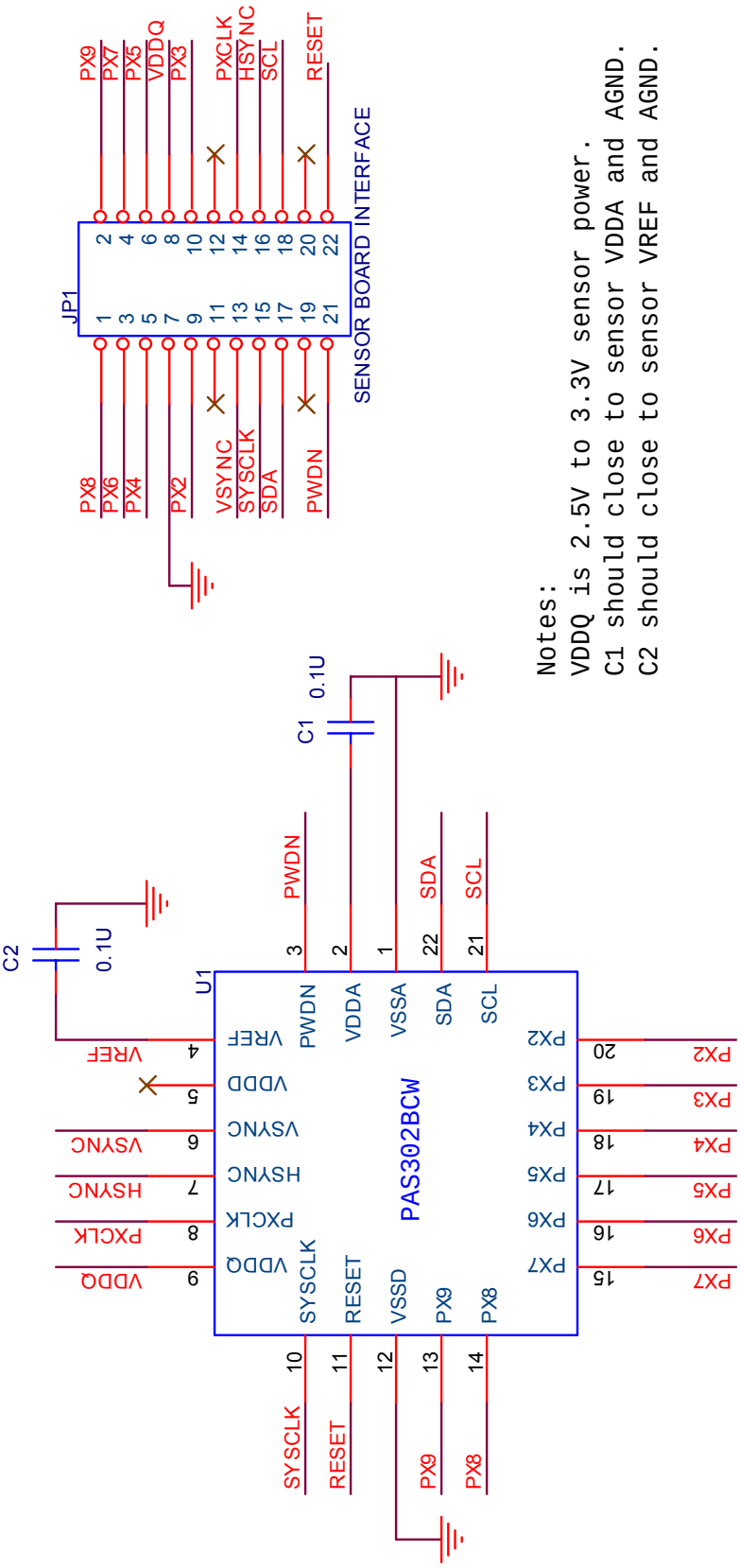
AC Operating Condition

Symbol	Parameter	Min.	Typ.	Max.	Unit
SYSCLK	Master clock frequency			48	MHz
PXCK	Pixel clock output frequency			12	MHz

Sensor Characteristics

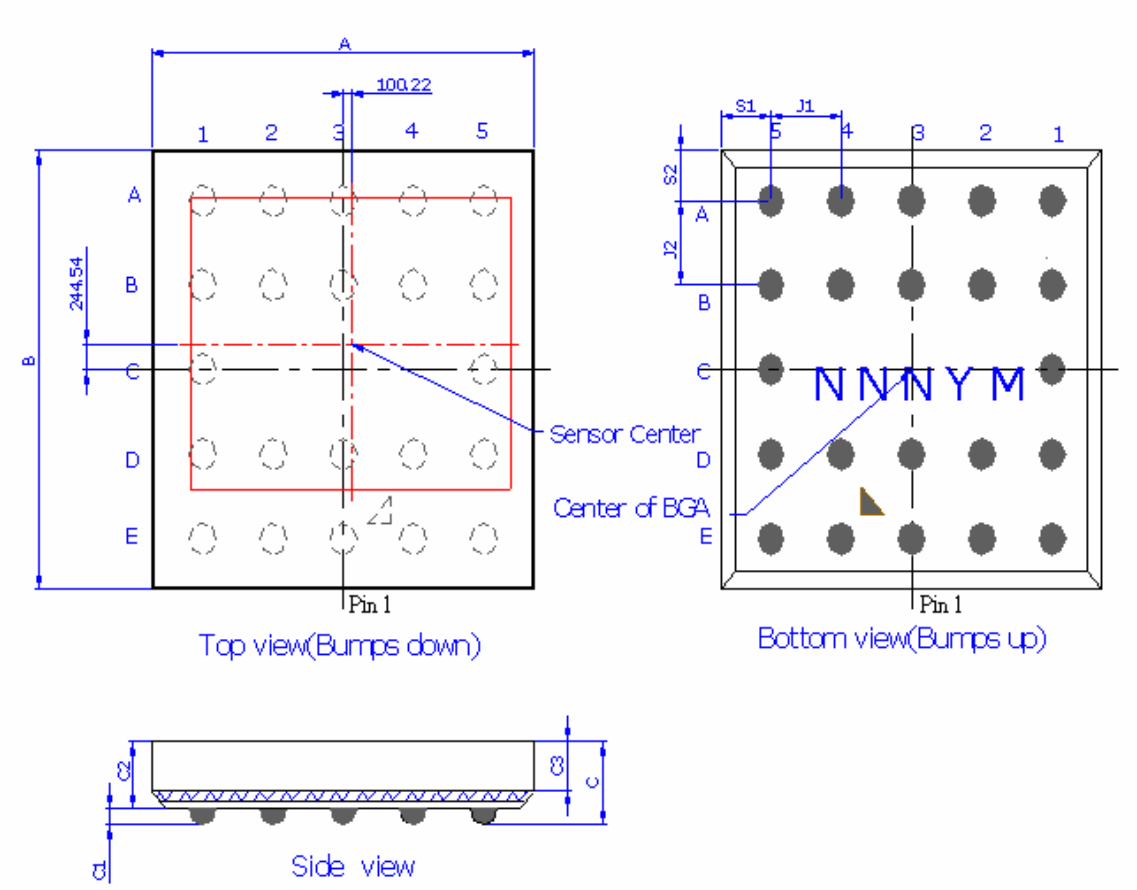
Parameter		Typ.	Unit	Note
Sensitivity		1.56	V/Lux-Sec	
Signal to Noise Ratio		> 45	dB	
Dynamic Range		60	dB	
Temperature Range	Operation	-10 ~ 70	℃	
	Stable Image	0 ~ 50		

7. Reference Circuit Schematic

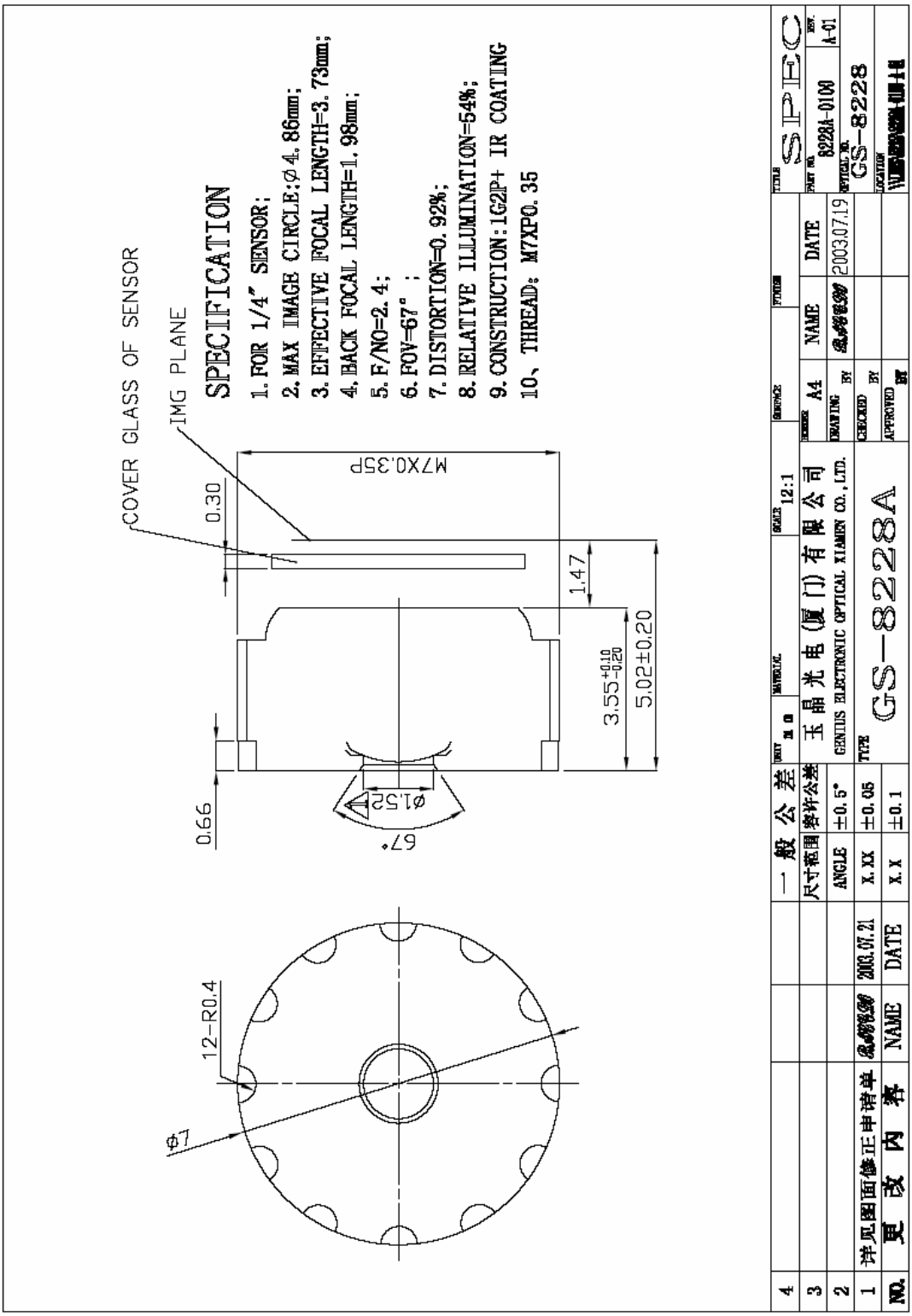


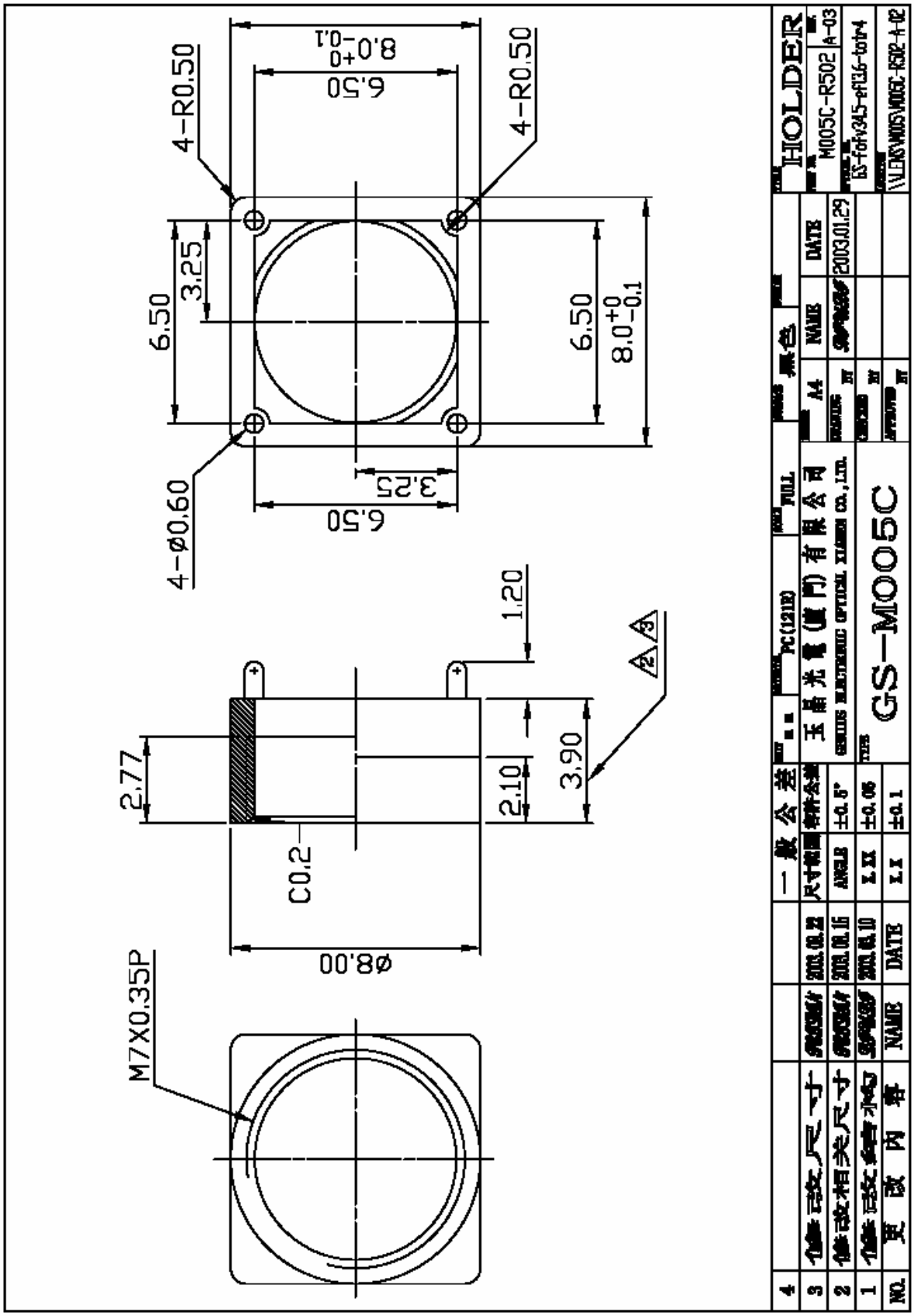
8. Package Specification

Dimensions	Symbol	Min.	Typ.	Max.	Unit
Package Body Dimension X	A	4310	4335	4360	µm
Package Body Dimension Y	B	4130	4155	4180	µm
Package Height	C	740	800	860	µm
Ball Height	C1	130	160	190	µm
Package Body Thickness	C2	605	640	675	µm
Thickness of Glass surface to wafer	C3	395	415	435	µm
Ball Diameter	D	270	300	330	µm
Pin Pitch X axis	J1	-	800	-	µm
Pin Pitch Y axis	J2	-	800	-	µm
Edge to Pin Center Distance along X	S1	537.5	567.5	597.5	µm
Edge to Pin Center Distance along Y	S2	447.5	477.5	507.5	µm



9. Recommended Lens and Holder




4-R0.50
4-R0.50
8.0+0 -0.1
6.50
3.25
6.50
6.50
8.0+0 -0.1
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6.50
4-ø0.60
1.20
2.77
2.10
3.90
C0.2
ø8.00
M7X0.35P
HOLDER
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玉晶光電(廣州)有限公司
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NAME
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