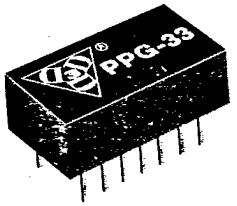
Programmable Pulse Generator

SERIES: PPG-33
(3 Bit) TTL Interfaced

data delay devices, inc.



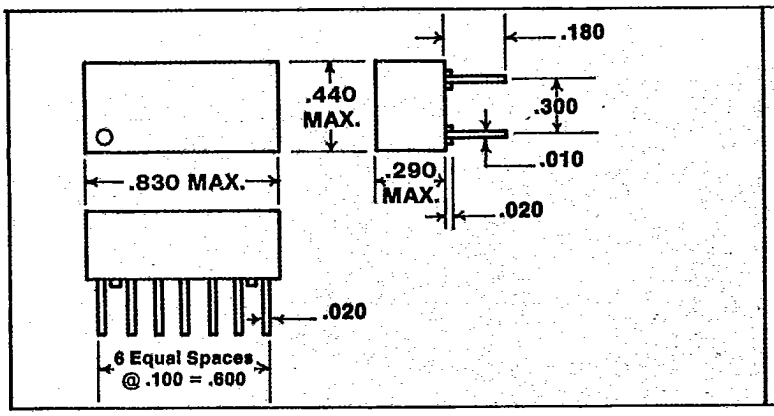
Features:

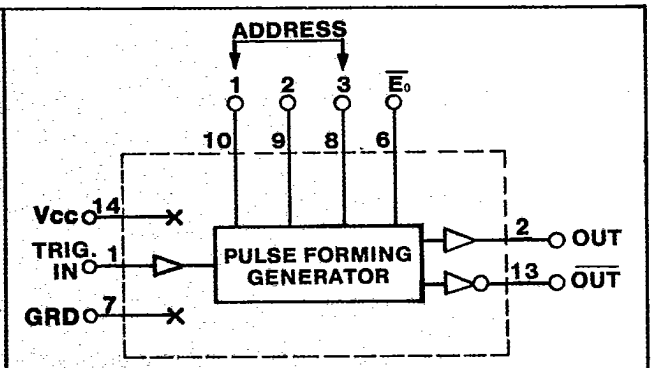
Precise pulse widths

- 3-BIT address
- 1 ns to 50 ns incremental steps
- Trigger inherent delay (T_{DO}) { –8 ns for $\overline{OUT}$ / –6 ns for OUT
- Inherent pulse width (PW_0) –10 ns typ.
- Positive pulse triggered
- 14 pins DIP package
- Low profile

Specifications:

- Input requirements: TTL logic, rising-edge triggered.
- Input pulse width: 6 ns min.
- Output fan-out: TTL Schottky loads.
- Programmed pulse-width tolerance: 5% or 1 ns whichever is greater.
- Supply voltage (Vcc): 5 Vdc ± 5%.
- Operating temperature: 0°C to 70°C.
- Temperature coefficient: 100 PPM/°C.
- Power dissipation: 740 mw max.





TRUTH TABLE

Enable ($\overline{E_0}$)	Address (Bit No.) 3	2	1	Pulse Width Out
0	0	0	0	T_0
0	0	0	1	T_1
0	0	1	0	T_2
0	0	1	1	T_3
0	1	0	0	T_4
0	1	0	1	T_5
0	1	1	0	T_6
0	1	1	1	T_7
1	Φ	Φ	Φ	0

1 = High
0 = Low
Φ = Don't care
T_0 = Reference or inherent pulse width.
T_1 to T_7 = Multiplier of pulse width.

Part Number	Incremental Pulse Width Per Step (ns)	Total Pulse Width Change (ns)
PPG-33-.5	.5 ± .3	3.5
PPG-33-1	1 ± .4	7
PPG-33-2	2 ± .4	14
PPG-33-3	3 ± .5	21
PPG-33-5	5 ± .6	35
PPG-33-10	10 ± 1.0	70
PPG-33-15	15 ± 1.3	105
PPG-33-20	20 ± 1.5	140
PPG-33-40	40 ± 2.0	280
PPG-33-50	50 ± 2.5	350

Contact us for specific requirements. We customize.

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