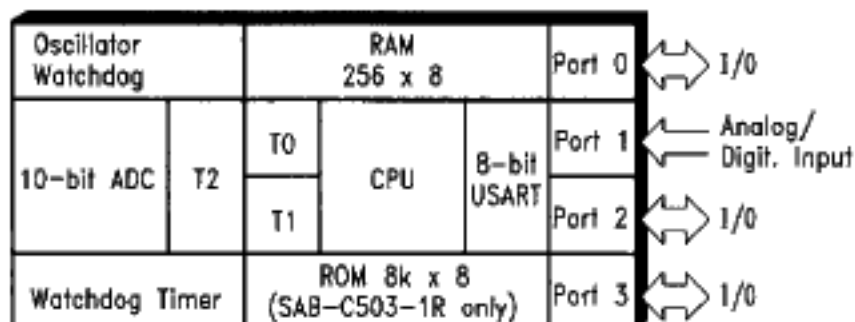


Preliminary

- Fully compatible to standard 8051 microcontroller
- Versions for 12 / 20 MHz operating frequency
- 8 K × 8 ROM (SAB-C503-1R only)
- 256 × 8 RAM
- Four 8-bit ports, (including one input port for digital or analog input)
- Three 16-bit Timers / Counters (Timer 2 with Up/Down Counter feature)
- USART
- Genuine 10-bit A/D Converter with 8 multiplexed inputs
- Seven interrupt sources, two priority levels
- Programmable 15-bit Watchdog Timer
- Oscillator Watchdog
- Fast Power On Reset
- Power Saving Modes
- P-LCC-44 package
- Temperature ranges: SAB-C503 T_A : 0 °C to 70 °C
 SAF-C503 T_A : - 40 °C to 85 °C

SAB-C503



MCA01764

The SAB-C503-L/C503-1R described in this document is compatible (not pin-compatible) with the SAB 80C32/C52 and can be used for all present SAB 80C52 applications.

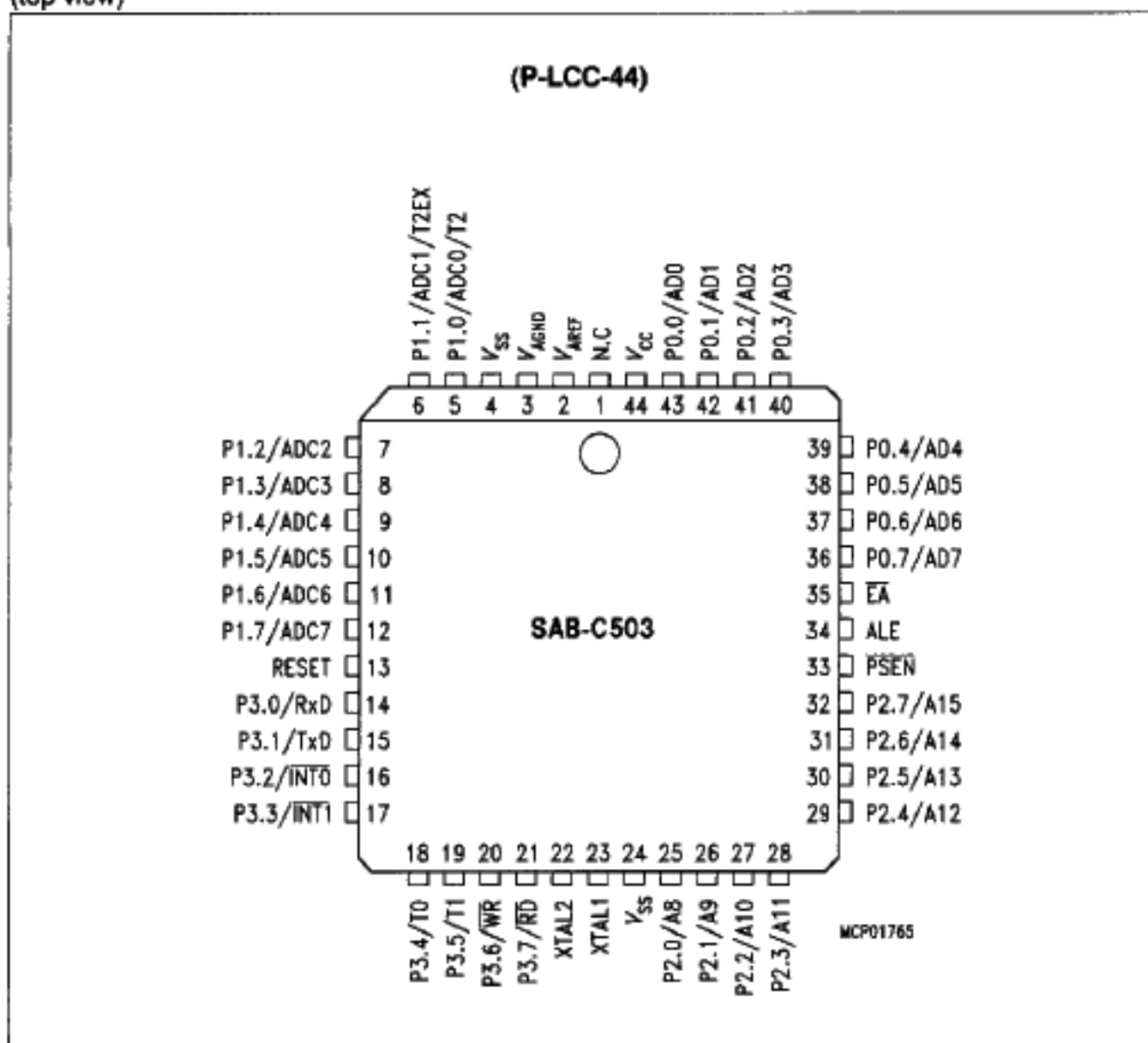
The SAB-C503-1R contains a non-volatile 8 K × 8 read-only program memory, a volatile 256 × 8 read/write data memory, four ports, three 16-bit timers/counters, a seven source, two priority level interrupt structure, a serial port, versatile fail save mechanisms and a genuine 10-bit A/D Converter. The SAB-C503-L is identical, except that it lacks the program memory on chip. Therefore the term SAB-C503 refers to both versions within this specification unless otherwise noted.

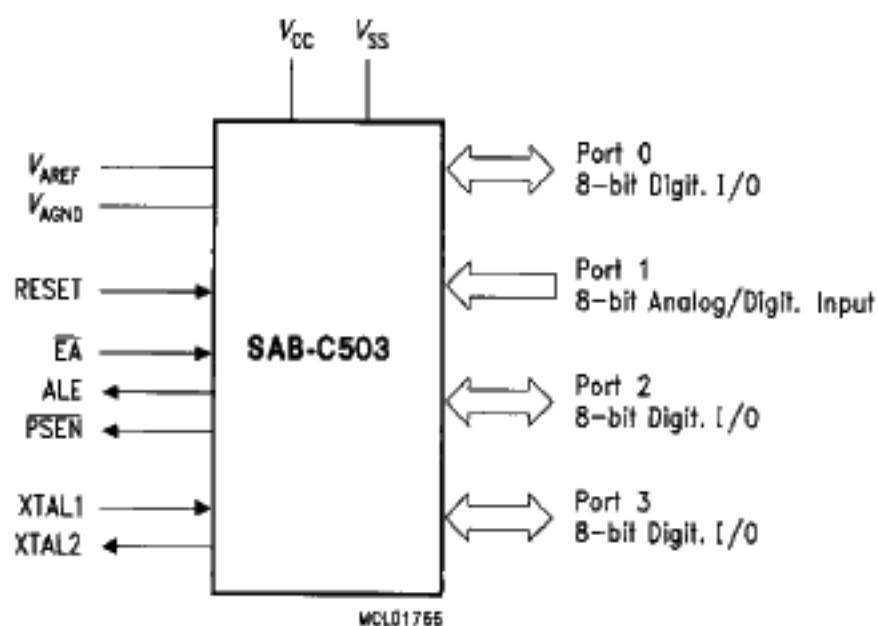
Ordering Information

Type	Ordering Code	Package	Description (8-Bit CMOS microcontroller)
SAB-C503-LN	Q67120-C835	P-LCC-44	for external memory 12 MHz
SAB-C503-1RN	Q67120-C834	P-LCC-44	with mask-programmable ROM, 12 MHz
SAB-C503-L20N	Q67120-C877	P-LCC-44	for external memory 20 MHz
SAB-C503-1R20N	Q67120-C878	P-LCC-44	with mask-programmable ROM, 20 MHz
SAF-C503-LN	Q67120-C879	P-LCC-44	for external ROM, 12 MHz, ext. temp. - 40 °C to 85 °C
SAF-C503-1RN	Q67120-C880	P-LCC-44	with mask-programmable ROM, 12 MHz, ext. temp. - 40 °C to 85 °C
SAF-C503-L20N	Q67120-C881	P-LCC-44	for external memory, 20 MHz, ext. temp. - 40 °C to 85 °C
SAF-C503-1R20N	Q67120-C882	P-LCC-44	with mask-programmable ROM, 20 MHz, ext. temp. - 40 °C to 85 °C

Note: Extended temperature range - 40 °C to 110 °C (SAH-C503) on request.

Pin Configuration
(top view)





Logic Symbol

Pin Definitions and Functions

Symbol	Pin Number	I/O *)	Function	
	P-LCC-44			
P1.7 – P1.0	12–5	I	<p>Port 1 is an 8-bit unidirectional input port. Port pins can be used for digital input, if voltage levels meet the specified input high low voltages, and for the multiplexed analog inputs of the A/D-Converter, simultaneously. Port 1 also contains the timer 2 pins as secondary function.</p> <p>The secondary functions are assigned to the pins of port 1, as follows:</p>	
	5			P1.0 AN0 / T2 Analog input channel 0 Input to counter 2
	6			P1.1 AN1 / T2EX Analog input channel 1 Capture - Reload trigger of timer 2 / Up-Down count
	7			P1.2 AN2 Analog input channel 2
	8			P1.3 AN3 Analog input channel 3
	9			P1.4 AN4 Analog input channel 4
	10			P1.5 AN5 Analog input channel 5
	11			P1.6 AN6 Analog input channel 6
	12			P1.7 AN7 Analog input channel 7

*) I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number	I/O)	Function
	P-LCC-44		
P3.0 – P3.7	14–21	I/O	<p>Port 3</p> <p>is a bidirectional I/O port with internal pull-up resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state they can be used as inputs. As inputs, port 3 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. Port 3 also contains the interrupt, timer, serial port 0 and external memory strobe pins which are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate.</p> <p>The secondary functions are assigned to the pins of port 3, as follows:</p>
	14		– RxD (P3.0): receiver data input (asynchronous) or data input/output (synchronous) of serial interface
	15		– TxD (P3.1): transmitter data output (asynchronous) or clock output (synchronous) of serial interface
	16		– $\overline{\text{INT0}}$ (P3.2): interrupt 0 input/timer 0 gate control
	17		– $\overline{\text{INT1}}$ (P3.3): interrupt 1 input/timer 1 gate control
	18		– T0 (P3.4): counter 0 input
	19		– T1 (P3.5): counter 1 input
	20		– $\overline{\text{WR}}$ (P3.6): the write control signal latches the data byte from port 0 into the external data memory
	21		– $\overline{\text{RD}}$ (P3.7): the read control signal enables the external data memory to port 0

*) I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number	I/O)	Function
	P-LCC-44		
XTAL2	22	–	XTAL2 Output of the inverting oscillator amplifier.
XTAL1	23	–	XTAL1 Input to the inverting oscillator amplifier and input to the internal clock generator circuits. To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is divided down by a divide-by-two flip-flop. Minimum and maximum high and low times as well as rise/fall times specified in the AC characteristics must be observed.
P2.0 – P2.7	25–32	I/O	Port 2 is a bidirectional I/O port with internal pull-up resistors. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state they can be used as inputs. As inputs, port 2 pins being externally pulled low will source current (I_{L} , in the DC characteristics) because of the internal pull-up resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pull-up resistors when issuing 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 issues the contents of the P2 special function register.
PSEN	33	O	The Program Store Enable output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods except during external data memory accesses. Remains high during internal program execution.
RESET	13	I	RESET A high level on this pin for two machine cycles while the oscillator is running resets the device. An internal diffused resistor to V_{SS} permits power-on reset using only an external capacitor to V_{CC} .

) I = Input
O = Output

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Pin Definitions and Functions (cont'd)

Symbol	Pin Number	I/O)	Function
	P-LCC-44		
ALE	34	O	The Address Latch Enable output is used for latching the low-byte of the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.
$\bar{E}A$	35	I	External Access Enable When held at high level, instructions are fetched from the internal ROM (SAB-C503-1R only) when the PC is less than 2000H. When held at low level, the SAB-C503 fetches all instructions from external program memory. For the SAB-C503-L this pin must be tied low.
P0.0 – P0.7	43–36	I/O	Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program or data memory. In this application it uses strong internal pull-up resistors when issuing 1s. Port 0 also outputs the code bytes during program verification in the SAB-C503-1R. External pull-up resistors are required during program verification.
V_{AREF}	2		Reference voltage for the A/D converter.
V_{AGND}	3		Reference ground for the A/D converter.
V_{SS}	4, 24	–	Circuit ground potential
V_{CC}	44	–	Supply terminal for all operating modes
N.C.	1	–	No connection

*) I = Input
O = Output

Functional Description

The SAB-C503 is fully compatible to the standard 8051 microcontroller family.

It is compatible with the SAB 80C52 but not pin-compatible. While maintaining all architectural and operational characteristics of the SAB 80C52 the SAB-C503 incorporates a genuine 10-bit A/D Converter as well as some enhancements in the Timer2 and Fail Save Mechanism Unit.

Figure 1 shows a block diagram of the SAB-C503.

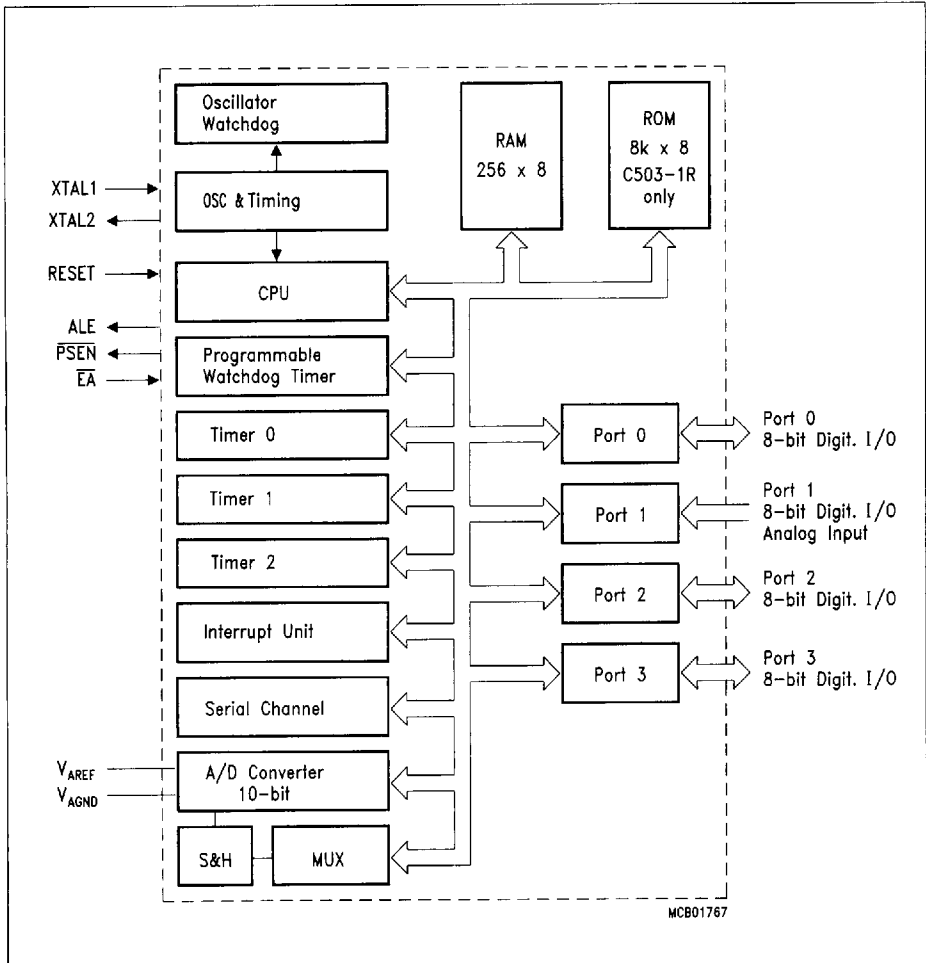


Figure 1
Block Diagram of the SAB-C503

CPU

The SAB-C503 is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44 % one-byte, 41 % two-byte, and 15 % three-byte instructions. With a 12 MHz crystal, 58 % of the instructions executed in 1.0 μ s (20 MHz : 600 ns).

Special Function Register PSW

Bit No.	MSB 7	6	5	4	3	2	1	LSB 0	
Addr. D0 _H	CY	AC	F0	RS1	RS0	OV	F1	P	PSW

Bit		Function
CY		Carry Flag
AC		Auxiliary Carry Flag (for BCD operations)
F0		General Purpose Flag
RS1	RS0	Register Bank select control bits
0	0	Bank 0 selected, data address 00 _H - 07 _H
0	1	Bank 1 selected, data address 08 _H - 0F _H
1	0	Bank 2 selected, data address 10 _H - 17 _H
1	1	Bank 3 selected, data address 18 _H - 1F _H
OV		Overflow Flag
F1		General Purpose Flag
P		Parity Flag. Set/cleared by hardware each instruction cycle to indicate an odd/even number of "one" bits in the accumulator, i.e. even parity.

Reset value of PSW is 00H.

Special Function Registers

All registers, except the program counter and the four general purpose register banks, reside in the special function register area.

The 33 special function registers (SFRs) include pointers and registers that provide an interface between the CPU and the other on-chip peripherals. There are also 128 directly addressable bits within the SFR area.

All SFRs are listed in **table 1**, **table 2** and **table 3**.

In **table 1** they are organized in numeric order of their addresses. In **table 2** they are organized in groups which refer to the functional blocks of the SAB-C503. **Table 3** illustrates the contents of the SFRs.

Table 1
Special Function Registers in Numeric Order of their Addresses

Address	Register	Contents after Reset	Address	Register	Contents after Reset
80H	P0 ¹⁾	FFH	98H	SCON ¹⁾	00H
81H	SP	07H	99H	SBUF	XXH ²⁾
82H	DPL	00H	9AH	reserved	XXH ²⁾
83H	DPH	00H	9BH	reserved	XXH ²⁾
84H	(WDTL) ³⁾	00H	9CH	reserved	XXH ²⁾
85H	(WDTH) ³⁾	00H	9DH	reserved	XXH ²⁾
86H	WDTRREL	00H	9EH	reserved	XXH ²⁾
87H	PCON	000X0000B ²⁾	9FH	reserved	XXH ²⁾
88H	TCON ¹⁾	00H	A0H	P2 ¹⁾	FFH
89H	TMOD	00H	A1H	reserved	XXH ²⁾
8AH	TL0	00H	A2H	reserved	XXH ²⁾
8BH	TL1	00H	A3H	reserved	XXH ²⁾
8CH	TH0	00H	A4H	reserved	XXH ²⁾
8DH	TH1	00H	A5H	reserved	XXH ²⁾
8EH	reserved	XXH ²⁾	A6H	reserved	XXH ²⁾
8FH	reserved	XXH ²⁾	A7H	reserved	XXH ²⁾
90H	P1 ¹⁾	FFH	A8H	IE ¹⁾	00H
91H	reserved	00H	A9H	reserved	XXH ²⁾
92H	reserved	XXH ²⁾	AAH	reserved	XXH ²⁾
93H	reserved	XXH ²⁾	ABH	reserved	XXH ²⁾
94H	reserved	XXH ²⁾	ACH	reserved	XXH ²⁾
95H	reserved	XXH ²⁾	ADH	reserved	XXH ²⁾
96H	reserved	XXH ²⁾	AEH	reserved	XXH ²⁾
97H	reserved	XXH ²⁾	AFH	reserved	XXH ²⁾

¹⁾: Bit-addressable Special Function Register

²⁾: X means that the value is indeterminate and the location is reserved

³⁾: () ... SFR not user accessible

Table 1
Special Function Register in Numeric Order of their Addresses (cont'd)

Address	Register	Contents after Reset	Address	Register	Contents after Reset
B0H	P3 ¹⁾	FFH	D8H	ADCON0 ¹⁾	00H
B1H	reserved	XXH ²⁾	D9H	ADDATH	00H
B2H	reserved	XXH ²⁾	DAH	ADDATL	00H
B3H	reserved	XXH ²⁾	DBH	reserved	XXH ²⁾
B4H	reserved	XXH ²⁾	DCH	ADCON1	0XXX0000B ²⁾
B5H	reserved	XXH ²⁾	DDH	reserved	XXH ²⁾
N6H	reserved	XXH ²⁾	DEH	reserved	XXH ²⁾
B7H	reserved	XXH ²⁾	DFH	reserved	XXH ²⁾
B8H	IP ¹⁾	XX000000B ²⁾	E0H	ACC ¹⁾	00H
B9H	reserved	XXH ²⁾	E1H	reserved	XXH ²⁾
BAH	reserved	XXH ²⁾	E2H	reserved	XXH ²⁾
BBH	reserved	XXH ²⁾	E3H	reserved	XXH ²⁾
BCH	reserved	XXH ²⁾	E4H	reserved	XXH ²⁾
BDH	reserved	XXH ²⁾	E5H	reserved	XXH ²⁾
BEH	reserved	XXH ²⁾	E6H	reserved	XXH ²⁾
BFH	reserved	XXH ²⁾	E7H	reserved	XXH ²⁾
C0H	WDCON ¹⁾	XXXX0000B ²⁾	E8H	reserved	XXH ²⁾
C1H	reserved	XXH ²⁾	E9H	reserved	XXH ²⁾
C2H	reserved	XXH ²⁾	EAH	reserved	XXH ²⁾
C3H	reserved	XXH ²⁾	EBH	reserved	XXH ²⁾
C4H	reserved	XXH ²⁾	ECH	reserved	XXH ²⁾
C5H	reserved	XXH ²⁾	EDH	reserved	XXH ²⁾
C6H	reserved	XXH ²⁾	EEH	reserved	XXH ²⁾
C7H	reserved	XXH ²⁾	EFH	reserved	XXH ²⁾
C8H	T2CON ¹⁾	00H	F0H	B ¹⁾	00H
C9H	T2MOD	XXXXXXXX0B ²⁾	F1H	reserved	XXH ²⁾
CAH	RC2L	00H	F2H	reserved	XXH ²⁾
CBH	RC2H	00H	F3H	reserved	XXH ²⁾
CCH	TL2	00H	F4H	reserved	XXH ²⁾
CDH	TH2	00H	F5H	reserved	XXH ²⁾
CEH	reserved	XXH ²⁾	F6H	reserved	XXH ²⁾
CFH	reserved	XXH ²⁾	F7H	reserved	XXH ²⁾
D0H	PSW ¹⁾	00H	F8H	reserved	XXH ²⁾
D1H	reserved	XXH ²⁾	F9H	reserved	XXH ²⁾
D2H	reserved	XXH ²⁾	FAH	reserved	XXH ²⁾
D3H	reserved	XXH ²⁾	FBH	reserved	XXH ²⁾
D4H	reserved	XXH ²⁾	FBH	reserved	XXH ²⁾
D5H	reserved	XXH ²⁾	FCH	reserved	XXH ²⁾
D6H	reserved	XXH ²⁾	FDH	reserved	XXH ²⁾
D7H	reserved	XXH ²⁾	FEH	reserved	XXH ²⁾
			FFH	reserved	XXH ²⁾

1): Bit-addressable Special Function Register

2): X means that the value is indeterminate and the location is reserved

Table 2
Special Function Registers - Functional Blocks

Block	Symbol	Name	Address	Contents after Reset
CPU	ACC	Accumulator	E0H ¹⁾	00H
	B	B-Register	F0H ¹⁾	00H
	DPH	Data Pointer, High Byte	83H	00H
	DPL	Data Pointer, Low Byte	82H	00H
	PSW	Program Status Word Register	D0H ¹⁾	00H
	SP	Stack Pointer	81H	07H
Interrupt System	IE	Interrupt Enable Register	A8H ¹⁾	00H
	IP	Interrupt Priority Register	B8H ¹⁾	X000 0000B ³⁾
Ports	P0	Port 0	80H ¹⁾	0FFH
	P1	Port 1, Analog/Digital Input	90H ¹⁾	XXH ³⁾
	P2	Port 2	A0H ¹⁾	0FFH
	P3	Port 3	B0H ¹⁾	0FFH
A/D-Converter	ADCON0	A/D Converter Control Register 0	D8H ¹⁾	00H
	ADCON1	A/D Converter Control Register 1	DCH	0XXX 0000B ³⁾
	ADDATH	A/D Converter Data Register High Byte	D9H	00H
	ADDATL	A/D Converter Data Register Low Byte	DAH	00H
Serial Channels	PCON ²⁾	Power Control Register	87H	00H
	SBUF	Serial Channel Buffer Reg.	99H	0XXH ³⁾
	SCON	Serial Channel 0 Control Reg.	98H ¹⁾	00H
Timer 0 / Timer 1	TCON	Timer 0/1 Control Register	88H ¹⁾	00H
	TH0	Timer 0, High Byte	8CH	00H
	TH1	Timer 1, High Byte	8DH	00H
	TL0	Timer 0, Low Byte	8AH	00H
	TL1	Timer 1, Low Byte	8BH	00H
	TMOD	Timer Mode Register	89H	00H
Timer 2	T2CON	Timer 2 Control Register	C8H ¹⁾	00H
	T2MOD	Timer 2 Mode Register	C9H	XXXX XXX0B ³⁾
	RC2H	Timer 2 Reload Capture Reg., High Byte	CAH	00H
	RC2L	Timer 2 Reload Capture Reg., Low Byte	CBH	00H
	TH2	Timer 2, High Byte	CDH	00H
	TL2	Timer 2, Low Byte	CEH	00H
	Watchdog	WDCON	Watchdog Timer Control Register	C0H ¹⁾
WDTREL		Watchdog Timer Reload Reg.	86H	00H
Pow.Sav. Modes	PCON	Power Control Register	87H	000X 0000B ³⁾

¹⁾ Bit-addressable special function registers

²⁾ This special function register is listed repeatedly since some bits of it also belong to other functional blocks

³⁾ X means that the value is indeterminate and the location is reserved

Table 3
Contents of SFRs, SFRs in Numeric Order

Address	Register	Bit 7	6	5	4	3	2	1	0
80 _H	P0								
81 _H	SP								
82 _H	DPL								
83 _H	DPH								
86 _H	WDTREL								
87 _H	PCON	SMOD	PDS	IDL5	–	GF1	GF0	PDE	IDLE
88 _H	TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
89 _H	TMOD	GATE	C/T	M1	M0	GATE	C/T	M1	M0
8A _H	TL0								
8B _H	TL1								
8C _H	TH0								
8D _H	TH1								
90 _H	P1								
98 _H	SCON	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
99 _H	SBUF								
A0 _H	P2								
A8 _H	IE	EA	EADC	ET2	ES	ET1	EX1	ET0	EX0
B0 _H	P3								
B8 _H	IP	–	PADC	PT2	PS	PT1	PX1	PT0	PX0
C0 _H	WDCON	–	–	–	–	OWDS	WDTS	WDT	SWDT
C8 _H	T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2
C9 _H	T2MOD	–	–	–	–	–	–	–	DCEN



SFR bit and byte addressable



SFR not bit addressable

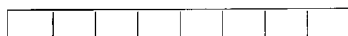


must not be used

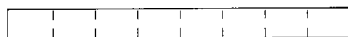
– : = bit location is reserved

Table 3
Contents of SFRs, SFRs in Numeric Order (cont'd)

Address	Register	Bit 7	6	5	4	3	2	1	0
CA _H	RC2L								
CB _H	RC2H								
CC _H	TL2								
CD _H	TH2								
D0 _H	PSW	CY	AC	F0	RS1	RS0	OV	F1	P
D8 _H	ADCON0	-	-	IADC	BSY	ADM	MX2	MX1	MX0
D9 _H	ADDATH	MSB							
DA _H	ADDATL		LSB	-	-	-	-	-	-
DC _H	ADCON1	ADCL	-	-	-	MX3	MX2	MX1	MX0
E0 _H	ACC								
F0 _H	B								



SFR bit and byte addressable



SFR not bit addressable



must not be used

- : = bit location is reserved

Timer / Counter 0 and 1

Timer/Counter 0 and 1 can be used in four operating modes as listed in **table 4**:

Table 4
Timer/Counter 0 and 1 Operating Modes

Mode	Description	TMOD				Input Clock	
		Gate	C/T	M1	M0	Internal	external (max)
0	8-bit timer/counter with a divide-by-32 prescaler	X	X	0	0	$f_{osc}/12 \times 32$	$f_{osc}/24 \times 32$
1	16-bit timer/counter	X	X	0	1	$f_{osc}/12$	$f_{osc}/24$
2	8-bit timer/counter with 8-bit auto-reload	X	X	1	0	$f_{osc}/12$	$f_{osc}/24$
3	Timer/counter 0 used as one 8-bit timer/counter and one 8-bit timer Timer 1 stops	X	X	1	1	$f_{osc}/12$	$f_{osc}/24$

In the "timer" function ($C/\bar{T} = '0'$) the register is incremented every machine cycle. Therefore the count rate is $f_{osc}/12$.

In the "counter" function the register is incremented in response to a 1-to-0 transition at its corresponding external input pin (P3.4/T0, P3.5/T1). Since it takes two machine cycles to detect a falling edge the max. count rate is $f_{osc}/24$. External inputs $\overline{INT0}$ and $\overline{INT1}$ (P3.2, P3.3) can be programmed to function as a gate to facilitate pulse width measurements. **Figure 2** illustrates the input clock logic.

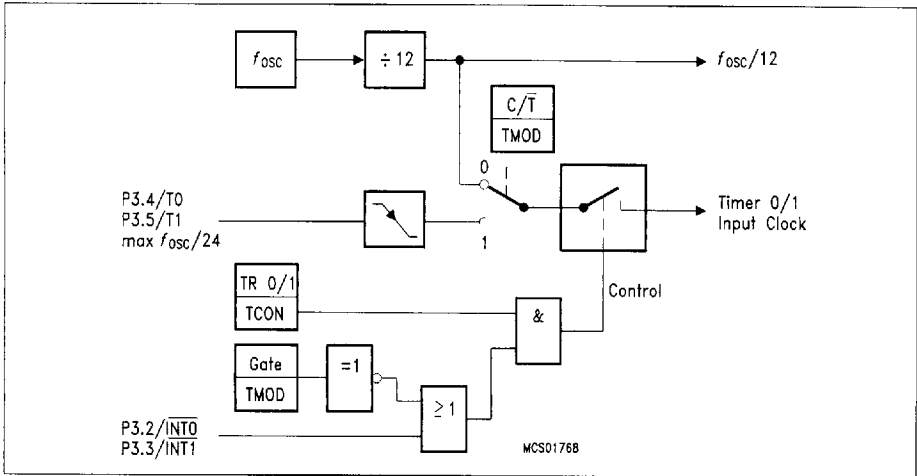


Figure 2
Timer/Counter 0 and 1 Input Clock Logic

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Timer 2

Timer 2 is a 16-bit Timer/Counter with an up/down count feature. It can operate either as timer or as an event counter which is selected by bit $C/\overline{T2}$ (T2CON.1). It has three operating modes as shown in table 5.

Table 5
Timer/Counter 2 Operating Modes

Mode	T2CON			T2MOD	T2CON		P1.1/ T2EX	Remarks	Input Clock	
	R×CLK or T×CLK	CP/ RL2	TR2	DCEN	EXEN	internal			external (P1.0/T2)	
16-bit Auto- reload	0	0	1	0	0	X		reload upon overflow reload trigger (falling edge) Down counting Up counting	$f_{osc}/12$	max $f_{osc}/24$
	0	0	1	0	1	↓				
	0	0	1	1	X	0				
	0	0	1	1	X	1				
16-bit Cap- ture	0	1	1	X	0	X		16 bit Timer/ Counter (only up-counting) capture TH2, TL2 → RC2H, RC2L	$f_{osc}/12$	max $f_{osc}/24$
	0	1	1	X	1	↓				
Baud Rate Gene- rator	1	X	1	X	0	X		no overflow interrupt request (TF2) extra external interrupt ("Timer 2")	$f_{osc}/2$	max $f_{osc}/24$
	1	X	1	X	1	↓				
off	X	X	0	X	X	X		Timer 2 stops	-	-

Note: ↓ =  falling edge

Serial Interface (USART)

The serial port is full duplex and can operate in four modes (one synchronous mode, three asynchronous modes) as illustrated in **table 6**. The possible baudrates can be calculated using the formulas given in **table 7**.

Table 6
USART Operating Modes

Mode	T2CON		Baudrate	Description
	SM0	SM1		
0	0	0	$f_{osc}/12$	Serial data enters and exits through RxD. TxD outputs the shift clock. 8-bits are transmitted/received (LSB first)
1	0	1	Timer 1/2 overflow rate	8-bit UART 10 bits are transmitted (through TxD) or received (RxD)
2	1	0	$f_{osc}/32$ or $f_{osc}/64$	9-bit UART 11 bits are transmitted (TxD) or received (RxD)
3	1	1	Timer 1/2 overflow rate	9-bit UART Like mode 2 except the variable baud rate

Table 7
Formulas for Calculating Baudrates

Baud Rate derived from	Interface Mode	Baudrate
Oscillator	0 2	$f_{osc}/12$ $(2^{SMOD} \times f_{osc}) / 64$
Timer 1 (16-bit timer) (8-bit timer with 8-bit autoreload)	1,3 1,3	$(2^{SMOD} \times \text{timer 1 overflow rate}) / 32$ $(2^{SMOD} \times f_{osc}) / (32 \times 12 \times (256 - TH1))$
Timer 2	1,3	$f_{osc} / (32 \times (65536 - (RC2H, RC2L)))$

10-bit A/D Converter

In the SAB-C503 a high performance/high speed 8-channel 10-bit A/D-Converter (ADC) using the successive approximation technique is implemented.

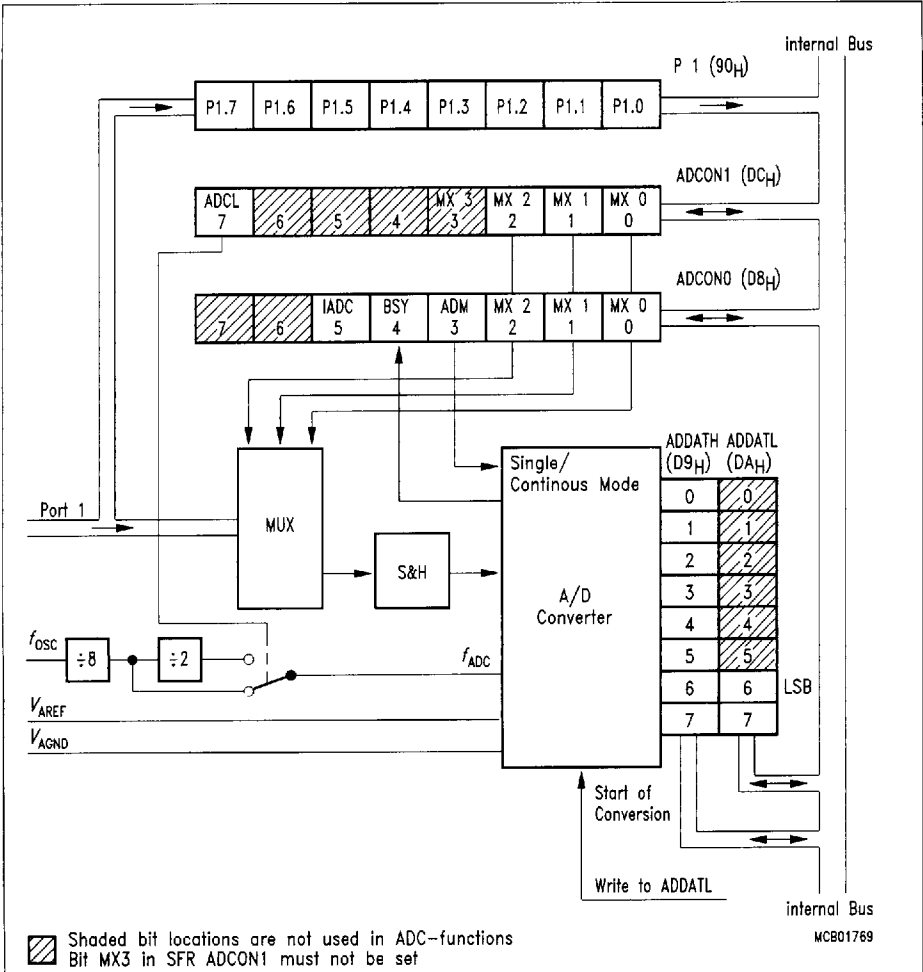


Figure 3
Block Diagram A/D-Converter

Note that bit ADCL in SFR ADCON0 has to be set when f_{OSC} is higher than 16 MHz. Furthermore bit MX3 in SFR ADCON1 must not be set otherwise a not connected channel would be selected.

The formula for the conversion time is given by: $t_C = 14 \times (8 \times 2^{ADCL}) / f_{OSC}$

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Interrupt System

The SAB-C503 provides 7 interrupt sources with two priority levels. **Figure 4** gives a general overview of the interrupt sources and illustrates the request and control flags.

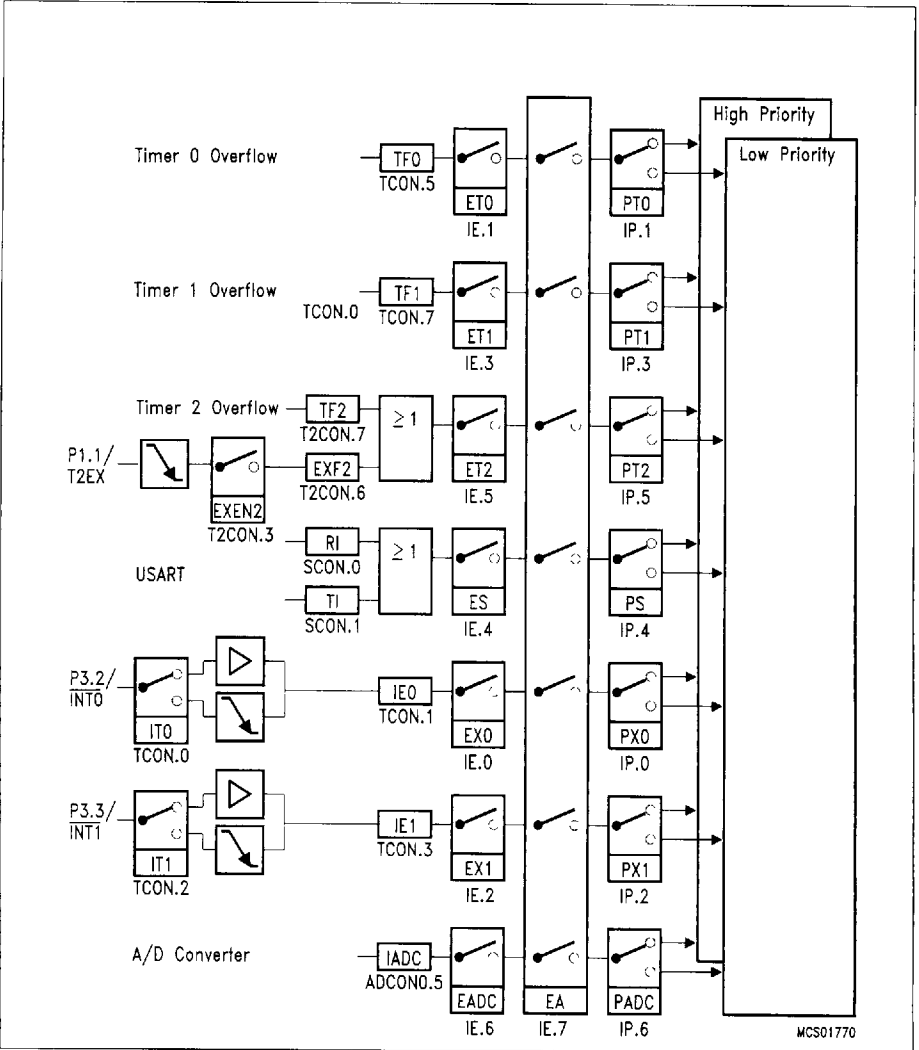


Figure 4
Interrupt Request Sources

Table 8
Interrupt Sources and their Corresponding Interrupt Vectors

Source (Request Flags)	Vector	Vector Address
IE0	External interrupt 0	0003 _H
TF0	Timer 0 interrupt	000B _H
IE1	External interrupt 1	0013 _H
TF1	Timer 1 interrupt	001B _H
RI + TI	Serial port interrupt	0023 _H
TF2 + EXF2	Timer 2 interrupt	002B _H
IADC	A/D converter interrupt	0043 _H

A low-priority interrupt can itself be interrupted by a high-priority interrupt, but not by another low-priority interrupt. A high-priority interrupt cannot be interrupted by any other interrupt source.

If two requests of different priority level are received simultaneously, the request of higher priority is serviced. If requests of the same priority are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence as shown in **table 9**.

Table 9
Interrupt Priority-within-Level

Interrupt Source		Priority
External Interrupt 0, A/D Converter,	IE0 IADC	High
Timer 0 Interrupt,	TF0	
External Interrupt 1, Timer 1 Interrupt,	IE1 TF1	↓
Serial Channel,	RI or TI	
Timer 2 Interrupt,	TF2 or EXF2	
		Low

Fail Safe Mechanisms

The SAB-C503 offers enhanced fail safe mechanisms, which allow an automatic recovery from software upset or hardware failure.

- 1) Watchdog Timer (15bit, WDT)
- 2) Oscillator Watchdog (OWD)

1) Watchdog Timer (WDT)

The Watchdog Timer in the SAB-C503 is a 15-bit timer, which is incremented by a count rate of either $f_{CYCLE}/2$ or $f_{CYCLE}/32$ ($f_{CYCLE} = f_{OSC}/12$). That is, the machine clock is divided by a series of arrangement of two prescalers, a divide-by-two and a divide-by-16 prescaler. The latter is enabled by setting bit WDTREL.7.

Figure 5 shows the block diagram of the programmable Watchdog Timer.

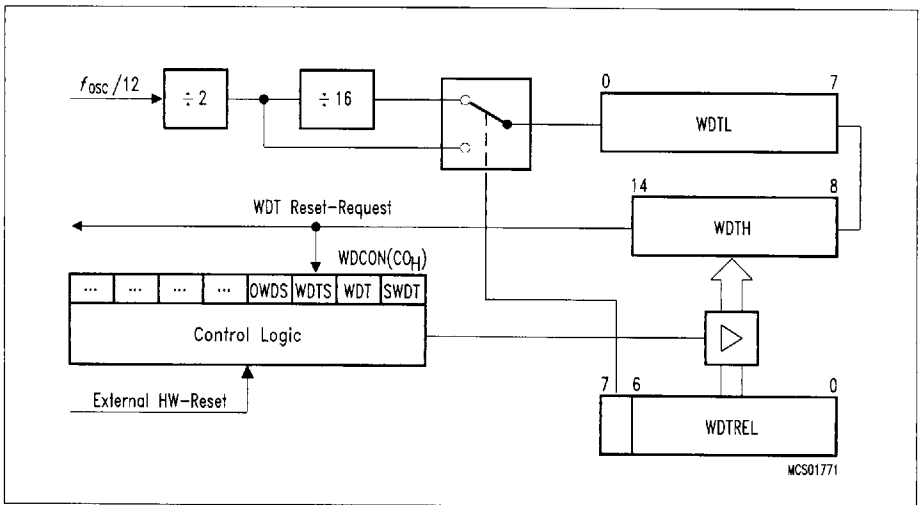


Figure 5
Block Diagram of the Programmable Watchdog Timer

- Starting and refreshing the WDT

Table 10 gives an overview how to start and refresh the WDT. The mentioned bits are located in SFR WDCON.

Table 10
Starting and Refreshing the WDT

Function	Example	Remarks
Starting WDT	SETB SWDT	Cannot be stopped during active mode of the device. WDT is halted during idle mode, power down mode or the oscillator watchdog reset is active.
Refreshing WDT	SETB WDT SETB SWDT	Double instruction sequence (setting bit WDT and SWDT consecutively) to increase system security.

- Watchdog reset and watchdog status flag (WDTS)

If the software fails to clear the watchdog in time, an internally generated watchdog reset is entered at the counter state $7FFC_H$. The duration of the reset signal then depends on the prescaler selection (either 8 or 128 cycles). This internal reset differs from an external one in so far as the Watchdog Timer is not disabled and bit WDTS (SFR WDCON) is set. The WDTS is a flip-flop, which is set by a Watchdog Timer reset and can be cleared by an external hardware reset. Bit WDTS allows the software to examine from which source the reset was activated. The bit WDTS can also be cleared by software.

2) Oscillator Watchdog (OWD)

The OWD consists of an internal RC oscillator which provides the reference frequency for the comparison with the frequency of the on-chip oscillator.

Figure 6 shows the block diagram of the oscillator watchdog unit while table 11 shows the effect when the OWD becomes active/inactive

Note: The OWD is always enabled!

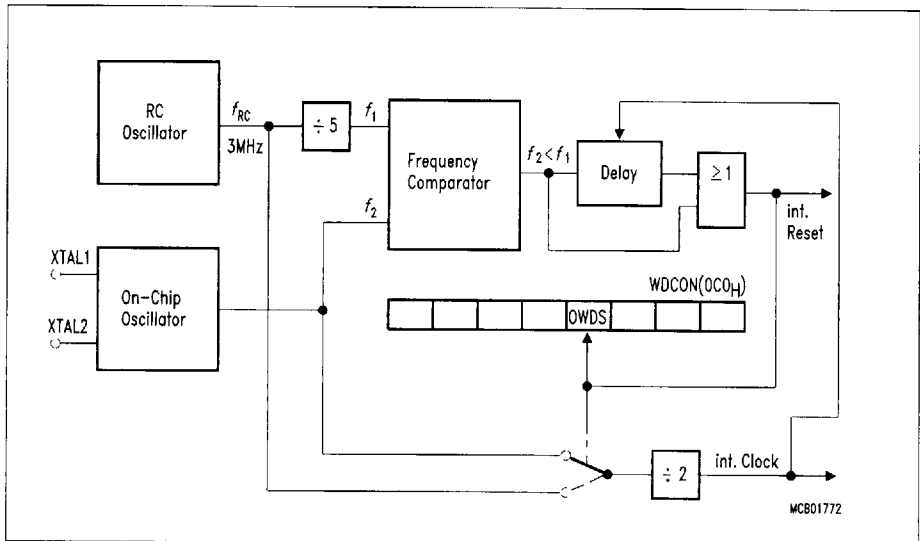


Figure 6
Functional Block Diagram of the Oscillator Watchdog

Table 11
Effects of the OWD

Conditions	Effect
$f_{osc} < f_{RC}/5$	Switch input of internal clock system to RC oscillator output Activating internal reset at the same time (reset sequence is clocked by RC-oscillator). Exception from effects of a Hardware Reset: Watchdog Timer Status Flag, WDTS is not reset Oscillator Watchdog Status Flag, OWDS is set
$f_{osc} > f_{RC}/5$	Input of internal clock system is $f_{osc}/2$. When failure condition ($f_{osc} < f_{RC}/5$) disappears the part executes a final reset phase of typ. 1 ms in order to allow the external oscillator to stabilize.

Fast Internal Reset after Power-On

The SAB-C503 can use the oscillator watchdog unit for a fast internal reset procedure after power-on.

Normally members of the 8051 family enter their default reset state not before the on-chip oscillator starts. The reason is that the external reset signal must be internally synchronized and processed in order to bring the device into the correct reset state. Especially if a crystal is used the start up time of the oscillator is relatively long (typ. 1 ms). During this time period the pins have an undefined state which could have severe effects e.g. to actuators connected to port pins.

In the SAB-C503 the oscillator watchdog unit avoids this situation. After power-on the oscillator watchdog's RC oscillator starts working within a very short start-up time (typ. less than 2 μ s). In the following the watchdog circuitry detects a failure condition for the on-chip oscillator this has not yet started (a failure is always recognized if the watchdog's RC oscillator runs faster than the on-chip oscillator). As long as this condition is valid the watchdog uses the RC oscillator output as a clock source for the chip rather than the on-chip oscillator's output. This allows correct resetting of the part and brings also all ports to the defined state.

Delay between power-on and correct reset state:

Typ: 18 μ s

Max: 34 μ s

Power Saving Modes

Two power down modes are available, the Idle Mode and Power Down Mode.

The bits PDE, PDS and IDLE, IDLS select the Power Down mode or the idle mode, respectively. If the Power Down mode and the idle mode are set at the same time, Power Down takes precedence. **Table 10** gives a general overview of the power saving modes.

Table 10
Power Saving Modes Overview

Mode	Entering Example	Leaving by	Remarks
Idle mode	ORL PCON, #01H ORL PCON, #20H	– enabled interrupt – Hardware Reset	CPU is gated off CPU status registers maintain their data. Peripherals are active Double instruction sequence
Power-Down Mode	ORL PCON, #02H ORL PCON, #40H	Hardware Reset	Oscillator are stopped. Contents of on-chip RAM and SFR's are maintained (leaving Power Down Mode means redefinition of SFR's contents). Double instruction sequence

In the Power Down mode of operation, V_{CC} can be reduced to minimize power consumption. It must be ensured, however, that V_{CC} is not reduced before the Power Down mode is invoked, and that V_{CC} is restored to its normal operating level, before the Power Down mode is terminated. The reset signal that terminates the Power Down mode also restarts the oscillator. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize (simulator to power-on reset).

Absolute Maximum Ratings

Ambient temperature under bias (T_A)	- 40 to + 85 °C
Storage temperature (T_{ST}).....	- 65 to + 150 °C
Voltage on V_{CC} pins with respect to ground (V_{SS})	- 0.5 V to 6.5 V
Voltage on any pin with respect to ground (V_{SS})	- 0.5 V to $V_{CC} + 0.5$ V
Input current on any pin during overload condition	- 10 mA to + 10 mA
Absolute sum of all input currents during overload condition	100 mA
Power dissipation.....	TBD

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During overload conditions ($V_{IN} > V_{CC}$ or $V_{IN} < V_{SS}$) the Voltage on V_{CC} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

DC Characteristics

 $V_{CC} = 5\text{ V} + 10\%, -15\%$; $V_{SS} = 0\text{ V}$; $T_A = 0\text{ }^\circ\text{C}$ to $70\text{ }^\circ\text{C}$

for the SAB-C503

 $T_A = -40\text{ }^\circ\text{C}$ to $85\text{ }^\circ\text{C}$

for the SAF-C503

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage (except $\overline{\text{EA}}$, RESET)	V_{IL}	-0.5	$0.2 V_{CC} - 0.1$	V	—
Input low voltage ($\overline{\text{EA}}$)	V_{IL1}	-0.5	$0.2 V_{CC} - 0.3$	V	—
Input low voltage (RESET)	V_{IL2}	-0.5	$0.2 V_{CC} + 0.1$	V	—
Input high voltage (except RESET, XTAL1, $\overline{\text{EA}}$)	V_{IH}	$0.2 V_{CC} + 0.9$	$V_{CC} + 0.5$	V	—
Input high voltage to XTAL1	V_{IH1}	$0.7 V_{CC}$	$V_{CC} + 0.5$	V	—
Input high voltage to RESET, $\overline{\text{EA}}$	V_{IH2}	$0.6 V_{CC}$	$V_{CC} + 0.5$	V	—
Output low voltage (ports 2, 3)	V_{OL}	—	0.45	V	$I_{OL} = 1.6\text{ mA}^{1)}$
Output low voltage (port 0, ALE, $\overline{\text{PSEN}}$)	V_{OL1}	—	0.45	V	$I_{OL} = 3.2\text{ mA}^{1)}$
Output high voltage (ports 2, 3)	V_{OH}	2.4 $0.9 V_{CC}$	— —	V	$I_{OH} = -80\text{ }\mu\text{A}$, $I_{OH} = -10\text{ }\mu\text{A}$
Output high voltage (port 0 in external bus mode, ALE, $\overline{\text{PSEN}}$)	V_{OH1}	2.4 $0.9 V_{CC}$	— —	V	$I_{OH} = -800\text{ }\mu\text{A}^{2)}$, $I_{OH} = -80\text{ }\mu\text{A}^{2)}$
Logic 0 input current (ports 1, 2, 3)	I_{IL}	-10	-50	μA	$V_{IN} = 0.45\text{ V}$
Logical 1-to-0 transition current (ports 2, 3)	I_{TL}	-65	-650	μA	$V_{IN} = 2\text{ V}$
Input leakage current (port 0, $\overline{\text{EA}}$, P1)	I_{LI}	—	± 1	μA	$0.45 < V_{IN} < V_{CC}$
Pin capacitance	C_{IO}	—	10	pF	$f_C = 1\text{ MHz}$, $T_A = 25\text{ }^\circ\text{C}$
Power supply current:					
Active mode, 12 MHz ⁷⁾	I_{CC}	—	25.8	mA	$V_{CC} = 5\text{ V}$, ⁴⁾
Idle mode, 12 MHz ⁷⁾	I_{CC}	—	8	mA	$V_{CC} = 5\text{ V}$, ⁵⁾
Active mode, 20 MHz ⁷⁾	I_{CC}	—	35.5	mA	$V_{CC} = 5\text{ V}$, ⁴⁾
Idle mode, 20 MHz ⁷⁾	I_{CC}	—	10.1	mA	$V_{CC} = 5\text{ V}$, ⁵⁾
Power Down Mode	I_{PD}	—	50	μA	$V_{CC} = 2 \dots 5.5\text{ V}$, ³⁾

- 1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and port 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a schmitt-trigger, or use an address latch with a schmitt-trigger strobe input.
- 2) Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and \overline{PSEN} to momentarily fall below the 0.9 V_{CC} specification when the address lines are stabilizing.
- 3) I_{PD} (Power Down Mode) is measured under following conditions:
 $\overline{EA} = \text{Port 0} = \text{Port 1} = V_{CC}$; RESET = V_{SS} ; XTAL2 = N.C.; XTAL1 = V_{SS} ; $V_{AGND} = V_{SS}$; all other pins are disconnected.
- 4) I_{CC} (active mode) is measured with:
 XTAL1 driven with t_{CLCH} , $t_{CHCL} = 5$ ns, $V_{IL} = V_{SS} + 0.5$ V, $V_{IH} = V_{CC} - 0.5$ V, XTAL2 = N.C.; $\overline{EA} = \text{Port 0} = \text{Port 1} = \text{RESET} = V_{CC}$; all other pins are disconnected. I_{CC} would be slightly higher if a crystal oscillator is used (appr. 1 mA).
- 5) I_{CC} (Idle mode) is measured with all output pins disconnected and with all peripherals disabled;
 XTAL1 driven with t_{CLCH} , $t_{CHCL} = 5$ ns, $V_{IL} = V_{SS} + 0.5$ V, $V_{IH} = V_{CC} - 0.5$ V; XTAL2 = N.C.; RESET = $\overline{EA} = V_{SS}$; Port 0 = Port 1 = V_{CC} ; all other pins are disconnected;
- 7) $I_{CC \text{ max}}$ other frequencies is given by:
 active mode: $I_{CC \text{ max}} = 1.21 \times f_{OSC} + 11.28$
 idle mode: $I_{CC \text{ max}} = 0.27 \times f_{OSC} + 4.73$
 where f_{OSC} is the oscillator frequency in MHz. I_{CC} values are given in mA and measured at $V_{CC} = 5$ V.

A/D Converter Characteristics

$$V_{CC} = 5\text{ V} + 10\%, -15\%; V_{SS} = 0\text{ V}$$

$$V_{AREF} = V_{CC} \pm 5\%;$$

$$V_{AGND} = V_{SS} \pm 0.2\text{ V};$$

$$T_A = 0\text{ }^\circ\text{C to }70\text{ }^\circ\text{C} \quad \text{for the SAB-C503}$$

$$T_A = -40\text{ }^\circ\text{C to }85\text{ }^\circ\text{C} \quad \text{for the SAF-C503}$$

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Analog input capacitance	C_i		25	70	pF	
Sample time (Inc. load time)	T_s			4 t_{CY} ¹⁾	μs	²⁾
Conversion time (inc. sample time)	T_C			14 t_{CY} ¹⁾	μs	³⁾
Total unadjusted error ⁴⁾	TUE			± 2	LSB	$V_{AREF} = V_{CC}$ $V_{AGND} = V_{SS}$

¹⁾ $t_{CY} = (8 \times 2^{ADCL}) / f_{OSC}$ ($t_{CY} = 1 / f_{ADC}$; $f_{ADC} = f_{OSC} / (8 \times 2^{ADCL})$)

²⁾ This parameter specifies the time during the input capacitance C_i , can be charged/discharged by the external source. It must be guaranteed, that the input capacitance C_i , is fully loaded within this time. 4 TCY is 2 μs at the $f_{OSC} = 16\text{ MHz}$. After the end of the sample time T_s , changes of the analog input voltage have no effect on the conversion result.

³⁾ This parameter includes the sample time T_s . 14 TCY is 7 μs at $f_{OSC} = 16\text{ MHz}$.

⁴⁾ This parameter includes also the DNLE.

AC Characteristics for SAB-C503-LN / C503-1RN
 $V_{CC} = 5\text{ V} + 10\%, -15\%$; $V_{SS} = 0\text{ V}$
 $T_A = 0\text{ }^\circ\text{C to }70\text{ }^\circ\text{C}$ for the SAB-C503

 $T_A = -40\text{ }^\circ\text{C to }85\text{ }^\circ\text{C}$ for the SAF-C503

 $(C_L \text{ for port 0, ALE and } \overline{\text{PSEN}} \text{ outputs} = 100\text{ pF}; C_L \text{ for all other outputs} = 80\text{ pF})$
Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		12 MHz Clock		Variable Clock $1/t_{CLCL} = 3.5\text{ MHz to }12\text{ MHz}$		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	127	–	$2t_{CLCL} - 40$	–	ns
Address setup to ALE	t_{AVLL}	43	–	$t_{CLCL} - 40$	–	ns
Address hold after ALE	t_{LLAX}	30	–	$t_{CLCL} - 53$	–	ns
ALE low to valid instr in	t_{LLIV}	–	233	–	$4t_{CLCL} - 100$	ns
ALE to $\overline{\text{PSEN}}$	t_{LLPL}	58	–	$t_{CLCL} - 25$	–	ns
$\overline{\text{PSEN}}$ pulse width	t_{PLPH}	215	–	$3t_{CLCL} - 35$	–	ns
$\overline{\text{PSEN}}$ to valid instr in	t_{PLIV}	–	150	–	$3t_{CLCL} - 100$	ns
Input instruction hold after $\overline{\text{PSEN}}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{\text{PSEN}}$	$t_{PXIZ}^*)$	–	63	–	$t_{CLCL} - 20$	ns
Address valid after $\overline{\text{PSEN}}$	$t_{PXAV}^*)$	75	–	$t_{CLCL} - 8$	–	ns
Address to valid instr in	t_{AVIV}	–	302	–	$5t_{CLCL} - 115$	ns
Address float to $\overline{\text{PSEN}}$	t_{AZPL}	0	–	0	–	ns

*) Interfacing the SAB-C503 to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 Drivers.

AC Characteristics for SAB-C503-LN / C503-1RN

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		12 MHz Clock		Variable Clock $1/t_{CLCL} = 3.5 \text{ MHz to } 12 \text{ MHz}$		
		min.	max.	min.	max.	
$\overline{\text{RD}}$ pulse width	t_{RLRH}	400	–	$6t_{CLCL} - 100$	–	ns
$\overline{\text{WR}}$ pulse width	t_{WLWH}	400	–	$6t_{CLCL} - 100$	–	ns
Address hold after ALE	t_{LLAX2}	30	–	$t_{CLCL} - 53$	–	ns
$\overline{\text{RD}}$ to valid data in	t_{RLDV}	–	252	–	$5t_{CLCL} - 165$	ns
Data hold after $\overline{\text{RD}}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{\text{RD}}$	t_{RHDZ}	–	97	–	$2t_{CLCL} - 70$	ns
ALE to valid data in	t_{LLDV}	–	517	–	$8t_{CLCL} - 150$	ns
Address to valid data in	t_{AVDV}	–	585	–	$9t_{CLCL} - 165$	ns
ALE to $\overline{\text{WR}}$ or $\overline{\text{RD}}$	t_{LLWL}	200	300	$3t_{CLCL} - 50$	$3t_{CLCL} + 50$	ns
Address valid to $\overline{\text{WR}}$ or $\overline{\text{RD}}$	t_{AVWL}	203	–	$4t_{CLCL} - 130$	–	ns
$\overline{\text{WR}}$ or $\overline{\text{RD}}$ high to ALE high	t_{WHLH}	43	123	$t_{CLCL} - 40$	$t_{CLCL} + 40$	ns
Data valid to $\overline{\text{WR}}$ transition	t_{QVWX}	33	–	$t_{CLCL} - 50$	–	ns
Data setup before $\overline{\text{WR}}$	t_{QVWH}	433	–	$7t_{CLCL} - 150$	–	ns
Data hold after $\overline{\text{WR}}$	t_{WHQX}	33	–	$t_{CLCL} - 50$	–	ns
Address float after $\overline{\text{RD}}$	t_{RLAZ}	–	0	–	0	ns

External Clock Drive

Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 3.5 MHz to 12 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	83.3	285.7	ns
High time	t_{CHCX}	20	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	20	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	—	20	ns
Fall time	t_{CHCL}	—	20	ns

AC Characteristics for SAB-C503-L20N / C503-1R20N

$V_{CC} = 5\text{ V} + 10\%, -15\%$; $V_{SS} = 0\text{ V}$

$T_A = 0\text{ }^\circ\text{C}$ to $70\text{ }^\circ\text{C}$ for the SAB-C503

$T_A = -40\text{ }^\circ\text{C}$ to $85\text{ }^\circ\text{C}$ for the SAF-C503

(C_L for port 0, ALE and $\overline{\text{PSEN}}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		20 MHz Clock		Variable Clock $1/f_{\text{CLCL}} = 3.5\text{ MHz to }20\text{ MHz}$		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	60	–	$2t_{\text{CLCL}} - 40$	–	ns
Address setup to ALE	t_{AVLL}	20	–	$t_{\text{CLCL}} - 30$	–	ns
Address hold after ALE	t_{LLAX}	20	–	$t_{\text{CLCL}} - 30$	–	ns
ALE low to valid instr in	t_{LLIV}	–	100	–	$4t_{\text{CLCL}} - 100$	ns
ALE to $\overline{\text{PSEN}}$	t_{LLPL}	25	–	$t_{\text{CLCL}} - 25$	–	ns
$\overline{\text{PSEN}}$ pulse width	t_{PLPH}	115	–	$3t_{\text{CLCL}} - 35$	–	ns
$\overline{\text{PSEN}}$ to valid instr in	t_{PLIV}	–	75	–	$3t_{\text{CLCL}} - 75$	ns
Input instruction hold after $\overline{\text{PSEN}}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{\text{PSEN}}$	$t_{\text{PXIZ}}^*)$	–	40	–	$t_{\text{CLCL}} - 10$	ns
Address valid after $\overline{\text{PSEN}}$	$t_{\text{PXAV}}^*)$	47	–	$t_{\text{CLCL}} - 3$	–	ns
Address to valid instr in	t_{AVIV}	–	190	–	$5t_{\text{CLCL}} - 60$	ns
Address float to $\overline{\text{PSEN}}$	t_{AZPL}	0	–	0	–	ns

*) Interfacing the SAB-C503 to devices with float times up to 45 ns is permissible. This limited bus contention will not cause any damage to port 0 Drivers.

AC Characteristics for SAB-C501-L20N / C503-1R20N

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		20 MHz Clock		Variable Clock $1/t_{CLCL} = 3.5 \text{ MHz to } 20 \text{ MHz}$		
		min.	max.	min.	max.	
$\overline{\text{RD}}$ pulse width	t_{RLRH}	200	–	$6t_{CLCL} - 100$	–	ns
$\overline{\text{WR}}$ pulse width	t_{WLWH}	200	–	$6t_{CLCL} - 100$	–	ns
Address hold after ALE	t_{LLAX2}	20	–	$t_{CLCL} - 30$	–	ns
$\overline{\text{RD}}$ to valid data in	t_{RLDV}	–	155	–	$5t_{CLCL} - 95$	ns
Data hold after $\overline{\text{RD}}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{\text{RD}}$	t_{RHDX}	–	76	–	$2t_{CLCL} - 24$	ns
ALE to valid data in	t_{LLDV}	–	250	–	$8t_{CLCL} - 150$	ns
Address to valid data in	t_{AVDV}	–	285	–	$9t_{CLCL} - 165$	ns
ALE to $\overline{\text{WR}}$ or $\overline{\text{RD}}$	t_{LLWL}	100	200	$3t_{CLCL} - 50$	$3t_{CLCL} + 50$	ns
Address valid to $\overline{\text{WR}}$ or $\overline{\text{RD}}$	t_{AVWL}	70	–	$4t_{CLCL} - 130$	–	ns
$\overline{\text{WR}}$ or $\overline{\text{RD}}$ high to ALE high	t_{WHLH}	20	80	$t_{CLCL} - 30$	$t_{CLCL} + 30$	ns
Data valid to $\overline{\text{WR}}$ transition	t_{QVWX}	5	–	$t_{CLCL} - 45$	–	ns
Data setup before $\overline{\text{WR}}$	t_{QVWH}	200	–	$7t_{CLCL} - 150$	–	ns
Data hold after $\overline{\text{WR}}$	t_{WHOX}	10	–	$t_{CLCL} - 40$	–	ns
Address float after $\overline{\text{RD}}$	t_{RLAZ}	–	0	–	0	ns

External Clock Drive

Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 3.5 MHz to 20 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	50	285.7	ns
High time	t_{CHCX}	12	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	12	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	—	12	ns
Fall time	t_{CHCL}	—	12	ns

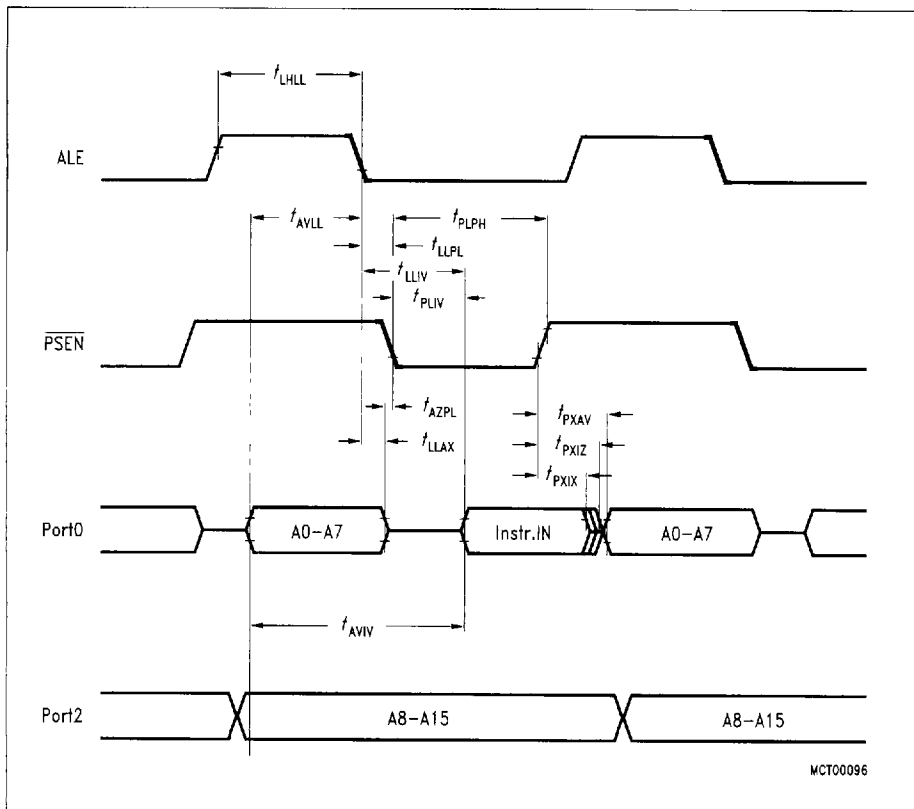


Figure 7
Program Memory Read Cycle

8235605 0061351 T54

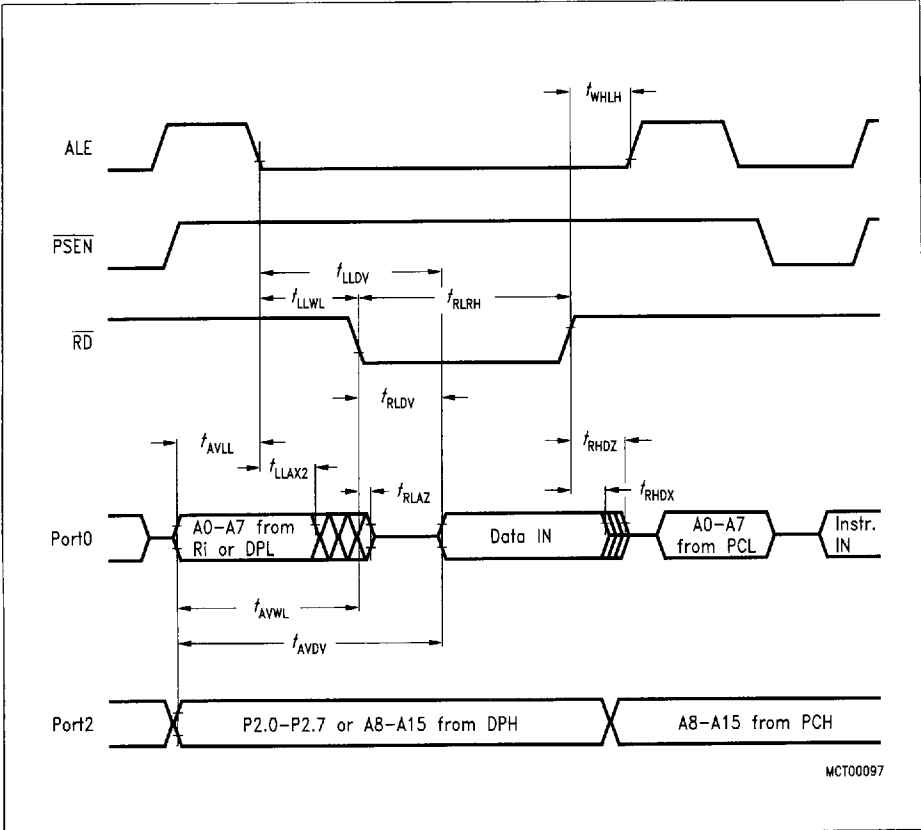


Figure 8
Data Memory Read Cycle

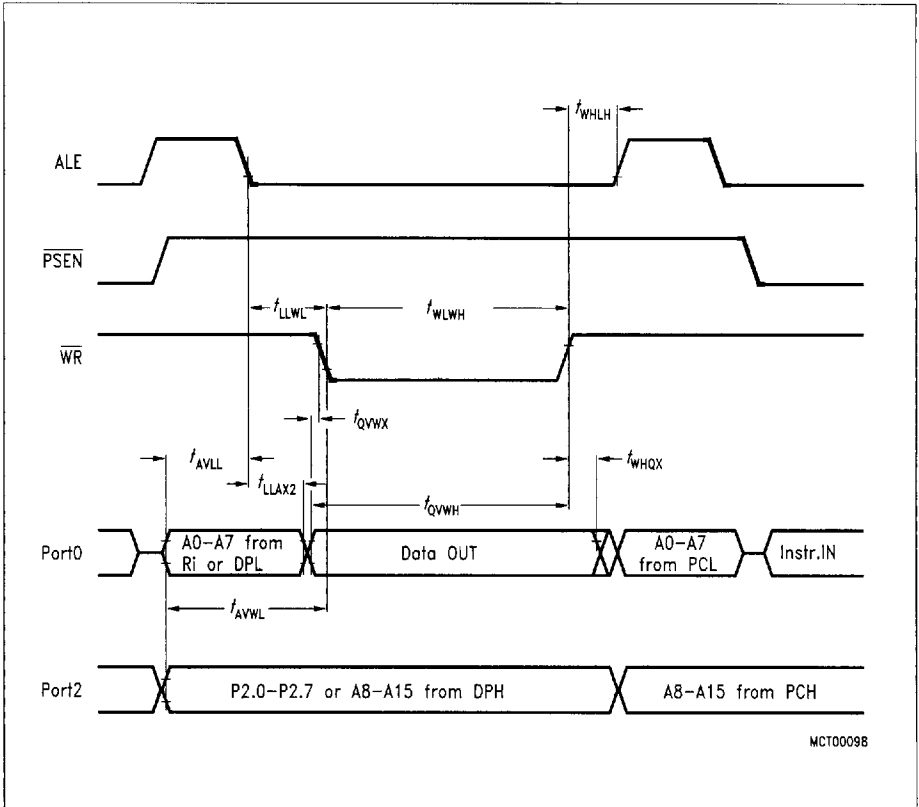


Figure 9
Data Memory Write Cycle

ROM Verification Characteristics for SAB-C503-1R

ROM Verification Mode 1

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Address to valid data	t_{AVQV}	—	$48t_{CLCL}$	ns
ENABLE to valid data	t_{ELQV}	—	$48t_{CLCL}$	ns
Data float after ENABLE	t_{EHQZ}	0	$48t_{CLCL}$	ns
Oscillator frequency	$1/t_{CLCL}$	4	6	MHz

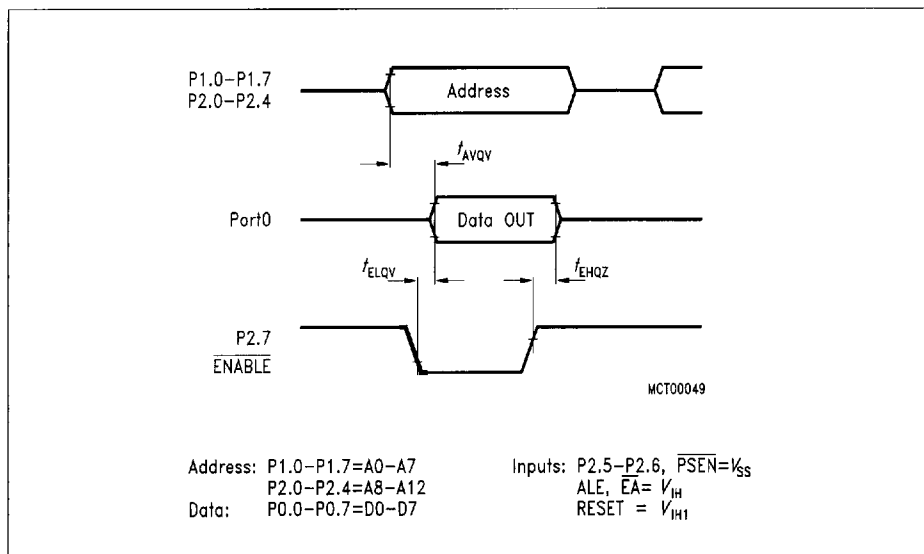


Figure 10
ROM Verification Mode 1

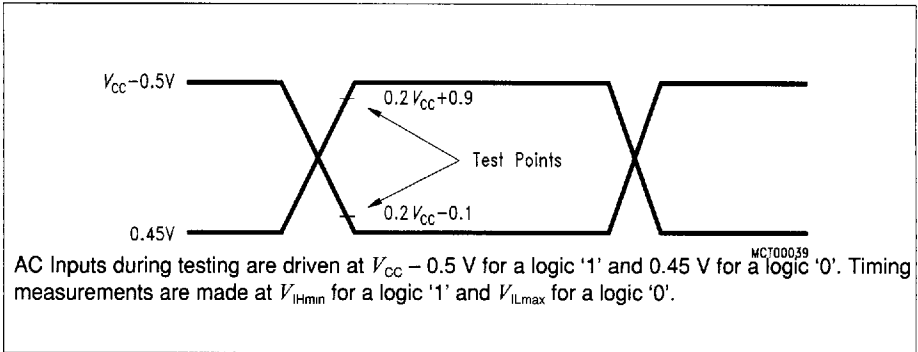


Figure 11
AC Testing: Input, Output Waveforms

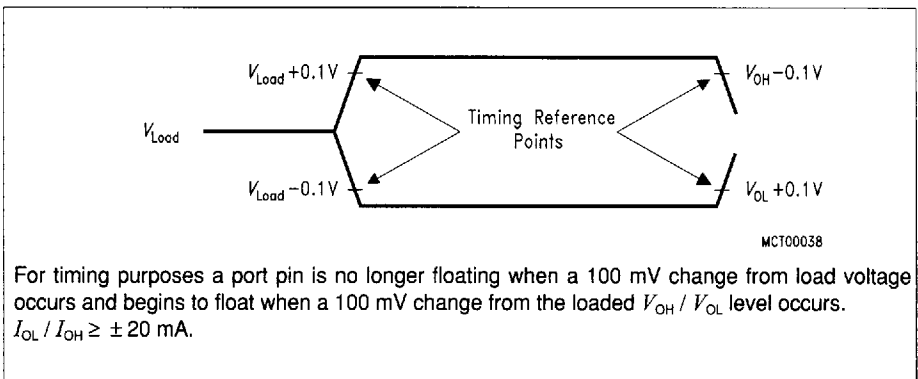


Figure 12
AC Testing: Float Waveforms

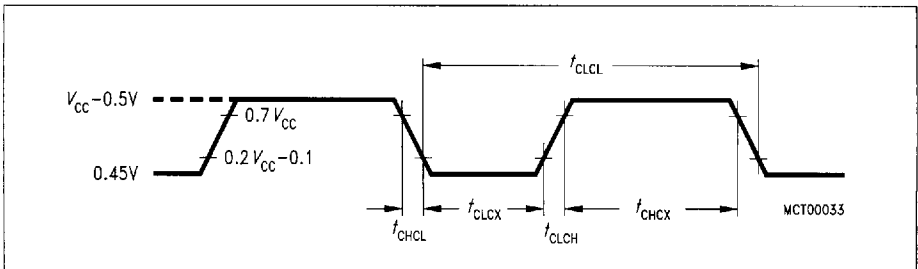


Figure 13
External Clock Cycle

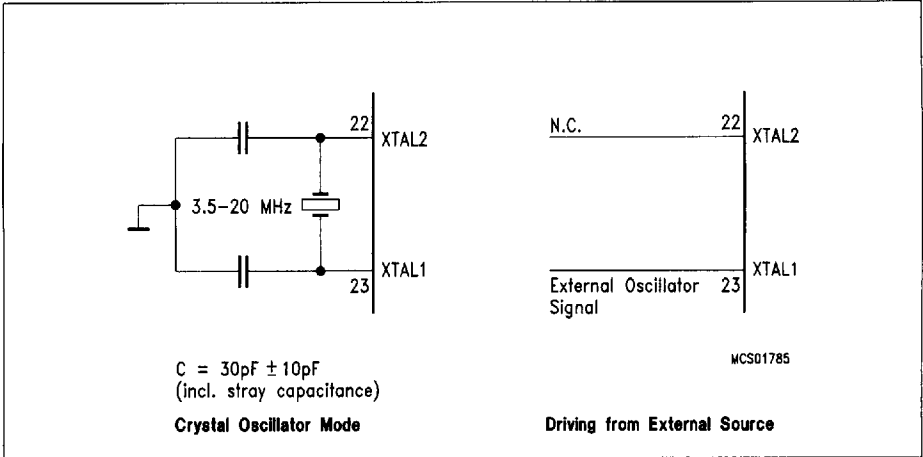


Figure 14
Recommended Oscillator Circuits