



# DATA SHEET

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## **SCN0080G\_A, SCN0080G\_B** 80-Segment Dot-matrix STN LCD Driver

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data sheet (v3)

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## 80-Segment Dot-matrix STN LCD Driver

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**1 GENERAL****1.1 Description**

The SCN0080G\_A and the SCN0080G\_B are two 80-segment dot-matrix STN LCD drivers. They are designed to be paired with the SCN6400G 64-common driver. The only difference between the SCN0080G\_A and the SCN0080G\_B is their pin assignment. The pin assignment of the SCN0080G\_B is a mirrored version of the SCN0080G\_A. Two types of pin assignments make PCB layout more flexible and increase component density.

**1.2 Features**

- 80-output segment driver for dot-matrix STN LCD.
- Display duty : 1/8 to 1/128
- Display-OFF function for reducing power consumption.
- 4-level external LCD bias voltage.
- 4-bit parallel or serial interface with a controller for display data.
- Capability of being cascaded in application to expand segment number.
- Operating voltage range (control logic): 2.7 ~ 5.5 volts.
- Operating voltage range (LCD bias voltage,  $V_{DD}-V_{EE}$ ): 8 ~ 20 volts.
- Data transfer clock: 6.0 MHz, when  $V_{DD}= 5$  volts.
- Operating temperature range: -20 to +85 °C.
- Storage temperature range: -40 to +125 °C.

**1.3 Ordering information****Table 1** Ordering information

TYPE NUMBER	DESCRIPTION
SCN0080G_A-LQFPG	LQFP100 Green package.
SCN0080G_A-QFPG	QFP100 Green package.
SCN0080G_A-LQFP	LQFP100 package.
SCN0080G_A-QFP	QFP100 package.
SCN0080G_A-D	tested die.
SCN0080G_B-LQFPG	LQFP100 Green package.
SCN0080G_B-QFPG	QFP100 Green package.
SCN0080G_B-LQFP	LQFP100 package.
SCN0080G_B-QFP	QFP100 package.
SCN0080G_B-D	tested die.

80-Segment Dot-matrix STN LCD Driver

2 FUNCTIONAL BLOCK DIAGRAM AND DESCRIPTION

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2.1 Functional block diagram

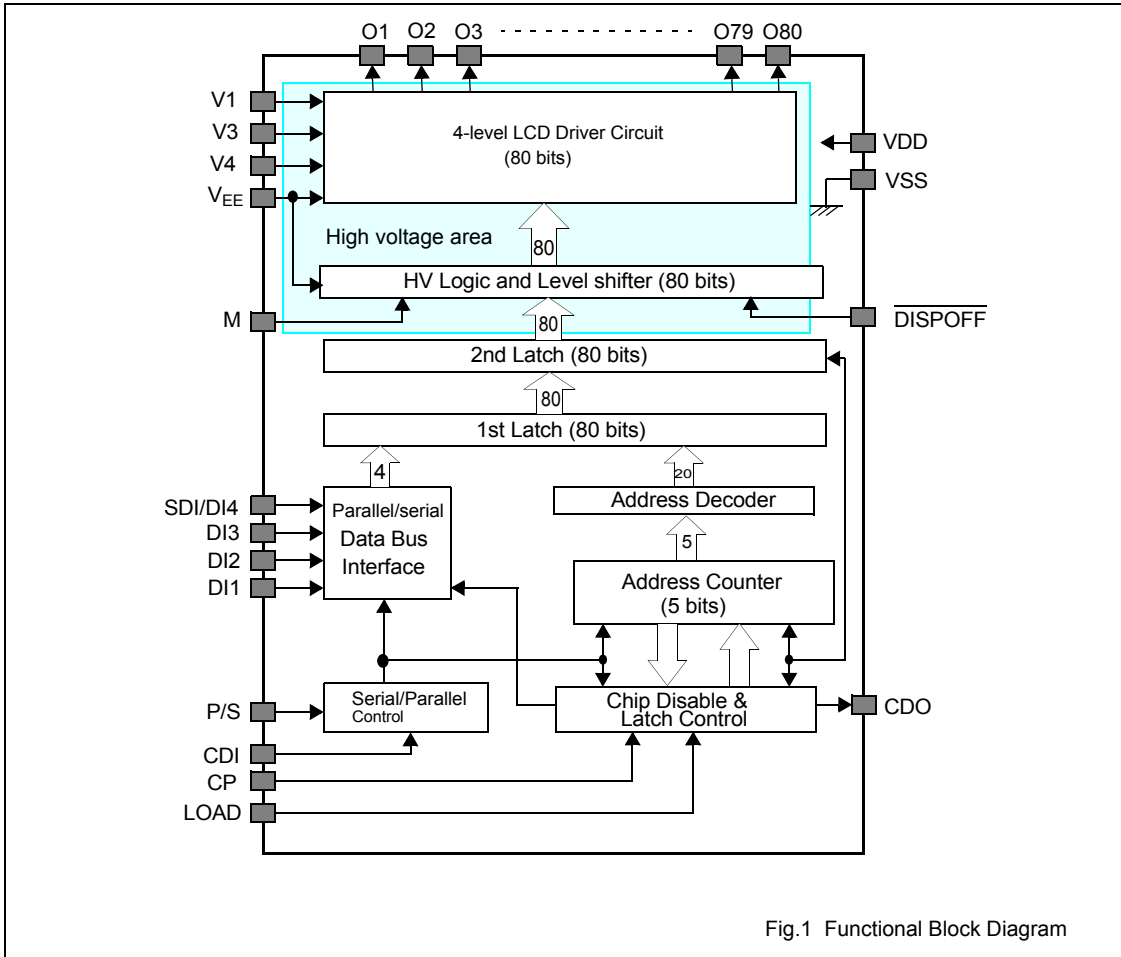
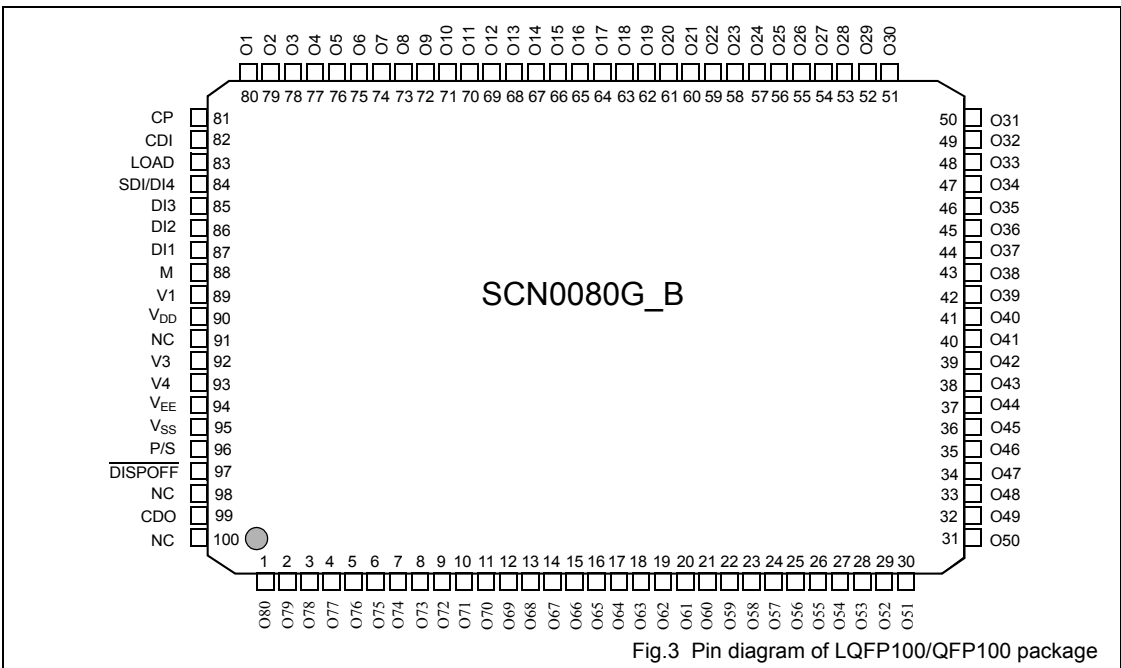
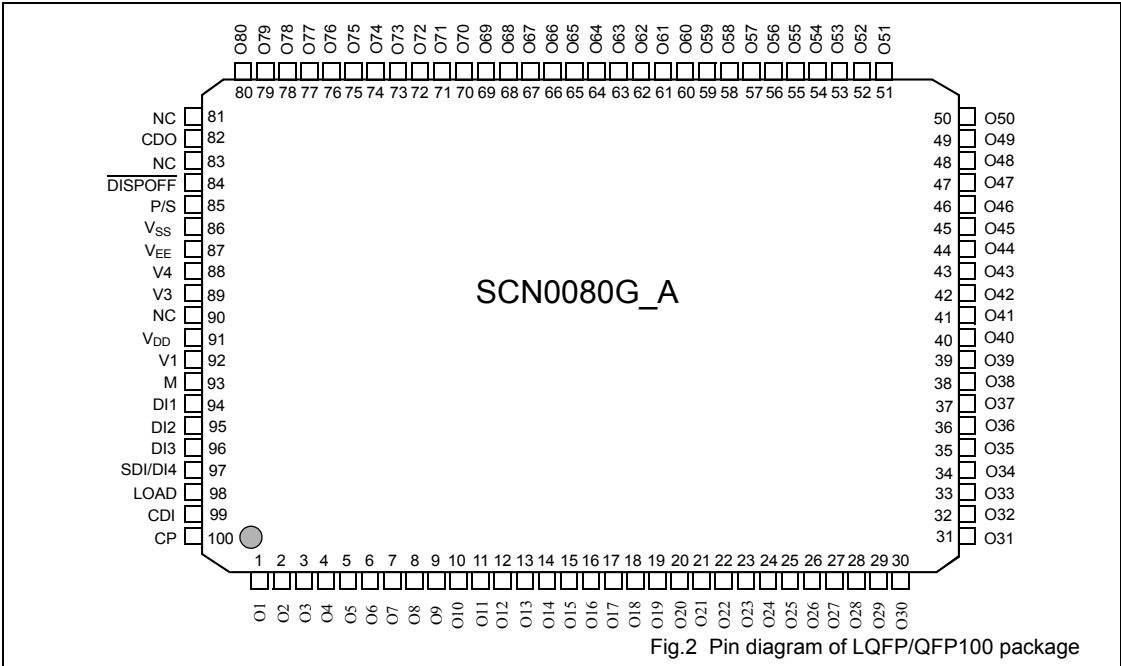


Fig.1 Functional Block Diagram

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3 PINNING INFORMATION

3.1 Pinning diagram



## 80-Segment Dot-matrix STN LCD Driver

## 3.2 Signal description

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**Table 2** Pin signal description.To avoid a latch-up effect at power-on:  $V_{SS} - 0.5\text{ V} < \text{voltage at any pin at any time} < V_{DD} + 0.5\text{ V}$ .

Pin number		SYMBOL	I/O	DESCRIPTION
SCN0080G_A	SCN0080G_B			
1~80	80~1	O1~O80	Output	Segment driver output. Please refer to Table 3 for output voltage level.
99	82	CDI	Input	Chip Disable pin. When CDI=High, on-chip data reception circuit is disabled and data can not be sent into the SCN0080G_A, SCN0080G_B. When CDI=LOW, data can be sent into the SCN0080G_A, SCN0080G_B.
92, 89, 88	89, 92, 93	V1, V3, V4	Input	LCD bias voltage. V1 and V <sub>EE</sub> are selected levels. V3 and V4 are unselected levels.
87	94	V <sub>EE</sub>	Input	Negative power supply for LCD bias.
93	88	M	Input	Frame signal, for generating alternating LCD bias voltages.
98	83	LOAD	Input	Display data (80 bits) latch clock. At the falling edge of the LOAD signal, 80-bit segment data is transferred from the first latch to the second latch for output. ( Refer to Fig. 1, Functional Block Diagram.
86	95	V <sub>SS</sub>	Input	Ground.
84	97	$\overline{\text{DISPOFF}}$	Input	Display Disable. When $\overline{\text{DISPOFF}}=\text{L}$ , the outputs O1~O81 are all at a fixed level of V1.
91	90	V <sub>DD</sub>	Input	Power supply for control logic.
85	96	P/S	Input	Selection of parallel or serial interface with a controller. When P/S= HIGH, 4-bit parallel interface is selected. When P/S=LOW, serial interface is selected.
81, 83, 90	91, 98, 100	NC		No Connection. These pins are not used in application and must be left open.

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Pin number		SYMBOL	I/O	DESCRIPTION
SCN0080G_A	SCN0080G_B			
97, 96, 95, 94	84, 85, 86, 87	SDI/DI4 ~ DI1	Input	<p>4-bit parallel data input or 1-bit serial input.</p> <p>When 4-bit parallel data bus interface is selected, the 4 bits of data are latched into the SCN0080G_A, SCN0080G_B at the falling edge of the CP clock. Please refer to Fig 4.</p> <p>When 1-bit serial interface is selected, data is input to the SDI/DI4 pin. In this interface mode, DI1~DI3 should be tied either to HIGH or to LOW.</p>
100	81	CP	Input	<p>Display data latch clock.</p> <p>4 bits of display data (DI1~DI4) are latched into the internal 80-bit latch at the falling edge of CP.</p> <p>Please refer to Fig 4.</p>
82	99	CDO	Output	Cascading output when the SCN0080G_A, SCN0080G_B are used in cascade.

**4 FUNCTIONAL DESCRIPTION**

**4.1 Segment output drive (O1~O80)**

The voltage level of the outputs O1~O80 is determined by Input data (display data), M (frame signal), and  $\overline{\text{DISPOFF}}$ , as given in the following table.

**Table 3** output voltage level of O1~O80

M	Data	$\overline{\text{DISPOFF}}$	Output
L	L	H	V3
L	H	H	V1
H	L	H	V4
H	H	H	V <sub>EE</sub>
X	X	L	V1

In the above table, X= don't care and must be tied either to H or L.

**4.2 Display Data Inputs (DI1~DI4)**

The SCN0080G\_A, SCN0080G\_B has a 4-bit parallel data bus (DI1~DI4) to interface with a controller. A logic High of a bit represents an ON cell (black pixel on the LCD screen).

**Table 4** Data bits

Display data	LCD drive output	LCD display
H	Selected level (V1, V <sub>EE</sub> )	ON
L	Unselected level (V3, V4)	OFF

**4.3 Sequence of data input when 4-bit parallel interface is selected.**

When 4-bit parallel interface mode is selected, the 4-bit data that is first latched goes to O77 ~ O80 and the 4-bit data that is last latched goes to O1 ~ O4.

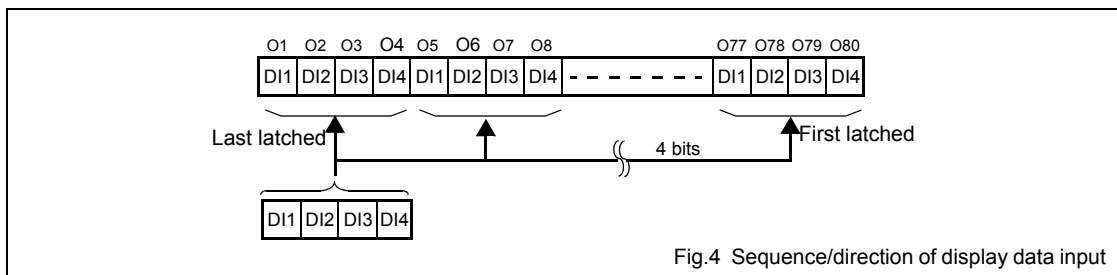


Fig.4 Sequence/direction of display data input

## 80-Segment Dot-matrix STN LCD Driver

## 5 ABSOLUTE MAXIMUM RATING

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Table 5 Absolute maximum rating

$V_{DD} = 5\text{ V} \pm 10\%$ ;  $V_{SS} = 0\text{ V}$ ; all voltages with respect to  $V_{SS}$  unless otherwise specified;  $T_{amb} = 25 \pm 2^\circ\text{C}$ .

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$V_{DD}$	Voltage on the $V_{DD}$ input	-0.3	+7.0	V
$V_{DD}-V_{EE}$	LCD bias voltage, note 1	0	22	V
$V_i(\text{max})$	Maximum input voltage to input pins	-0.3	$V_{DD} + 0.3$	V
$T_{amb}$	Operating ambient temperature range	-20	+ 85	$^\circ\text{C}$
$T_{stg}$	Storage temperature range	-40	+125	$^\circ\text{C}$

**Note:**

1. The condition  $V_{DD} \geq V1 > V3 > V4 > V_{EE}$  must always be met.



## 80-Segment Dot-matrix STN LCD Driver

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## 6 DC CHARACTERISTICS

Table 6 DC Characteristics

$V_{DD} = 5\text{ V} \pm 10\%$ ;  $V_{SS} = 0\text{ V}$ ; all voltages with respect to  $V_{SS}$  unless otherwise specified;  $T_{amb} = 25 \pm 2\text{ }^{\circ}\text{C}$ .

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{DD}$	Supply voltage for control logic	Please refer to Fig. 14 for DC power-up sequence.	2.7	5.0	5.5	V
$V_{DD}-V_{EE}$	LCD bias voltage	Note 1.	8		20	
$V_{IL}$	Input LOW voltage of input pins	D11~SDI/DI4, CP, LOAD, CDI, P/S, M, DISPOFF	0		$0.2V_{DD}$	V
$V_{IH}$	Input HIGH voltage of input pins	D11~SDI/DI4, CP, LOAD, CDI, P/S, M, DISPOFF	$0.8V_{DD}$		$V_{DD}$	V
$I_{IL}$	Input LOW leakage current of input pins (i. e. Reverse leakage current of input ESD protection diode)	$V_{IN}=V_{SS}$ , LOAD, CP, CDI, P/S, D11~SDI/DI4, M, DISPOFF			1	$\mu\text{A}$
$I_{IH}$	Input HIGH leakage current of input pins (i. e. Reverse leakage current of input protection diode)	$V_{IN}=V_{DD}$ , LOAD, CP, CDI, P/S, D11~SDI/DI4, M, DISPOFF			1	$\mu\text{A}$
$V_{OL}$	Output LOW voltage level of the CDO pin	$I_{OL}=400\mu\text{A}$	0.0		0.4	V
$V_{OH}$	Output HIGH voltage level of the CDO pin	$I_{OH}=-400\mu\text{A}$	$V_{DD} - 0.4$		$V_{DD}$	V
$I_{STBY}$	Standby current	Note 2.			200	$\mu\text{A}$
$I_{SS}$	Operating current ( $V_{DD}$ to $V_{SS}$ )	Note 3.			1.0	mA
$I_{EE}$	Operating current ( $V_{DD}$ to $V_{EE}$ )	Note 4.			0.1	mA
$C_i$	Input capacitance of the CP pin	The CP clock frequency is 3.3 MHz.		5.0		pF
$R_{ON}$	Driver ON resistance at $V_{LCD}=18\text{ V}$ (HV transmission transistors of O1~O80)	Note 5.		2.0	4.0	$\text{K}\Omega$

## Notes:

1. The condition  $V_{DD} \geq V1 > V3 > V4 > V_{EE}$  must always be met.
2.  $CDI=V_{DD}$ ,  $V_{DD}-V_{EE}=18\text{ V}$ ,  $CP=3.3\text{ MHz}$ , Output unloaded; measured at the  $V_{SS}$  pin.
3. Condition for the measurement:  $V_{LCD}=V_{DD}-V_{EE}=18\text{ V}$ ,  $CP=3.3\text{ MHz}$ ,  $LOAD=5.156\text{ KHz}$ ,  $M=52\text{ Hz}$ . This is the current flowing from  $V_{DD}$  to  $V_{SS}$ , measured at the  $V_{SS}$  pin.
4. Condition for the measurement:  $V_{LCD}=V_{DD}-V_{EE}=18\text{ V}$ ,  $CP=3.3\text{ MHz}$ ,  $LOAD=5.156\text{ KHz}$ ,  $M=52\text{ Hz}$ . This is the current flowing from  $V_{DD}$  to  $V_{EE}$ , measured at the  $V_{EE}$  pin.
5. Condition for the measurement:  $V_{DD}-V_{EE}=18\text{ V}$ ,  $|V_{DE}-V_O|=0.25\text{ V}$ , where  $V_{DE} =$  one of V1, V3, V4, or  $V_{EE}$ .  $V1=V_{DD}$ ,  $V3 = (9/11) \times (V_{DD}-V_{EE})$ ,  $V4 = (2/11) \times (V_{DD}-V_{EE})$ . For the driver circuits (O1~O80), please refer to Section 14, Pin Circuits.

7 AC CHARACTERISTICS

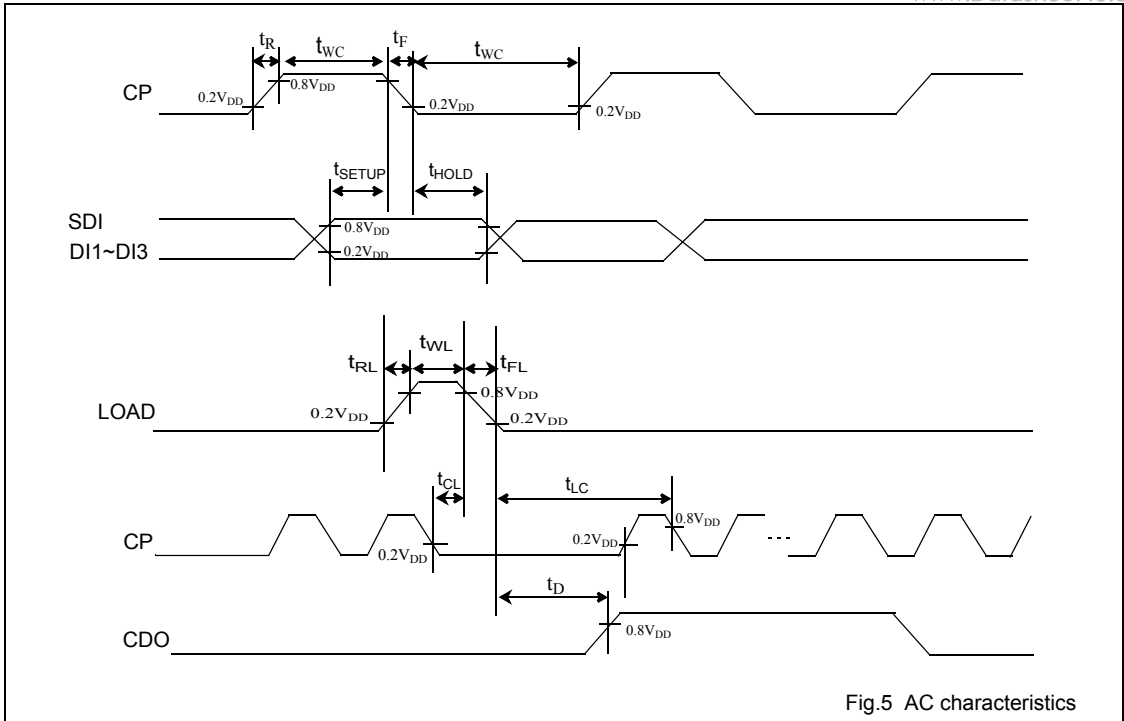


Fig.5 AC characteristics

Table 7 AC Characteristics

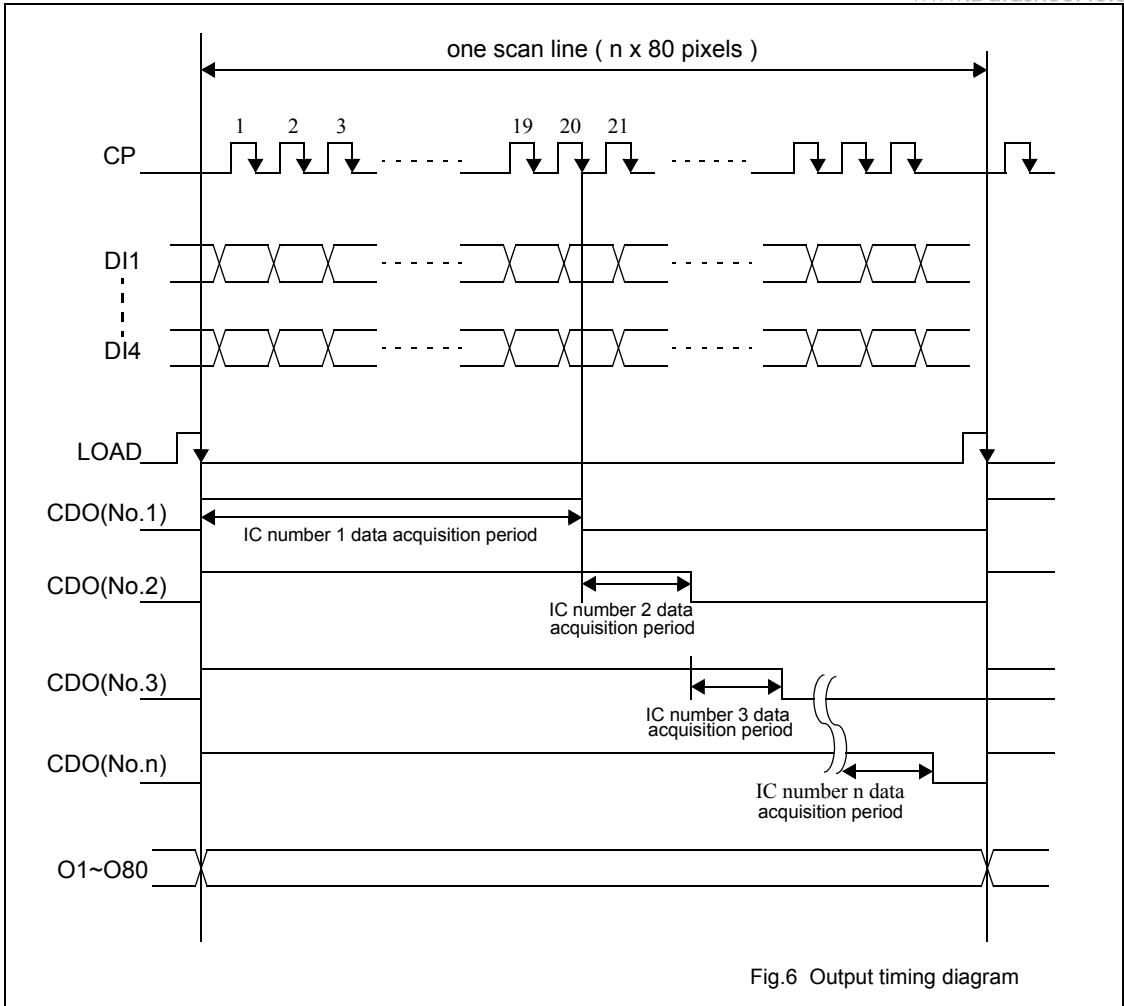
$V_{DD} = 5\text{ V} \pm 10\%$ ;  $V_{SS} = 0\text{ V}$ ; all voltages with respect to  $V_{SS}$  unless otherwise specified;  $T_{amb} = 25 \pm 2\text{ }^\circ\text{C}$ .

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$f_{CP}$	CP clock frequency			3.6	MHz
$T_{WC}$	CP clock pulse width		90		ns
$T_{WL}$	LOAD clock pulse width		90		ns
$t_{SETUP}$	Input data setup time	DI1~SDI/DI4 data to the falling edge of the CP clock.	60		ns
$t_{HOLD}$	Input data hold time.	Falling edge of the CP clock to DI1~SDI/DI4 data change.	60		ns
$t_{CL}$	CP to LOAD		80		ns
$t_{LC}$	LOAD to CP		80		ns
$t_R$	CP rise time			40	ns
$t_F$	CP fall time			40	ns
$t_{RL}$	Load rise time			40	
$t_{FL}$	Load fall time			40	
$t_D$	Output delay time	the CDO pin, Load=30 pF.		180	ns

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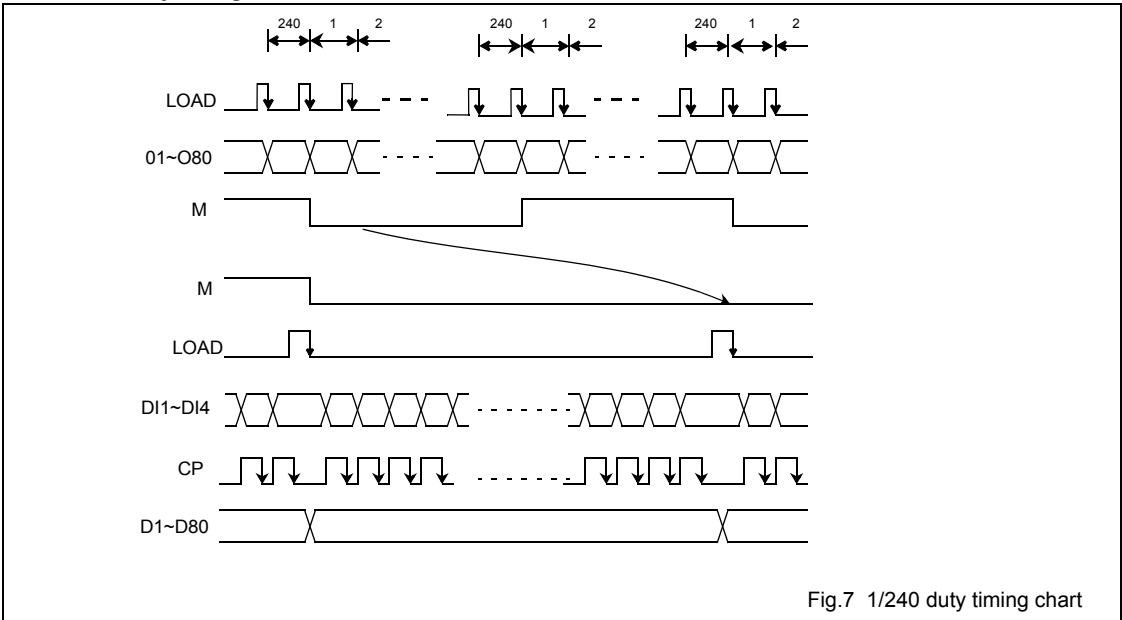
8 OUTPUT TIMING DIAGRAM

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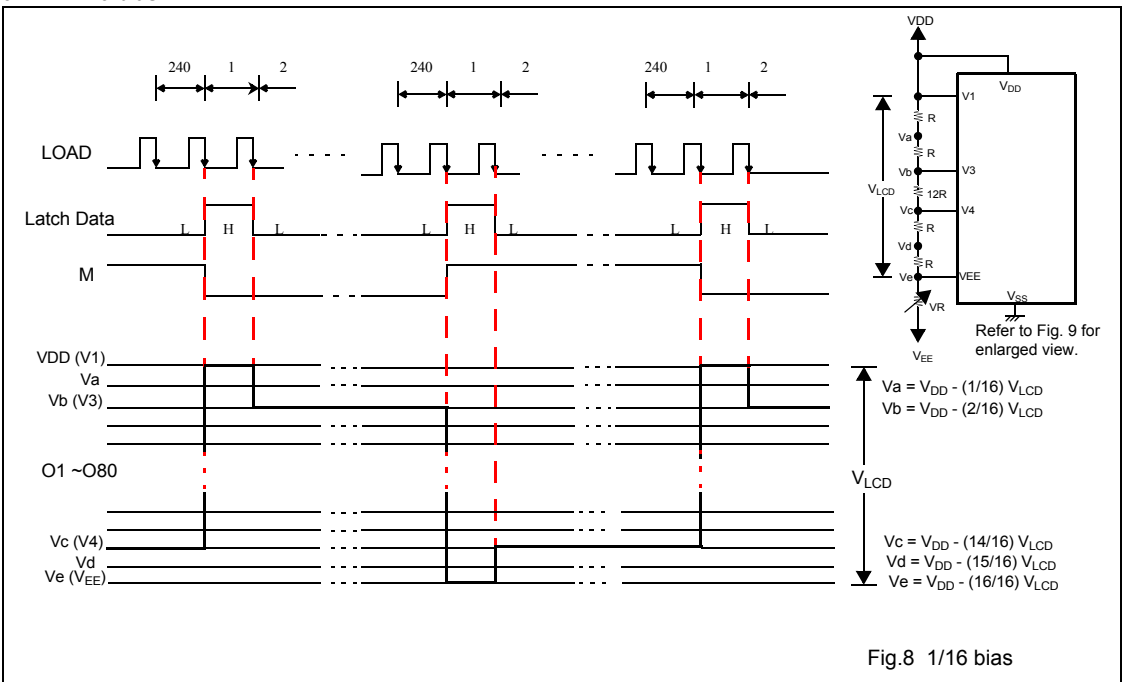


9 TIMING CHART ( 1/240 DUTY, 1/16 BIAS)

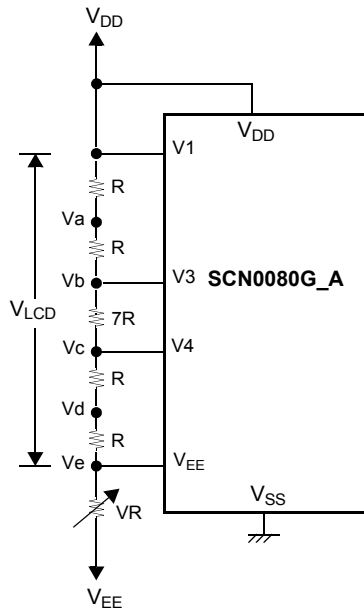
9.1 1/240 duty timing chart



9.2 1/16 bias



9.3 Bias circuit



$$V_a = V_{DD} - (1/11) V_{LCD}$$

$$V_b = V_{DD} - (2/11) V_{LCD}$$

$$V_c = V_{DD} - (9/11) V_{LCD}$$

$$V_d = V_{DD} - (10/11) V_{LCD}$$

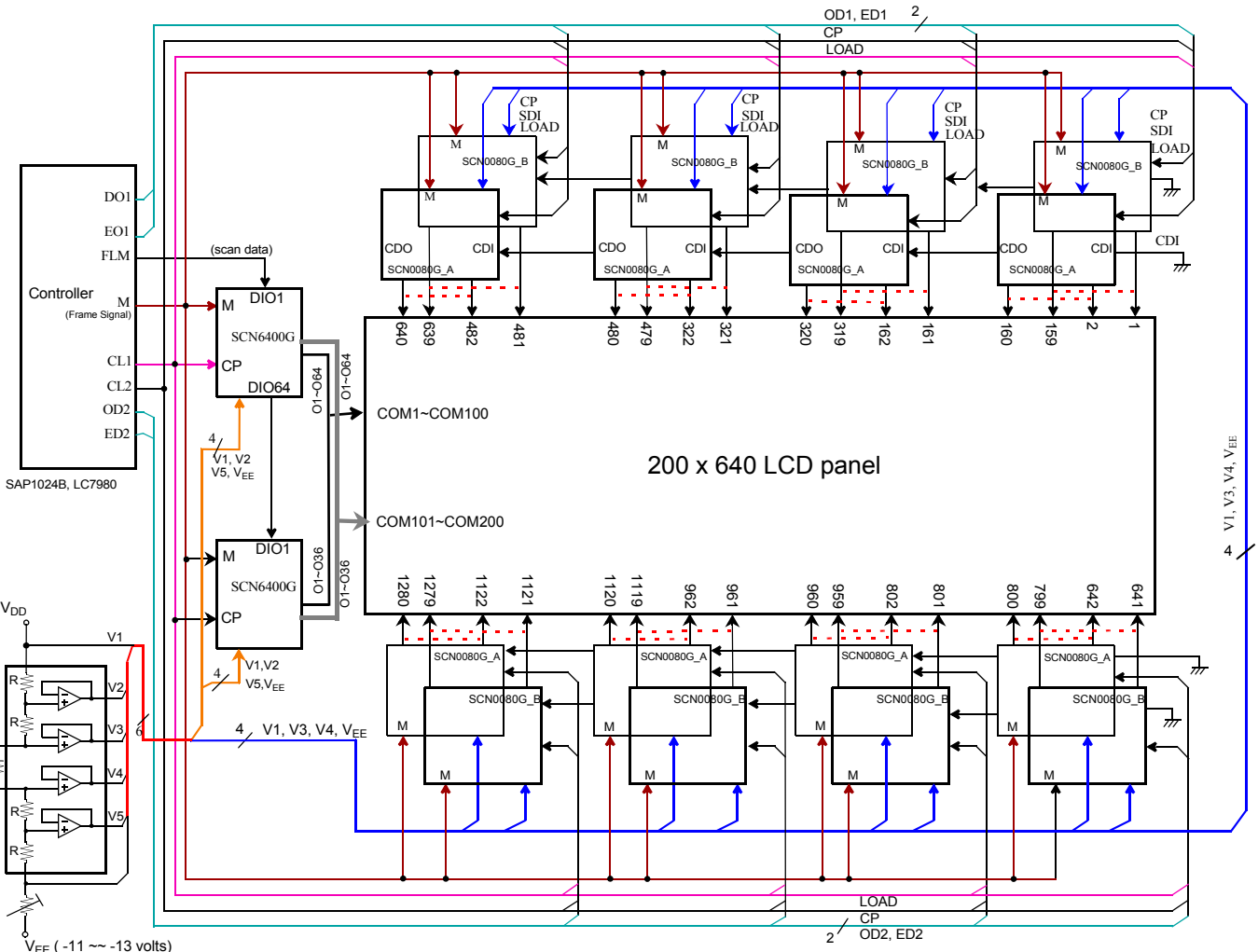
$$V_e = V_{DD} - (11/11) V_{LCD}$$

Bias for the SCN0080G\_B is the same as that for the SCN0080G\_A.

Fig.9 LCD bias voltage

# 80-Segment Dot-matrix STN LCD Driver

## 10 200 X 640 APPLICATION

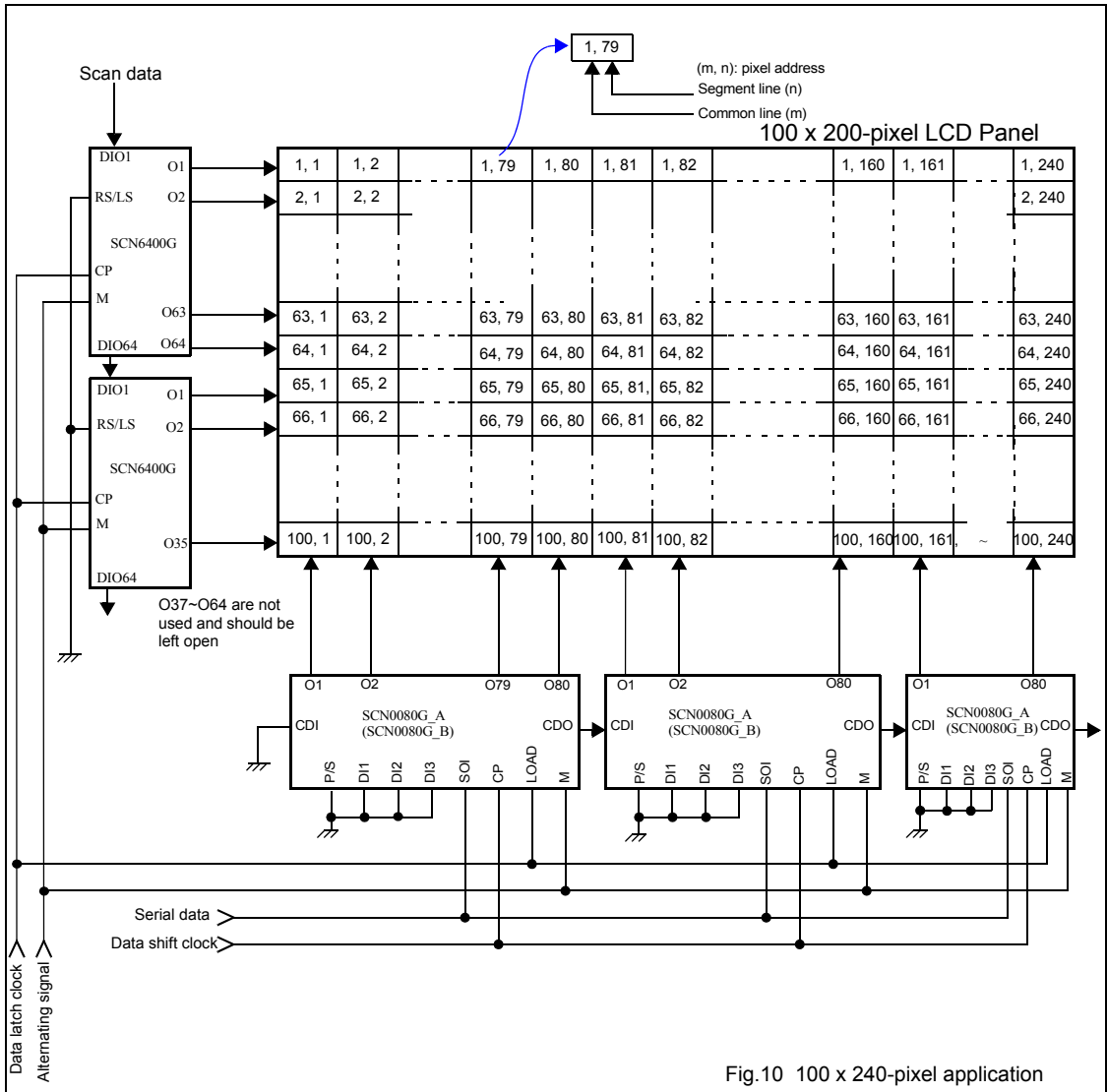


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11 100 X 240-PIXEL APPLICATION

The following diagram illustrates an example of using three SCN0080G\_A (or SCN0080G\_B) and two SCN6400G to design a 100 x 240-dots LCD panel. The duty cycle of the design is 1/100. For cascading application, Cascading Output (CDO) of the previous chip should be connected to the Cascading Input of the next chip.



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12 TIMING DIAGRAM FOR 100 X 240-PIXEL APPLICATION

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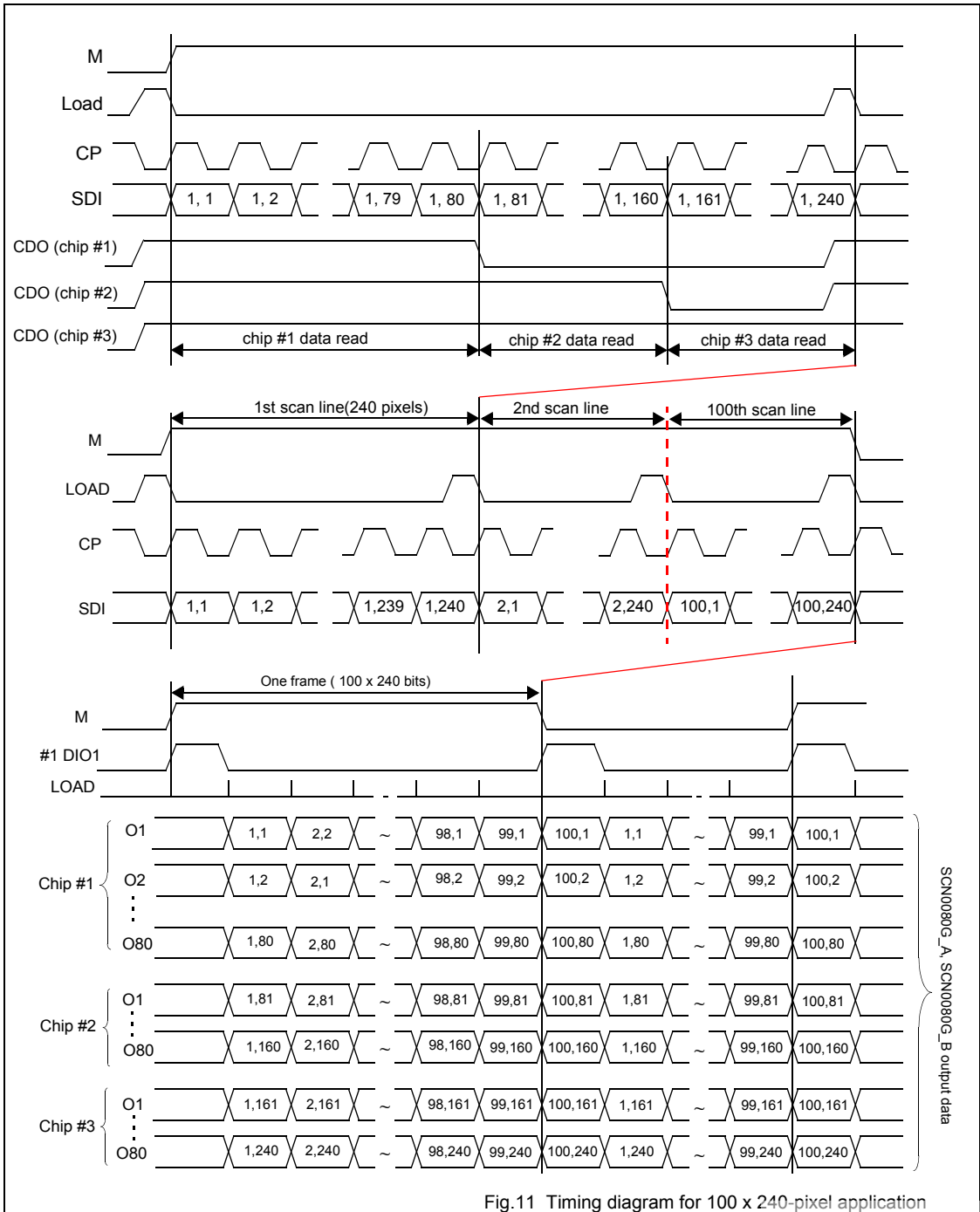


Fig.11 Timing diagram for 100 x 240-pixel application

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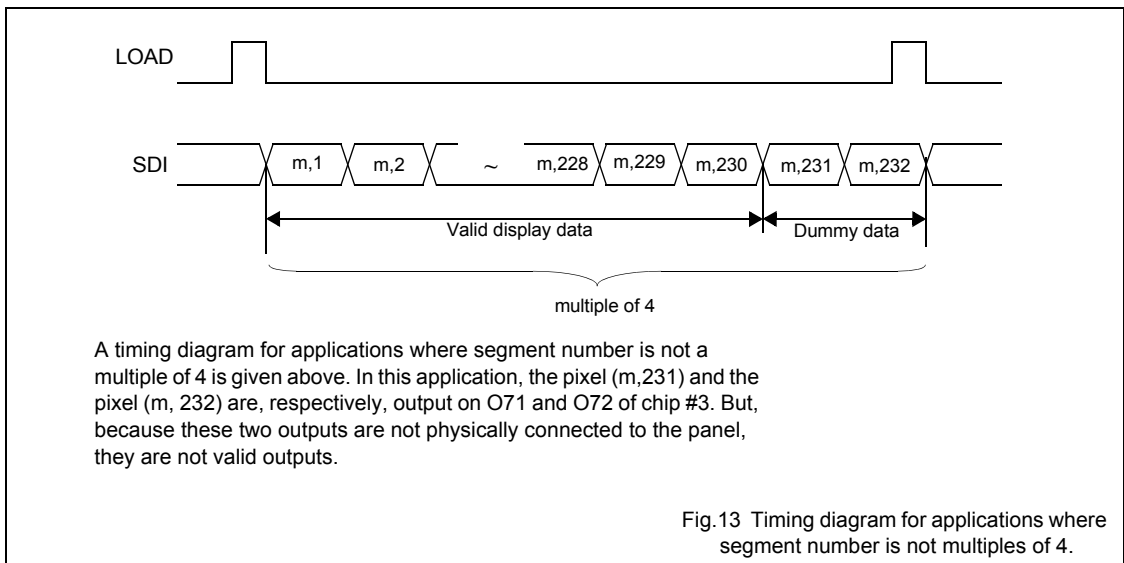
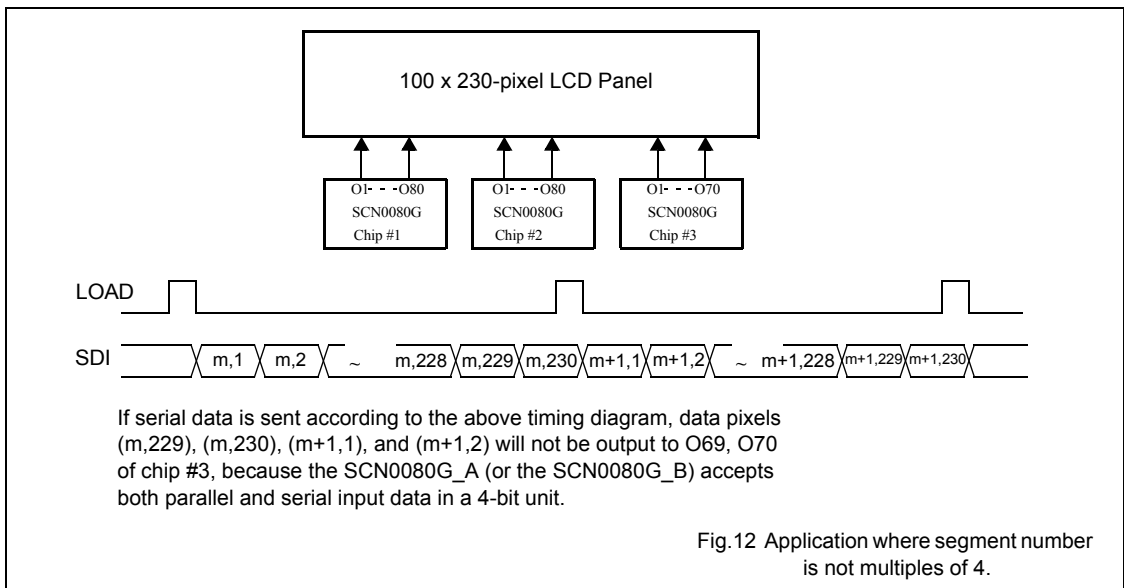


## 80-Segment Dot-matrix STN LCD Driver

## SCN0080G\_A, SCN0080G\_B

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## 13 APPLICATIONS WHERE SEGMENT DATA IS NOT A MULTIPLE OF 4



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SCN0080G\_A, SCN0080G\_B

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14 PIN CIRCUITS

Table 8 MOS-level schematics of all input, output, and I/O pins.

SYMBOL	Input/output	CIRCUIT	NOTES
CDO	Output		
CP, LOAD, DI1~SDI/DI4, P/S, M, CDI, DISPOFF	Inputs		
O1~O80, V1, V3, V4, VEE	Driver outputs, High voltage inputs		

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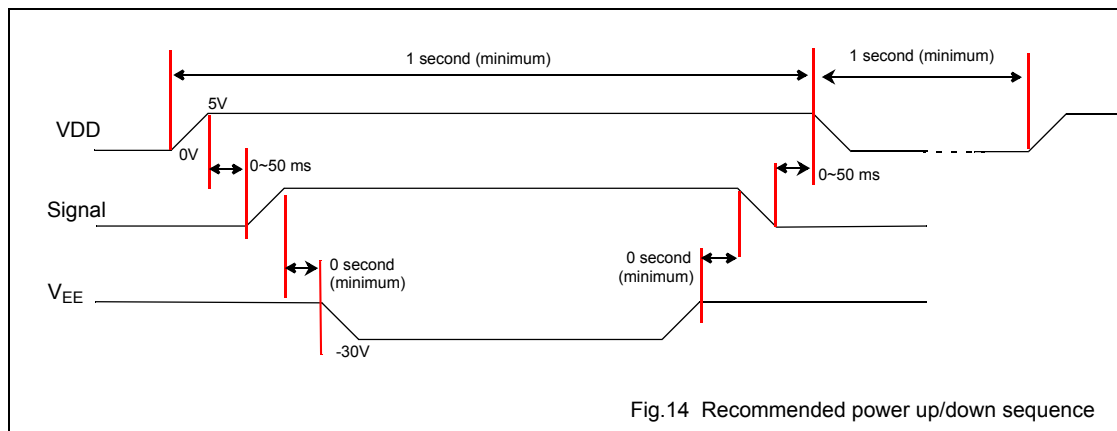
## 80-Segment Dot-matrix STN LCD Driver

## SCN0080G\_A, SCN0080G\_B

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**15 APPLICATION NOTES**

1. It is recommended that the following power-up sequence be followed to ensure reliable operation of your display system. As the ICs are fabricated in CMOS and there is intrinsic latch-up problem associated with any CMOS devices, proper power-up sequence can reduce the danger of triggering latch-up. When powering up the system, control logic power must be powered on first. When powering down the system, control logic must be shut off later than or at the same time with the LCD bias ( $V_{EE}$ ).



SYMBOLS	MIN.	NOM	MAX.
A	-	-	3.40
A1	0.25	-	0.50
A2	2.50	2.70	2.90
b	0.22	-	0.40
c	0.11	-	0.23
D	23.20 BASIC		
D1	20.00 BASIC		
e	0.65 BASIC		
E	17.20 BASIC		
E1	14.00 BASIC		
L	0.73	0.88	1.03
L1	-	1.60	-
$\theta^\circ$	0	-	7

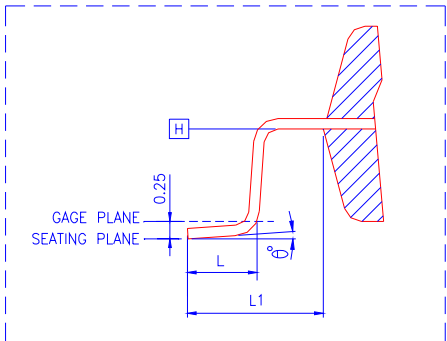
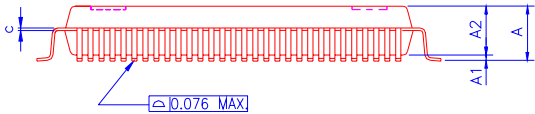
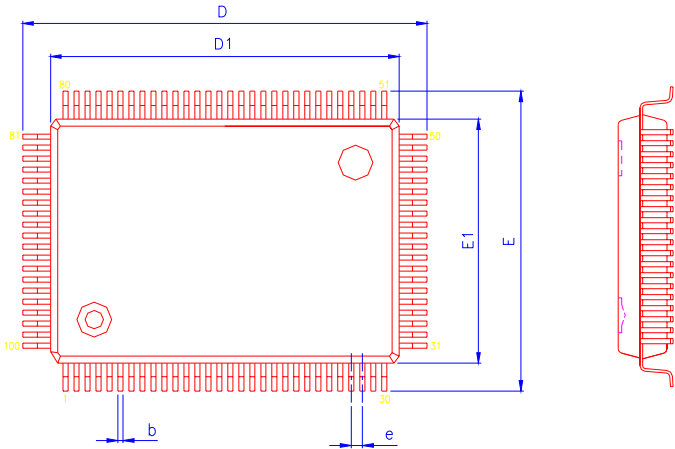
UNIT : mm

NOTES:

- 1.JEDEC OUTLINE:MS-022 GC-1
- 2.DATUM PLANE  $\square$  IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- 3.DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE  $\square$ .
- 4.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION .

SCN0080G\_A  
QFP100 Package Outline Drawing

16 PACKAGE INFORMATION



# 80-Segment Dot-matrix STN LCD Driver

# SCN0080G\_A, SCN0080G\_B

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## 17 SOLDERING

### 17.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. For more in-depth account of soldering ICs, please refer to dedicated reference materials.

### 17.2 Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, please contact Avant for drypack information.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

### 17.3 Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

**If wave soldering cannot be avoided, the following conditions must be observed:**

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

### 17.4 Repairing soldered joints

Fix the component by first soldering two diagonally- opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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**80-Segment Dot-matrix STN LCD Driver****SCN0080G\_A, SCN0080G\_B**

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