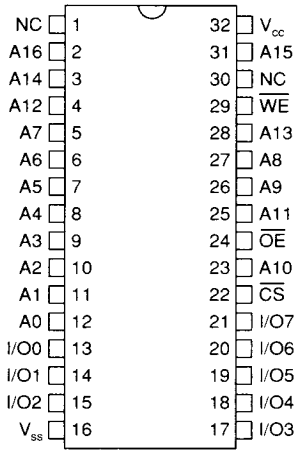


FIGURE 1 — Pin Configuration

A0 - A16	Address Inputs
I/O0 - I/O7	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	+5.0V Power
V_{SS}	Ground

Pin Description

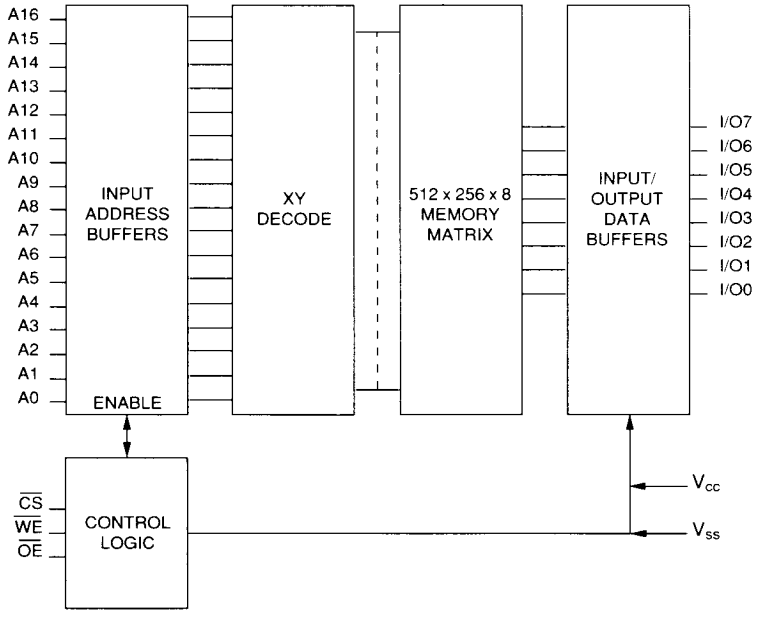


FIGURE 2 — Block Diagram

WS-128K8 CX

128K x 8 BIT CMOS SRAM

FEATURES

- **5 Volt Operation**
- **All CMOS Fully Static Design, No Clock**
- **Hermetic Ceramic Package**
- **Wide Range of Access Times**
- **Battery Back-Up Operation**
- **Military Temperature Range (-55°C to +125°C)**
- **Industrial and Commercial Screening Available**
- **TTL Compatible Inputs and Outputs**
- **JEDEC Approved Pinout and Outline**

DESCRIPTION

The White Technology model WS-128K8 is a CMOS SRAM housed in a hermetically sealed ceramic 32 pin package. Featuring JEDEC standard pinouts, the device provides 128K bytes of read/write low power memory. The device is well suited for battery backed operation and will retain data at voltages as low as 2.0 volts.

Designed for use in demanding applications, the memory packaging and construction is well suited for military and severe industrial applications. Screening and burn in are to military standards.

The advanced 128K x 8 SRAM is constructed using co-fired ceramic packaging and high density CMOS memory. The module also features internal power supply bypass capacitors to enhance performance.

Inputs and outputs are TTL compatible. The logic levels and drive capabilities permit the memory to interface with most digital logic systems. Since the device is all CMOS, low power operation for standby applications such as battery backed systems is straightforward. (continued)

DESCRIPTION (continued)

The memory features low power consumption. In typical systems where multiple modules are operating using chip select to activate each device, the overall current requirement is only slightly above that for one unit. Those units not selected require only standby current.

Since the device is a fully static memory, refreshing is not needed. The memory read and write cycles are compatible with virtually all microprocessors. The maximum read and write access time from address change or chip enable is as specified.

The rugged ceramic package features a welded metal cover and co-fired construction to assure maximum integrity and hermetic seal. The package is designed and rated to meet military specifications.

The memory has seventeen address lines, A0 through A16. These lines combine to select a specific byte from the memory array of 128K (131,072 bytes). The data input and output share a common read/write data bus I/O0 through I/O7. Additional control lines with inverse sense logic are $\overline{CS}$ (Chip Select), $\overline{WE}$ (Write Enable), and $\overline{OE}$ (Output Enable).

When asserted low, the chip enable line selects the memory and permits response to the write enable and output enable lines. When the chip enable line is high, the memory is deactivated and current drain is sharply reduced. The write enable line permits data storage to the memory when asserted low. To present the data to the I/O bus, the output enable line is asserted low. When this line is high, the output of the memory is set to high impedance and no data is presented to the I/O bus.

The timing diagrams of Figures 4 and 5 illustrate the preferred timing sequence and timing specifications for the memory. The output enable line is high during write cycles while the write enable line is high during read cycles.

The memory is designed to operate and interface with TTL and CMOS logic levels. The memory will also retain data at lower levels of V_{CC}.

ABSOLUTE MAXIMUM RATINGS

Operating Temperature WS-128K8-XXX CM	-55°C to +125°C
Storage Temperature Range	-65°C to + 150°C
Supply Voltage	-0.5V to 7.0V
Signal Voltages Any Pin	-0.5V to 7.0V

RECOMMENDED OPERATING CONDITIONS

Parameter	Sym.	Min.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC}+.3	V
Input Low Voltage	V_{IL} (1)	-0.5	0.8	V
Operating Temp. (Mil.)	T_A	-55	+125	°C

(1) V_{IL} (min.) = -3.0V for pulse width less than 20 ns.

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0-A16	Mode	Data I/O	Device Current
H	X	X	X	Standby	High Z	Standby
L	L	H	Stable	Read	Data Out	Active
L	X	L	Stable	Write	Data In	Active
L	H	H	Stable	Out Disable	High Z	Active

NOTES

1. All voltages referenced to V_{SS} (Gnd).
2. All I/O transitions are measured ±200 mV from steady state with loading as specified in "A.C. Test Circuits."
3. Typical limits are at V_{CC} = 5.0V, T_A = 25°C, with specified loading.

DC AND OPERATING CHARACTERISTICS

(V_{CC} = 5V, V_{SS} = 0V, T_A = -55°C TO 125°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Leakage Current	I_{LI}	V_{CC} = Max., V_{IN} = Gnd. or V_{CC}			15	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = Gnd. to V_{CC}			15	µA
Static Supply Current	I_{CC1}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, Duty Cycle = 0			1.0	mA
Dynamic Supply Current	I_{CC2}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max.			30	mA
Standby Current	I_{SB1}	$\overline{CS}$ = V_{CC}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max.			1.0	mA
Output Low Voltage	V_{OL}	I_{OL} = 2.1 mA			0.4	V
Output High Voltage	V_{OH}	I_{OH} = -1.0 mA	2.4			V
* Input Capacitance	C_{IN}	V_{IN} = 0V, f = 1.0 MHz			40	pF
* Output Capacitance	C_{OUT}	V_{OUT} = 0V, f = 1.0 MHz			40	pF

DATA RETENTION CHARACTERISTICS

(T_A = -55°C TO 125°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Data Retention Supply Voltage	V_{DR}	$\overline{CS} \geq V_{CC}$ -.2V	2.0		5.5	V
Data Retention Current	I_{CCDR1}	V_{CC} = 3V		1.0	400	µA
	I_{CCDR2}	V_{CC} = 2V		1.0	300	µA

AC CHARACTERISTICS

(V_{CC} = 5V, V_{SS} = 0V, T_A = -55°C TO 125°C)

Parameter	Symbol		Min.	Typ.	Max.	Unit
Read Cycle Time	t_{RC}	Figure 4, (1)	120			nS
Address Access Time	t_{AA}	Figure 4, (2)			120	nS
$\overline{CS}$ Access Time	t_{ACS}	Figure 4, (3)			120	nS
Output Hold from Address Change	t_{OH}	Figure 4, (4)	15			nS
Chip Select to Output in Low Z	t_{CLZ}	Figure 4, (5)	10			nS
Chip Select to Output in High Z	t_{CHZ}	Figure 4, (6)			50	nS
Output Enable to Output Valid	t_{OE}	Figure 4, (7)			60	nS
Output Enable to Output in Low Z	t_{OLZ}	Figure 4, (8)	5			nS
Output Enable to Output in High Z	t_{OHZ}	Figure 4, (9)			50	nS
Write Cycle Time	t_{WC}	Figure 5, (10)	120			nS
Address Setup Time	t_{AS}	Figure 5, (11)	0			nS
Write Pulse Width	t_{WP}	Figure 5, (12)	80			nS
Write Recovery Time	t_{WR}	Figure 5, (13)	0			nS
Write Enable to Output in High Z	t_{WHZ}	Figure 5, (14)	0		50	nS
Data Valid to End of Write	t_{DW}	Figure 5, (15)	50			nS
Data Hold Time	t_{DH}	Figure 5, (16)	0			nS
Output Active from End of $\overline{WE}$	t_{OW}	Figure 5, (16)	10			nS
Address Valid to End of Write	t_{AW}	Figure 5, (17)	85			nS
Input Pulse Levels			0		3	V
Input Rise and Fall Times					5	nS
Input Timing Reference Level				1.5		V
Output Reference Level				1.5		V
Output Load		See Figure 3				

*** GUARANTEED BUT NOT TESTED.**

DC AND OPERATING CHARACTERISTICS

(V_{CC} = 5V, V_{SS} = 0V, T_A = -55°C TO 125°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Leakage Current	I_{LI}	V_{CC} = Max., V_{IN} = Gnd. or V_{CC}			15	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = Gnd. to V_{CC}			15	µA
Static Supply Current	I_{CC1}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, Duty Cycle = 0			1.0	mA
Dynamic Supply Current	I_{CC2}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max.			30	mA
Standby Current	I_{SB1}	$\overline{CS}$ = V_{CC}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max.			1.0	mA
Output Low Voltage	V_{OL}	I_{OL} = 2.1 mA			0.4	V
Output High Voltage	V_{OH}	I_{OH} = -1.0 mA	2.4			V
* Input Capacitance	C_{IN}	V_{IN} = 0V, f = 1.0 MHz			40	pF
* Output Capacitance	C_{OUT}	V_{OUT} = 0V, f = 1.0 MHz			40	pF

DATA RETENTION CHARACTERISTICS

(T_A = -55°C TO 125°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Data Retention Supply Voltage	V_{DR}	$\overline{CS} \geq V_{CC}$ -.2V	2.0		5.5	V
Data Retention Current	I_{CCDR1}	V_{CC} = 3V		1.0	400	µA
	I_{CCDR2}	V_{CC} = 2V		1.0	300	µA

AC CHARACTERISTICS

(V_{CC} = 5V, V_{SS} = 0V, T_A = -55°C TO 125°C)

Parameter	Symbol		Min.	Typ.	Max.	Unit
Read Cycle Time	t_{RC}	Figure 4, (1)	100			nS
Address Access Time	t_{AA}	Figure 4, (2)			100	nS
$\overline{CS}$ Access Time	t_{ACS}	Figure 4, (3)			100	nS
Output Hold from Address Change	t_{OH}	Figure 4, (4)	15			nS
Chip Select to Output in Low Z	t_{CLZ}	Figure 4, (5)	10			nS
Chip Select to Output in High Z	t_{CHZ}	Figure 4, (6)			50	nS
Output Enable to Output Valid	t_{OE}	Figure 4, (7)			60	nS
Output Enable to Output in Low Z	t_{OLZ}	Figure 4, (8)	5			nS
Output Enable to Output in High Z	t_{OHZ}	Figure 4, (9)			50	nS
Write Cycle Time	t_{WC}	Figure 5, (10)	100			nS
Address Setup Time	t_{AS}	Figure 5, (11)	0			nS
Write Pulse Width	t_{WP}	Figure 5, (12)	70			nS
Write Recovery Time	t_{WR}	Figure 5, (13)	0			nS
Write Enable to Output in High Z	t_{WHZ}	Figure 5, (14)	0		50	nS
Data Valid to End of Write	t_{DW}	Figure 5, (15)	50			nS
Data Hold Time	t_{DH}	Figure 5, (16)	0			nS
Output Active from End of $\overline{WE}$	t_{OW}	Figure 5, (16)	10			nS
Address Valid to End of Write	t_{AW}	Figure 5, (17)	75			nS
Input Pulse Levels			0		3	V
Input Rise and Fall Times					5	nS
Input Timing Reference Level				1.5		V
Output Reference Level				1.5		V
Output Load		See Figure 3				

*** GUARANTEED BUT NOT TESTED.**

DC AND OPERATING CHARACTERISTICS

(V_{CC} = 5V, V_{SS} = 0V, T_A = -55°C TO 125°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Leakage Current	I_{LI}	V_{CC} = Max., V_{IN} = Gnd. or V_{CC}			15	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = Gnd. to V_{CC}			15	µA
Static Supply Current	I_{CC1}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, Duty Cycle = 0			1.0	mA
Dynamic Supply Current	I_{CC2}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max.			30	mA
Standby Current	I_{SB1}	$\overline{CS}$ = V_{CC}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max.			1.0	mA
Output Low Voltage	V_{OL}	I_{OL} = 2.1 mA			0.4	V
Output High Voltage	V_{OH}	I_{OH} = -1.0 mA	2.4			V
* Input Capacitance	C_{IN}	V_{IN} = 0V, f = 1.0 MHz			40	pF
* Output Capacitance	C_{OUT}	V_{OUT} = 0V, f = 1.0 MHz			40	pF

DATA RETENTION CHARACTERISTICS

(T_A = -55°C TO 125°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Data Retention Supply Voltage	V_{DR}	$\overline{CS} \geq V_{CC}$ -.2V	2.0		5.5	V
Data Retention Current	I_{CCDR1}	V_{CC} = 3V		1.0	400	µA
	I_{CCDR2}	V_{CC} = 2V		1.0	300	µA

AC CHARACTERISTICS

(V_{CC} = 5V, V_{SS} = 0V, T_A = -55°C TO 125°C)

Parameter	Symbol		Min.	Typ.	Max.	Unit
Read Cycle Time	t_{RC}	Figure 4, (1)	85			nS
Address Access Time	t_{AA}	Figure 4, (2)			85	nS
$\overline{CS}$ Access Time	t_{ACS}	Figure 4, (3)			85	nS
Output Hold from Address Change	t_{OH}	Figure 4, (4)	15			nS
Chip Select to Output in Low Z	t_{CLZ}	Figure 4, (5)	10			nS
Chip Select to Output in High Z	t_{CHZ}	Figure 4, (6)			45	nS
Output Enable to Output Valid	t_{OE}	Figure 4, (7)			55	nS
Output Enable to Output in Low Z	t_{OLZ}	Figure 4, (8)	5			nS
Output Enable to Output in High Z	t_{OHZ}	Figure 4, (9)			45	nS
Write Cycle Time	t_{WC}	Figure 5, (10)	85			nS
Address Setup Time	t_{AS}	Figure 5, (11)	0			nS
Write Pulse Width	t_{WP}	Figure 5, (12)	65			nS
Write Recovery Time	t_{WR}	Figure 5, (13)	0			nS
Write Enable to Output in High Z	t_{WHZ}	Figure 5, (14)	0		45	nS
Data Valid to End of Write	t_{DW}	Figure 5, (15)	45			nS
Data Hold Time	t_{DH}	Figure 5, (16)	0			nS
Output Active from End of $\overline{WE}$	t_{OW}	Figure 5, (16)	10			nS
Address Valid to End of Write	t_{AW}	Figure 5, (17)	75			nS
Input Pulse Levels			0		3	V
Input Rise and Fall Times					5	nS
Input Timing Reference Level				1.5		V
Output Reference Level				1.5		V
Output Load		See Figure 3				

*** GUARANTEED BUT NOT TESTED.**

DC AND OPERATING CHARACTERISTICS

(V_{CC} = 5V, V_{SS} = 0V, T_A = -55°C TO 125°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Leakage Current	I_{LI}	V_{CC} = Max., V_{IN} = Gnd. or V_{CC}			15	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = Gnd. to V_{CC}			15	µA
Static Supply Current	I_{CC1}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, Duty Cycle = 0			1.0	mA
Dynamic Supply Current	I_{CC2}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max.			60	mA
Standby Current	I_{SB1}	$\overline{CS}$ = V_{CC}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max.			1.0	mA
Output Low Voltage	V_{OL}	I_{OL} = 2.1 mA			0.4	V
Output High Voltage	V_{OH}	I_{OH} = -1.0 mA	2.4			V
* Input Capacitance	C_{IN}	V_{IN} = 0V, f = 1.0 MHz			40	pF
* Output Capacitance	C_{OUT}	V_{OUT} = 0V, f = 1.0 MHz			40	pF

DATA RETENTION CHARACTERISTICS

(T_A = -55°C TO 125°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Data Retention Supply Voltage	V_{DR}	$\overline{CS} \geq V_{CC}$ -.2V	2.0		5.5	V
Data Retention Current	I_{CCDR1}	V_{CC} = 3V		5.0	400	µA
	I_{CCDR2}	V_{CC} = 2V		5.0	300	µA

AC CHARACTERISTICS

(V_{CC} = 5V, V_{SS} = 0V, T_A = -55°C TO 125°C)

Parameter	Symbol		Min.	Typ.	Max.	Unit
Read Cycle Time	t_{RC}	Figure 4, (1)	70			nS
Address Access Time	t_{AA}	Figure 4, (2)			70	nS
$\overline{CS}$ Access Time	t_{ACS}	Figure 4, (3)			70	nS
Output Hold from Address Change	t_{OH}	Figure 4, (4)	5			nS
Chip Select to Output in Low Z	t_{CLZ}	Figure 4, (5)	5			nS
Chip Select to Output in High Z	t_{CHZ}	Figure 4, (6)			40	nS
Output Enable to Output Valid	t_{OE}	Figure 4, (7)			50	nS
Output Enable to Output in Low Z	t_{OLZ}	Figure 4, (8)	5			nS
Output Enable to Output in High Z	t_{OHZ}	Figure 4, (9)			40	nS
Write Cycle Time	t_{WC}	Figure 5, (10)	70			nS
Address Setup Time	t_{AS}	Figure 5, (11)	0			nS
Write Pulse Width	t_{WP}	Figure 5, (12)	40			nS
Write Recovery Time	t_{WR}	Figure 5, (13)	0			nS
Write Enable to Output in High Z	t_{WHZ}	Figure 5, (14)	0		40	nS
Data Valid to End of Write	t_{DW}	Figure 5, (15)	40			nS
Data Hold Time	t_{DH}	Figure 5, (16)	0			nS
Output Active from End of $\overline{WE}$	t_{OW}	Figure 5, (16)	10			nS
Address Valid to End of Write	t_{AW}	Figure 5, (17)	50			nS
Input Pulse Levels			0		3	V
Input Rise and Fall Times					5	nS
Input Timing Reference Level				1.5		V
Output Reference Level				1.5		V
Output Load		See Figure 3				

*** GUARANTEED BUT NOT TESTED.**

DC AND OPERATING CHARACTERISTICS

(V_{CC} = 5V, V_{SS} = 0V, T_A = -55°C TO 125°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Leakage Current	I_{LI}	V_{CC} = Max., V_{IN} = Gnd. or V_{CC}			15	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = Gnd. to V_{CC}			15	µA
Static Supply Current	I_{CC1}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, Duty Cycle = 0			1.0	mA
Dynamic Supply Current	I_{CC2}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max.			60	mA
Standby Current	I_{SB1}	$\overline{CS}$ = V_{CC}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max.			1.0	mA
Output Low Voltage	V_{OL}	I_{OL} = 2.1 mA			0.4	V
Output High Voltage	V_{OH}	I_{OH} = -1.0 mA	2.4			V
* Input Capacitance	C_{IN}	V_{IN} = 0V, f = 1.0 MHz			40	pF
* Output Capacitance	C_{OUT}	V_{OUT} = 0V, f = 1.0 MHz			40	pF

DATA RETENTION CHARACTERISTICS

(T_A = -55°C TO 125°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Data Retention Supply Voltage	V_{DR}	$\overline{CS} \geq V_{CC}$ -.2V	2.0		5.5	V
Data Retention Current	I_{CCDR1}	V_{CC} = 3V			400	µA
	I_{CCDR2}	V_{CC} = 2V			300	µA

AC CHARACTERISTICS

(V_{CC} = 5V, V_{SS} = 0V, T_A = -55°C TO 125°C)

Parameter	Symbol		Min.	Typ.	Max.	Unit
Read Cycle Time	t_{RC}	Figure 4, (1)	55			nS
Address Access Time	t_{AA}	Figure 4, (2)			55	nS
$\overline{CS}$ Access Time	t_{ACS}	Figure 4, (3)			55	nS
Output Hold from Address Change	t_{OH}	Figure 4, (4)	5			nS
Chip Select to Output in Low Z	t_{CLZ}	Figure 4, (5)	5			nS
Chip Select to Output in High Z	t_{CHZ}	Figure 4, (6)			35	nS
Output Enable to Output Valid	t_{OE}	Figure 4, (7)			40	nS
Output Enable to Output in Low Z	t_{OLZ}	Figure 4, (8)	5			nS
Output Enable to Output in High Z	t_{OHZ}	Figure 4, (9)			30	nS
Write Cycle Time	t_{WC}	Figure 5, (10)	55			nS
Address Setup Time	t_{AS}	Figure 5, (11)	0			nS
Write Pulse Width	t_{WP}	Figure 5, (12)	40			nS
Write Recovery Time	t_{WR}	Figure 5, (13)	0			nS
Write Enable to Output in High Z	t_{WHZ}	Figure 5, (14)	0		30	nS
Data Valid to End of Write	t_{DW}	Figure 5, (15)	30			nS
Data Hold Time	t_{DH}	Figure 5, (16)	0			nS
Output Active from End of $\overline{WE}$	t_{OW}	Figure 5, (16)	5			nS
Address Valid to End of Write	t_{AW}	Figure 5, (17)	50			nS
Input Pulse Levels			0		3	V
Input Rise and Fall Times					5	nS
Input Timing Reference Level				1.5		V
Output Reference Level				1.5		V
Output Load		See Figure 3				

*** GUARANTEED BUT NOT TESTED.**

DC AND OPERATING CHARACTERISTICS

(V_{CC} = 5V, V_{SS} = 0V, T_A = -55°C TO 125°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Leakage Current	I_{LI}	V_{CC} = Max., V_{IN} = Gnd. or V_{CC}			15	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = Gnd. to V_{CC}			15	µA
Static Supply Current	I_{CC1}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, Duty Cycle = 0			2.5	mA
Dynamic Supply Current	I_{CC2}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max.			70	mA
Standby Current	I_{SB1}	$\overline{CS}$ = V_{CC}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max.			15	mA
Output Low Voltage	V_{OL}	I_{OL} = 2.1			0.4	V
Output High Voltage	V_{OH}	I_{OH} = 1.0	2.4			V
* Input Capacitance	C_{IN}	V_{IN} = 0V, f = 1.0 MHz			40	pF
* Output Capacitance	C_{OUT}	V_{OUT} = 0V, f = 1.0 MHz			40	pF

DATA RETENTION CHARACTERISTICS

(T_A = -55°C TO 125°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Data Retention Supply Voltage	V_{DR}	$\overline{CS} \geqq V_{CC}$ -.2V	2.0		5.5	V
Data Retention Current	I_{CCDR1}	V_{CC} = 3V		15	900	µA
	I_{CCDR2}	V_{CC} = 2V		10	600	µA

AC CHARACTERISTICS

(V_{CC} = 5V, V_{SS} = 0V, T_A = -55°C TO 125°C)

Parameter	Symbol		Min.	Typ.	Max.	Unit
Read Cycle Time	t_{RC}	Figure 4, (1)	45			nS
Address Access Time	t_{AA}	Figure 4, (2)			45	nS
$\overline{CS}$ Access Time	t_{ACS}	Figure 4, (3)			45	nS
Output Hold from Address Change	t_{OH}	Figure 4, (4)	5			nS
Chip Select to Output in Low Z	t_{CLZ}	Figure 4, (5)	5			nS
Chip Select to Output in High Z	t_{CHZ}	Figure 4, (6)			30	nS
Output Enable to Output Valid	t_{OE}	Figure 4, (7)			35	nS
Output Enable to Output in Low Z	t_{OLZ}	Figure 4, (8)	5			nS
Output Enable to Output in High Z	t_{OHZ}	Figure 4, (9)			25	nS
Write Cycle Time	t_{WC}	Figure 5, (10)	45			nS
Address Setup Time	t_{AS}	Figure 5, (11)	0			nS
Write Pulse Width	t_{WP}	Figure 5, (12)	30			nS
Write Recovery Time	t_{WR}	Figure 5, (13)	0			nS
Write Enable to Output in High Z	t_{WHZ}	Figure 5, (14)	0		25	nS
Data Valid to End of Write	t_{DW}	Figure 5, (15)	25			nS
Data Hold Time	t_{DH}	Figure 5, (16)	0			nS
Output Active from End of $\overline{WE}$	t_{OW}	Figure 5, (16)	5			nS
Address Valid to End of Write	t_{AW}	Figure 5, (17)	30			nS
Input Pulse Levels			0		3	V
Input Rise and Fall Times					5	nS
Input Timing Reference Level				1.5		V
Output Reference Level				1.5		V
Output Load		See Figure 3				

*** GUARANTEED BUT NOT TESTED.**

DC AND OPERATING CHARACTERISTICS

(V_{CC} = 5V, V_{SS} = 0V, T_A = -55°C TO 125°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Leakage Current	I_{LI}	V_{CC} = Max., V_{IN} = Gnd. or V_{CC}			15	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = Gnd. to V_{CC}			15	µA
Static Supply Current	I_{CC1}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, Duty Cycle = 0			25	mA
Dynamic Supply Current	I_{CC2}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max.			150	mA
Standby Current	I_{SB1}	$\overline{CS}$ = V_{CC}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max.			40	mA
Output Low Voltage	V_{OL}	I_{OL} = 8 mA, V_{CC} = Min.			0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4 mA, V_{CC} = Min.	2.2			V
* Input Capacitance	C_{IN}	V_{IN} = 0V, f = 1.0 MHz			40	pF
* Output Capacitance	C_{OUT}	V_{OUT} = 0V, f = 1.0 MHz			40	pF

DATA RETENTION CHARACTERISTICS

(T_A = -55°C TO 125°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Data Retention Supply Voltage	V_{DR}	$\overline{CS} \geq V_{CC}$ -.2V	2.0		5.5	V
Data Retention Current	I_{CCDR1}	V_{CC} = 3V		.10	3.5	mA
	I_{CCDR2}	V_{CC} = 2V		.05	2.0	mA

AC CHARACTERISTICS

(V_{CC} = 5V, V_{SS} = 0V, T_A = -55°C TO 125°C)

Parameter	Symbol		Min.	Typ.	Max.	Unit
Read Cycle Time	t_{RC}	Figure 4, (1)	35			nS
Address Access Time	t_{AA}	Figure 4, (2)			35	nS
$\overline{CS}$ Access Time	t_{ACS}	Figure 4, (3)			35	nS
Output Hold from Address Change	t_{OH}	Figure 4, (4)	5			nS
Chip Select to Output in Low Z	t_{CLZ}	Figure 4, (5)	5			nS
Chip Select to Output in High Z	t_{CHZ}	Figure 4, (6)			20	nS
Output Enable to Output Valid	t_{OE}	Figure 4, (7)			25	nS
Output Enable to Output in Low Z	t_{OLZ}	Figure 4, (8)	5			nS
Output Enable to Output in High Z	t_{OHZ}	Figure 4, (9)			20	nS
Write Cycle Time	t_{WC}	Figure 5, (10)	35			nS
Address Setup Time	t_{AS}	Figure 5, (11)	0			nS
Write Pulse Width	t_{WP}	Figure 5, (12)	25			nS
Write Recovery Time	t_{WR}	Figure 5, (13)	0			nS
Write Enable to Output in High Z	t_{WHZ}	Figure 5, (14)	0		20	nS
Data Valid to End of Write	t_{DW}	Figure 5, (15)	20			nS
Data Hold Time	t_{DH}	Figure 5, (16)	0			nS
Output Active from End of $\overline{WE}$	t_{OW}	Figure 5, (16)	5			nS
Address Valid to End of Write	t_{AW}	Figure 5, (17)	25			nS
Input Pulse Levels			0		3	V
Input Rise and Fall Times					5	nS
Input Timing Reference Level				1.5		V
Output Reference Level				1.5		V
Output Load		See Figure 3				

*** GUARANTEED BUT NOT TESTED.**

DC AND OPERATING CHARACTERISTICS

(V_{CC} = 5V, V_{SS} = 0V, T_A = -55°C TO 125°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Leakage Current	I_{LI}	V_{CC} = Max., V_{IN} = Gnd. or V_{CC}			15	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = Gnd. to V_{CC}			15	µA
Static Supply Current	I_{CC1}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, Duty Cycle = 0			25	mA
Dynamic Supply Current	I_{CC2}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max.			150	mA
Standby Current	I_{SB1}	$\overline{CS}$ = V_{CC}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max.			40	mA
Output Low Voltage	V_{OL}	I_{OL} = 8 mA, V_{CC} = Min.			0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4 mA, V_{CC} = Min.	2.4			V
* Input Capacitance	C_{IN}	V_{IN} = 0V, f = 1.0 MHz			40	pF
* Output Capacitance	C_{OUT}	V_{OUT} = 0V, f = 1.0 MHz			40	pF

DATA RETENTION CHARACTERISTICS

(T_A = -55°C TO 125°C)

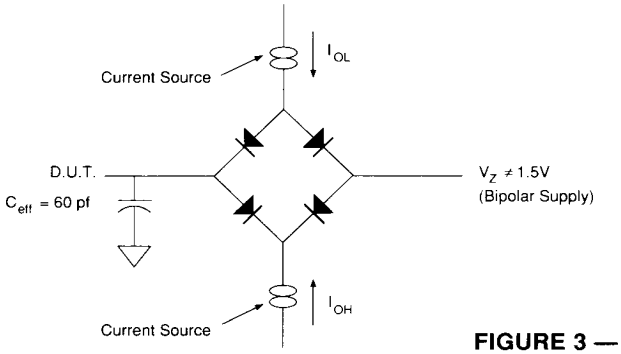
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Data Retention Supply Voltage	V_{DR}	$\overline{CS} \geq V_{CC}$ -.2V	2.0		5.5	V
Data Retention Current	I_{CCDR1}	V_{CC} = 3V		.1	3.5	mA
	I_{CCDR2}	V_{CC} = 2V		.05	2.0	mA

AC CHARACTERISTICS

(V_{CC} = 5V, V_{SS} = 0V, T_A = -55°C TO 125°C)

Parameter	Symbol		Min.	Typ.	Max.	Unit
Read Cycle Time	t_{RC}	Figure 4, (1)	25			nS
Address Access Time	t_{AA}	Figure 4, (2)			25	nS
$\overline{CS}$ Access Time	t_{ACS}	Figure 4, (3)			25	nS
Output Hold from Address Change	t_{OH}	Figure 4, (4)	5			nS
Chip Select to Output in Low Z	t_{CLZ}	Figure 4, (5)	5			nS
Chip Select to Output in High Z	t_{CHZ}	Figure 4, (6)			15	nS
Output Enable to Output Valid	t_{OE}	Figure 4, (7)			20	nS
Output Enable to Output in Low Z	t_{OLZ}	Figure 4, (8)	5			nS
Output Enable to Output in High Z	t_{OHZ}	Figure 4, (9)			15	nS
Write Cycle Time	t_{WC}	Figure 5, (10)	25			nS
Address Setup Time	t_{AS}	Figure 5, (11)	0			nS
Write Pulse Width	t_{WP}	Figure 5, (12)	20			nS
Write Recovery Time	t_{WR}	Figure 5, (13)	0			nS
Write Enable to Output in High Z	t_{WHZ}	Figure 5, (14)	0		15	nS
Data Valid to End of Write	t_{DW}	Figure 5, (15)	15			nS
Data Hold Time	t_{DH}	Figure 5, (16)	0			nS
Output Active from End of $\overline{WE}$	t_{OW}	Figure 5, (16)	5			nS
Address Valid to End of Write	t_{AW}	Figure 5, (17)	20			nS
Input Pulse Levels			0		3	V
Input Rise and Fall Times					5	nS
Input Timing Reference Level				1.5		V
Output Reference Level				1.5		V
Output Load		See Figure 3				

*** GUARANTEED BUT NOT TESTED.**



V_Z		Programmable from -2V to +7V
I_{OL} & I_{OH}		Programmable from 0 to 16 mA
		Tester Impedance $Z_O = 75\ \Omega$
		V_Z is typically the midpoint of V_{OH} and V_{OL} (i.e. (2.4 + 0.4)/2 = ± 1.4 V)
		I_{OL} and I_{OH} are adjusted to simulate a typical resistive load circuit.
Notes:	D.U.T.	Device Under Test
	C_{eff}	Effective Capacitance
		ATE Tester Includes Jig Capacitance

FIGURE 3 — AC Test Circuit

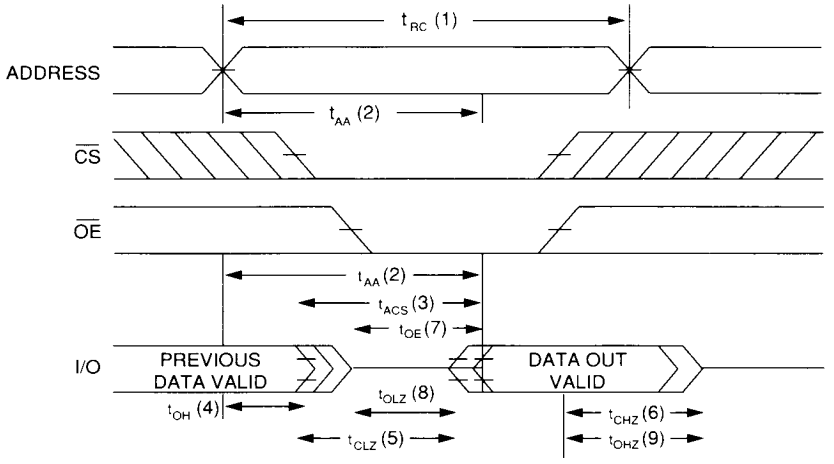


FIGURE 4 — Read Cycle Timing Diagram

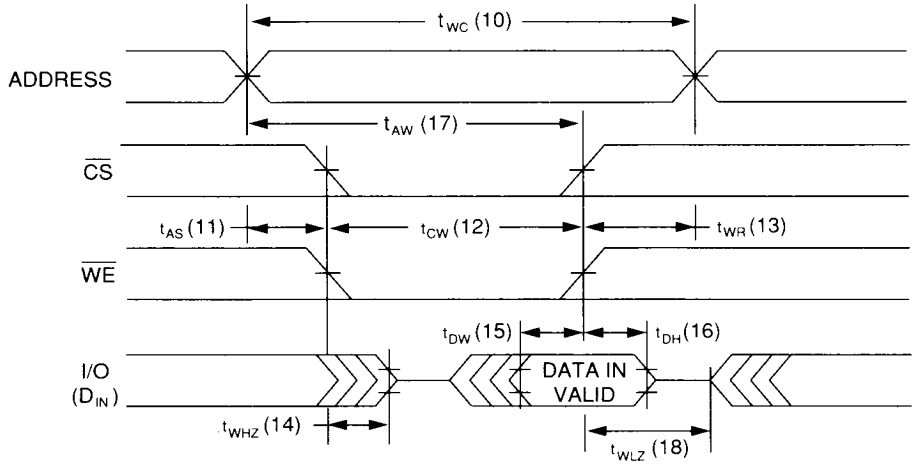


FIGURE 5 — Write Cycle Timing Diagram

ORDERING INFORMATION

TEMPERATURE RANGE OPTIONS

M	Military	-55°C to +125°C
I	Industrial	-40°C to +85°C
C	Commercial	0°C to +70°C

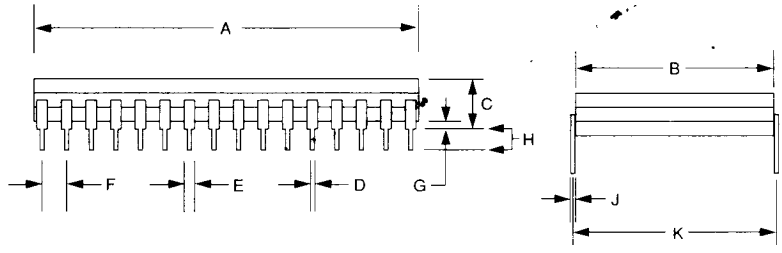
W S - 128K 8 - XXX C X

- PROCESSING:
  - M = Military
  - I = Industrial
  - C = Commercial
- PACKAGE:
  - C = Ceramic
- ACCESS TIME
- BITS PER WORD
- NUMBER OF WORDS
- STATIC RAM
- WHITE TECHNOLOGY

PACKAGE OUTLINE

FOR 25 AND 35 nS PARTS

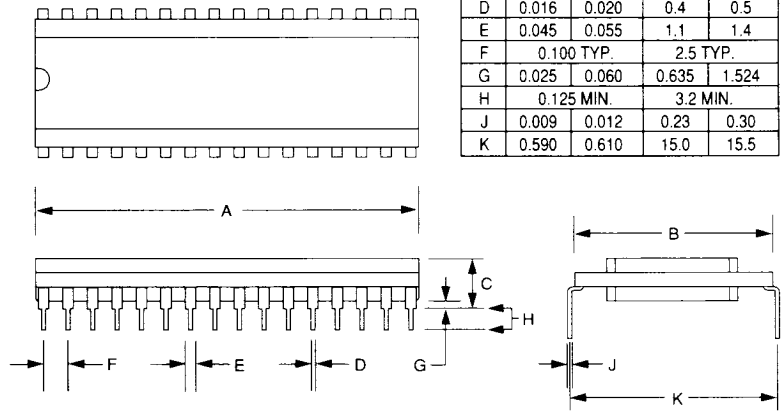
DIM.	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.654	1.686	42.0	42.8
B	0.580	0.600	14.7	15.2
C	0.235	0.275	6.0	7.0
D	0.016	0.020	0.4	0.5
E	0.045	0.055	1.1	1.4
F	0.100 TYP.		2.5 TYP.	
G	0.015	0.060	1.0	1.5
H	0.125 MIN.		3.2 MIN.	
J	0.008	0.012	0.2	0.30
K	0.590	0.610	15.0	15.5



PACKAGE OUTLINE

FOR 45–120 nS PARTS

DIM.	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.584	1.616	40.23	41.05
B	0.544	0.556	13.8	14.1
C	0.145	0.200	3.68	5.08
D	0.016	0.020	0.4	0.5
E	0.045	0.055	1.1	1.4
F	0.100 TYP.		2.5 TYP.	
G	0.025	0.060	0.635	1.524
H	0.125 MIN.		3.2 MIN.	
J	0.009	0.012	0.23	0.30
K	0.590	0.610	15.0	15.5



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All specifications are subject to change without notice.

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