PLESSEY Semiconductors

ADVANCED PRODUCT INFORMATION

ZN538/ZN539

T-51-07-01

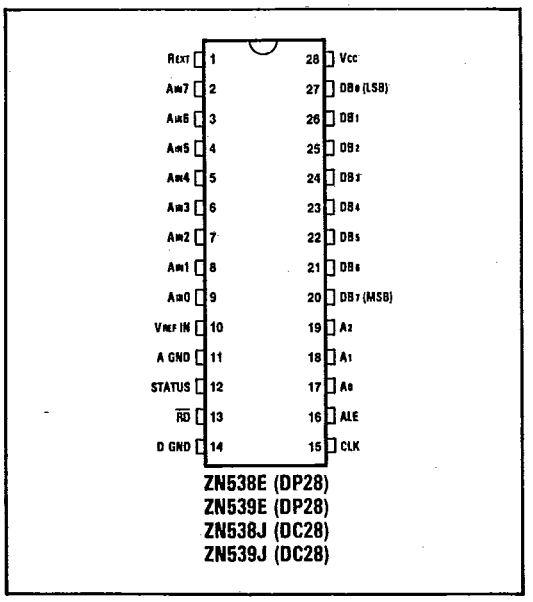
MICROPROCESSOR-COMPATIBLE 8-BIT, 8 CHANNEL DATA ACQUISITION SYSTEM

The ZN538 and ZN539 are 8-bit, 8-channel data acquisition systems designed to easily interface to most popular microprocessors. Each consists of an 8-bit successive approximation A-D converter, an 8 channel multiplexer, 8 x 8 bit RAM, clock prescaler, control logic and double buffered latches with 3-state outputs.

Using the successive approximation technique, the result of each channel conversion is loaded into the correct location of the 8 x 8 bit RAM. The address bus (A_2-A_0) is used to select the channel data to be read with the double buffered output latches allowing data to be read at any time irrespective of the conversion status.

FEATURES

- Choice of Linearity: ±0.5 LSB (ZN538) or ±1 LSB (ZN539)
- 16 microseconds Conversion Time
- 8 Analog Inputs
- On-Chip 8 x 8 RAM
- Continuous Conversion Operation
- Versatile Microprocessor Interfacing with Double Buffered Output Latch
- Microprocessor, TTL and CMOS Compatible
- Accepts Microprocessor Clocks up to 4MHz
- ROM Type Operation
- Commercial or Military Temperature Ranges



ZN538E (DP28)
ZN539E (DP28)
ZN538J (DC28)
ZN539J (DC28)

Pin connections - top view

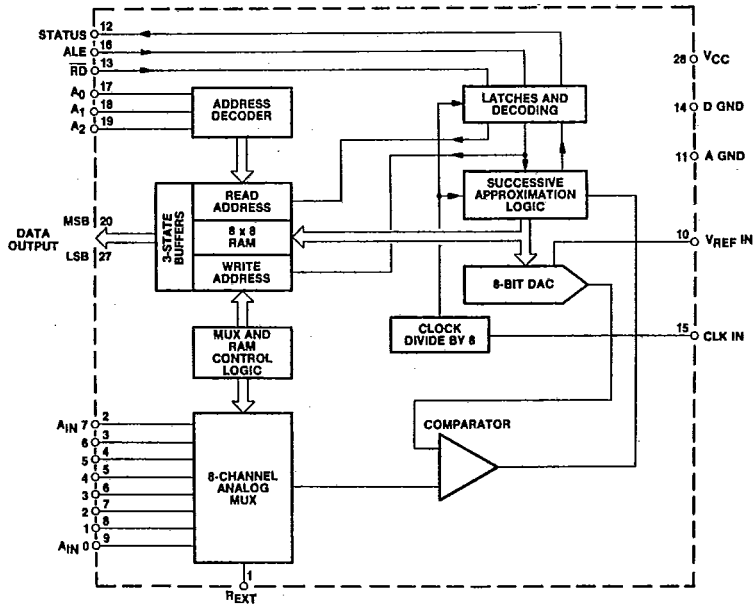


Fig.1 System diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{CC} = 5V, T_{amb} = +25°C, f_{CLK} = 500kHz

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Characteristic	Value					Units	Conditions
	T_{amb} = +25°C			Over specified temp. range			
	Min.	Typ.	Max.	Min.	Max.		
ZN538							
Linearity error	-	-	±0.5	-	±0.5	LSB	
Differential linearity error	-	-	±0.75	-	±0.75	LSB	
ZN539							
Linearity error	-	-	±1	-	±1	LSB	
Differential linearity error	-	-	±1	-	±1	LSB	
All types							
Zero transition	-	10	-	-	-	mV	Plastic DP28 } Ext. Ref.
(00000000 00000001)	-	10	-	-	-	mV	Ceramic DG28 } = 2.56V
Full-scale transition	-	2.550	-	-	-	V	Plastic DP28 }
(11111110 11111111)	-	2.550	-	-	-	V	Ceramic DG28 }
Linearity temperature coefficient		±3 typ.				ppm/°C	} Ext. Ref. = 2.50V
Differential linearity temperature coefficient		±6 typ.				ppm/°C	} Ext. Ref. = 2.50V
Gain temperature coefficient		±10 typ.				ppm/°C	} Ext. Ref. = 2.50V
Offset temperature coefficient		±7 typ.				ppm/°C	} Ext. Ref. = 2.50V
Resolution	8	-	-	-	-	Bits	
Conversion time	16	-	-	-	-	µs	per channel
Supply rejection	-	0.2	-	-	-	%/V	
Supply voltage	4.5	5.0	5.5	4.5	5.5	V	
Supply current	-	42	-	-	-	mA	} Outputs in high impedance state
Power consumption	-	210	-	-	-	mW	} Outputs in high impedance state
Reference input range	1.5	-	3.0	-	-	V	
Ladder output impedance	-	2.7	-	-	-	kΩ	
Multiplexed inputs							
Input current	-	10	-	-	-	nA	V_{IN} = +3V, R_{EXT} = 1.8kΩ
Input resistance	-	10	-	-	-	MΩ	
Tail current	-	1.1	-	-	-	mA	R_{EXT} = 1.8kΩ, V_{EE} = -5V
Negative supply	-3	-5	-30	-3	-30	V	
Input voltage, V_{IN}	-0.5	-	+3.5	-0.5	+3.5	V	
External voltage reference							
Output voltage	1.5	-	3.0	-	-	V	
Slope impedance	-	0.75	-	-	-	Ω	
ZN538 current drain from V_{REF} IN	-	-	1.0	-	-	mA	Note 1
Output voltage temperature coefficient	-	50	-	-	-	ppm/°C	
External clock							
Clock frequency	-	-	4.0	-	4.0	MHz	
High level input voltage V_{IH}	2.0	-	-	2.0	-	V	
Low level input voltage V_{IL}	-	-	0.8	-	0.8	V	
High level input current I_{IH}	-	200	-	-	-	µA	V_{CC} = 5.5V, V_{IN} = 4V
Low level input current I_{IL}	-	-160	-	-	-	µA	V_{CC} = 5.5V, V_{IN} = 0.8V

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Characteristic	Value					Units	Conditions
	T_{amb} = +25°C			Over specified temp. range			
	Min.	Typ.	Max.	Min.	Max.		
Logic ALE RD, A_2, A_1, A_0 inputs							
High level input voltage V_{IH}	2.0	-	-	2.0	-	V	
Low level input voltage V_{IL}	-	-	0.8	-	0.8	V	
High level input current I_{IH}	-	220	-	-	-	μA	V_{CC} = +5.5V V_{IN} = +5.5V
High level input current I_{IH}	-	35	-	-	-	μA	V_{CC} = +5.5V V_{IN} = +2.4V
Low level input current I_{IL}	-	-200	-	-	-	μA	V_{CC} = +5.5V V_{IN} = +0.4V
Data outputs							
High level output voltage V_{OH}	2.4	-	-	2.4	-	V	I_{OH} max.
Low level output voltage V_{OL}	-	-	0.4	-	0.4	V	I_{OL} max.
High level output current I_{OH}	-	-	-800	-	-	μA	
Low level output current I_{OL}	-	-	2.0	-	-	mA	
Enable/disable delay times							
TE1	90	-	220	-	-	ns	
TE0	60	-	120	-	-	ns	
TD1	80	-	160	-	-	ns	See Fig.9
TD0	60	-	110	-	-	ns	
ALE pulse width	150	-	-	-	-	ns	
Read pulse width	220	-	-	-	-	ns	
RD high to STATUS high	-	240	400	-	-	ns	
Address inputs stable prior to RD going low	10	-	-	-	-	ns	
Address inputs stable after RD going high	0	-	-	-	-	ns	

NOTES
1. When bipolar operation is employed, the external component connections will present an additional load to the reference. See section on bipolar operation.

ORDERING INFORMATION

Device type	Linearity error (LSB)	Operating temperature	Package
ZN538E	±0.5	0°C to +70°C	DP28
ZN538J	±0.5	-55°C to +125°C	DC28
ZN539E	±1.0	0°C to +70°C	DP28
ZN539J	±1.0	-55°C to +125°C	DC28

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	+7V
Max. voltage, logic and V_{REF} inputs	V_{CC}
Operating temperature range	0°C to 70°C (DP) -55°C to +125°C (DG)
Storage temperature range	-55°C to +125°C

GENERAL CIRCUIT DESCRIPTION

The ZN538/9 accepts eight analog inputs. Each input channel can be converted into an eight bit binary word using the successive approximation technique with the result of the conversion being loaded into the correct location of the 8 x 8 bit RAM. The STATUS output goes high to indicate the beginning of the conversion and the DAC input is set to the MSB. The multiplexer selects one input channel at a time on which a conversion is to be performed. The output of the DAC is compared to the unknown analog signal by means of the comparator. If the analog input is larger, the MSB is left in the circuit and if not the MSB is removed. On the second clock pulse this sequence is repeated for the next most significant bit and so on until all eight bits have been compared. On the 8th negative clock edge the STATUS goes low indicating that the conversion is complete and the RAM is updated.

The STATUS signal may be used to provide an interrupt signal when a particular channel receives updated data. To achieve this it is necessary to identify which channel is currently under conversion. The STATUS output provides an identifying signal by staying low for an additional 7 clock periods over normal 8 clock periods when channel 7 is active (see Fig.2).

Data can be read from the chip by placing the correct channel address on pins A_0, A_1 A_2. The Input address is latched when ALE goes low, when ALE goes high address input latch is transparent, and $\overline{RD}$ is taken low. The negative edge of the $\overline{RD}$ pulse powers up the required channel's RAM location and enables the 3-state outputs. The RAM is kept in a low power standby mode when not being accessed. Double buffered latches on-chip allow the outputs to be enabled at any time, irrespective of the conversion status and valid data will always be presented to the data bus, this data will be the result of the most recent conversion on that channel, therefore the $\overline{RD}$ signal can be completely asynchronous with respect to the STATUS.

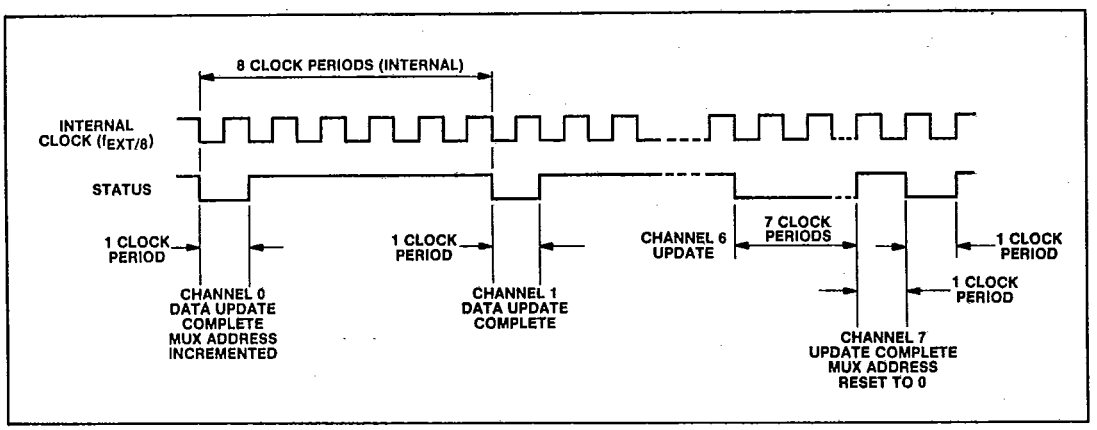

Fig.2 Status timing diagram

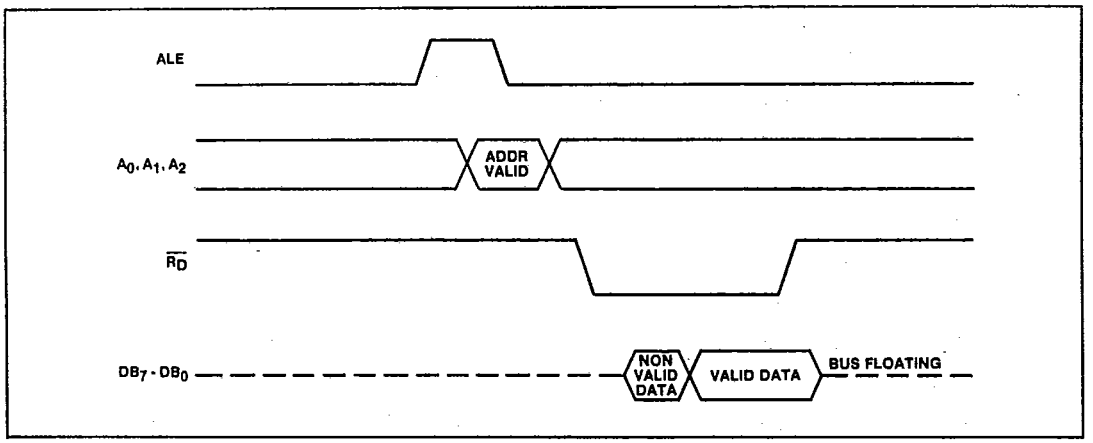

Fig.3 Read access timing diagram