HARRIS

HF-10

Universal Active Filter

Features

- Industry Standard Pinout
- Low Crosstalk .... -60dB
- Low Clock Feed Through 2mVrms
- Low Standby Current 500μA
- Clock to Center Frequency Ratio Accuracy $\pm$2%
- Filter Cutoff Frequency Stability Directly Dependent on External Clock Quality
- Separate High-pass (or Notch or All-Pass), Band-Pass, Low-pass Outputs
- f_O x Q Range up to 50kHz Minimum
- Operates to f_O = 20KHz Minimum
- Specifications Guaranteed for T_A from -55°C to +125°C

Applications

- General Purpose Audio-Band Filtering
- Real-Time Programming
  - ▸ Prototyping ▸ Dynamic Reconfiguration
- High Q Applications
- Precision Filtering at Low Q
- Precision Oscillators
- Extended Temperature
- Voice Response Systems
  - ▸ Modems ▸ Tone Generators
- Data Acquisition Systems
- Building Block for Precision Higher-Order Filters (Directly Cascadable)

Description

The HF-10 consists of two fully independent second order switched capacitor CMOS filter sections. Each second order section is a modified state-variable filter. In each section there are three operational amplifiers and an additional "summing node". The extra summing node is a direct benefit of the switched capacitor design approach. This provides increased versatility as compared to the classical continuous-time active filter. The transfer function of each section is tailored by the user's choice of feedback configuration, external resistor values, and external clock rate.

The HF-10 topology is very useful since it produces three different, but related, transfer functions simultaneously. Each transfer function has the same pole locations but different zero locations. One of the outputs is either a notch, all-pass, or high-pass signal, depending on the feedback configuration chosen by the user; the other outputs are band-pass and low-pass signals. The center frequency of the complex pole pair, f_O, is determined by the external clock frequency and the state of the "50/100/CL" input. This value can also be scaled by a function of the external resistor values depending on the feedback configuration. The other important filter characteristics, such as gain, Q, etc. are determined by functions of external resistor values. Any of the classical filter configurations (Butterworth, Bessel, Cauer/Elliptic, Chebyshev, etc.) can be realized.

The second order sections can be used separately with the constraint that the clock input for each section be driven by signals of the same level (i.e., either TTL or CMOS logic levels), and that the two clock signals share the same digital ground. If it is desired that a fourth order function be realized, the two sections can be cascaded. The "L Sh" (level shift) input is used in conjunction with the clock inputs to allow compatibility with either TTL or CMOS clock levels.

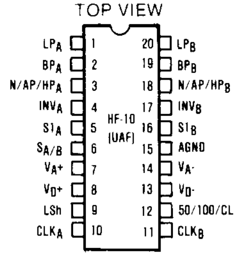
The HF-10 can be powered-down by connecting the "50/100/CL" input to V_D-. This disables the reference current generators for the operational amplifiers and the clock level shifters.

The HF-10 provides a number of advantages over other universal active filters: higher accuracy at frequency extremes; superior clock feedthrough supression; significantly lower crosstalk; better performance over -55°C to +125°C; drives smaller impedance to higher peak output voltage; and capable of precision oscillator applications (phase is continuous when frequency is changed).

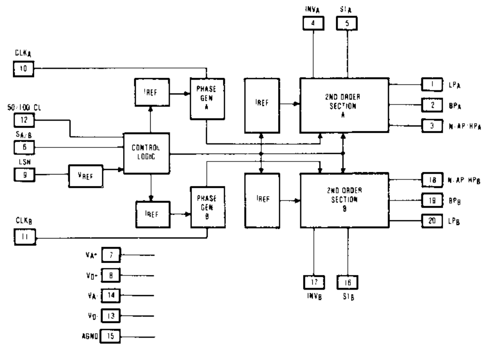
The device is available in a 20 pin ceramic package with temperature ranges of 0°C to +75°C and -55°C to +125°C. Application Note 578 is available.

Pinout

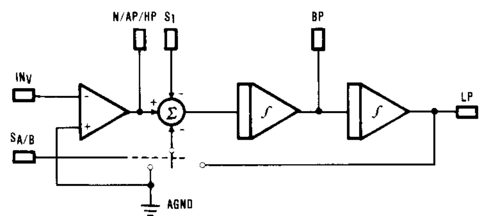
TOP VIEW



System Block Diagram



Filter Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Absolute Maximum Ratings

Supply Voltages .... ±6.5 Volts
Power Dissipation 300mW
Lead Temperature (Soldering, 10 Sec.) .... 300°C
Output Loading .... RLOAD > 3.5kΩ
CLOAD <100pF
Junction Temperature .... 175°C

Operating Temperature Ranges
HF-10-2, -8 .... -55°C to +125°C
HF-10-5, -7 .... 0°C to +75°C
HF-10-9 .... -40°C to +85°C
Storage Temperature .... -65°C to +150°C

Electrical Specifications (Complete Filter) $\pm 4.5V < V_S < \pm 5.5V$, (Note 1) Refer to Figure 1.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Range	f_O XQ < 50kHz	50		20K	Hz
Clock to Center Frequency Ratio					
$f_{CLK}/f_O = 50$	Pin 12 = V_D+, Q = 10 f_O XQ < 50kHz			±2%	
$f_{CLK}/f_O = 100$	Pin 12 = AGND, Q = 10 f_O XQ < 50kHz			±2%	
Q Range	f_O XQ < 50kHz	0.5		100	
Q Accuracy (Q Deviation from an Ideal Continuous Filter)					
$f_{CLK}/f_O = 50$	Pin 12 = V_D+, Q ≤ 20 f_O XQ < 50kHz			±4%	
$f_{CLK}/f_O = 100$	Pin 12 = AGND, Q ≤ 20 f_O XQ < 50kHz			±3%	
f_O XQ Product		50K			Hz
f_O Temperature Coefficient					
$f_{CLK}/f_O = 50$	T_A = 25°C Pin 12 = V_D+, f_O XQ < 50kHz External Clock Temperature Independent			±100	ppm/°C
$f_{CLK}/f_O = 100$	Pin 12 = AGND, f_O XQ < 50kHz External Clock Temperature Independent			±100	ppm/°C
Q Temperature Coefficient	T_A = 25°C f_O XQ < 50kz, Q Setting Resistors Temperature Independent			±500	ppm/°C
Crosstalk	INV_A = 0dBm @ 1kHz INV_B = 0V		-60		dB
Clock Feedthrough	See Figure 2		2	5	mVrms
Clock Frequency	Min @ f_{CLK}/f_O = 50, Max @ f_{CLK}/f_O = 100	2.5		2048	kHz
Power Supply Current	T_A = 25°C		13		mA
Standby Current	Pin 12 = V_A-		500		μA

Electrical Specifications (Internal Operational Amplifiers) $\pm 4.5V < V_S < \pm 5.5V$, (Note 1) Refer to Figure 1

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Voltage Swing (Pins 1, 2, 3, 18, 19, 20)	R_{LOAD} = 3.5KΩ	±3.5			V
Op Amp Gain-BW Product		2.5	3.8		MHz
Op Amp Slew Rate		5	15		V/μs
Power Supply Rejection Ratio (PSRR)	DC Only	40			dB

NOTE 1. Unless Otherwise Specified, typical parameters are at +25°C, min-max parameters are over operating temperature range.

Die Characteristics

Transistor Count 464
Die Dimensions .... 88 x 127
Substrate Potential .... +V
Process .... SAJI CMOS

Thermal Constants (°C)	θ_{ja}	θ_{jc}
Ceramic DIP	81	24
Ceramic LCC	76	19

Pin Assignments

SYMBOL	DESCRIPTION
LP, BP, N/AP/HP (A or B)	Low-pass, band-pass, notch or all-pass or high-pass outputs of each second order section.
INV (A or B)	Inverting input of the summing op amp of each filter.
S1 (A or B)	Inverting summing input pin used in most filter configurations.
$S_{A/B}$	Activates a switch connecting one of the inputs of the filter's second summer to either analog ground ($S_{A/B}$ low to V_A-) or to the low-pass output of the circuit ($S_{A/B}$ high to V_A+). This allows flexibility in the various modes of operation of the I. C.
V_A+, V_D+*	Analog positive supply and digital positive supply. These pins are internally connected through the I.C. substrate and therefore, V_A+ and V_D+ should be derived from the same power supply source. They have been brought out separately so they can be bypassed by separate capacitors, if desired. They can be externally tied together and bypassed by a single capacitor.
V_A-, V_D-*	Analog and digital negative supply, respectively. The same comments as for V_A+, V_D+ apply here, except V_A- and V_D- are not tied together internally.
L Sh	Level shift pin. Accommodates various clock levels with dual or single supply operation. With dual ±5V supplies, the HF-10 can be driven with CMOS clock levels (±5V), and the "L Sh" pin should be tied either to the system ground or to the negative supply pin. If the same supplies as above are used and TTL clock levels, derived from a 0V to 5V supply, are used, the "L Sh" pin should be tied to the system ground. For single supply operation (0V and 10V), the V_D- and V_A- pins should be connected to the system ground, the AGND pin should be biased at 5V, and the "L Sh" pin should also be tied to the system ground. This will accommodate both CMOS and TTL clock levels.
CLK (A or B)	Clock inputs for each switched capacitor filter building block. Should both be of the same level (TTL or CMOS). The level shift (L Sh) pin description discusses how to accommodate their levels. The duty cycle of the clock should preferably be close to 50%, especially when clock frequencies above 200kHz are used. This allows the maximum time for the op amps to settle, yielding optimum filter operation.
50/100/CL	By tying this pin to V_D+, a 50:1 clock to filter center frequency operation is obtained. Tying at mid-supplies (i.e., analog ground with dual supplies) allows the filter to operate at a 100:1 clock to center frequency ratio. When tied to VD-, a simple current limiting circuit is triggered to limit the overall supply current. The filtering action is then aborted. This pin also acts as a power up reset when pulled to V_D- after power is applied.
AGND	Analog ground pin. Should be connected to the system ground for dual supply operation or biased at mid-supply for single supply operation. The Non-inverting inputs of the filter op amps are connected to the AGND pin so a "clean" ground is mandatory.

NOTE: All pins are protected against static discharge.

*To initiate the internal power-on reset feature of the HF-10, V+ and V- should be brought up at the same time, or V- should be brought up first. An alternative to power supply sequencing is to strobe Pin 12 (50/100/CL) to V- after power is applied, regardless of power supply sequencing. This will also initiate the power-on reset feature of the HF-10.

Typical Filter Configuration

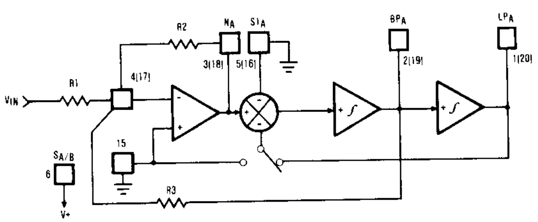


FIGURE 1.

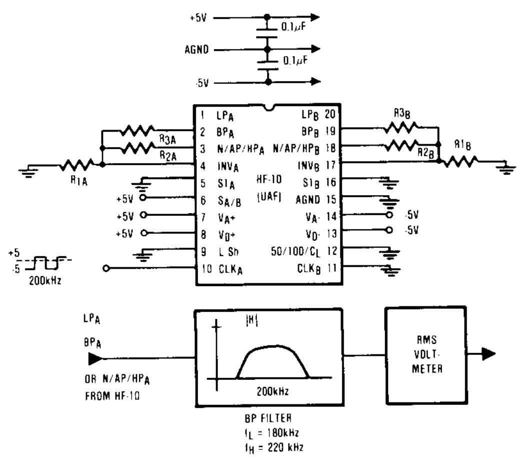
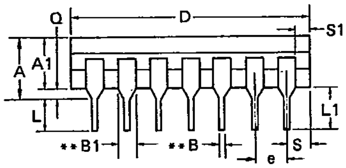


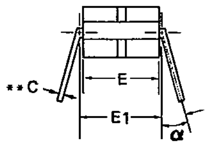
FIGURE 2. MEASURING CHANNEL A CLOCK FEEDTHROUGH

Package Configuration

T-90-20

A B C D E .300 CERAMIC DUAL-IN-LINE





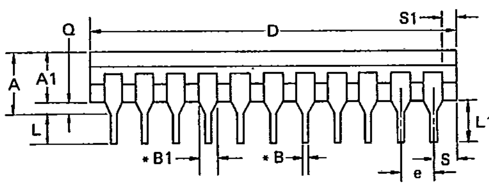
PKG. CODE	LEAD COUNT	DIM. A	DIM. A1	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. L1	DIM. S	DIM. S1	DIM. Q	DIM. α
A	8 / SSI	— / .200	.140 / .160	.016 / .023	.050 / .065	.008 / .015	.375 / .395	.245 / .265	.290 / .310	.100 / BSC	.125 / .150	.150 / —	— / .055	.005 / —	.015 / .060	0° / 15°
B1	14 / MSI	— / .200	.140 / .170	.016 / .023	.050 / .065	.008 / .015	.753 / .785	.265 / .285	.290 / .310	.100 / BSC	.125 / .180	.150 / —	— / .098	.005 / —	.015 / .060	0° / 15°
B2	14 / LSI	— / .200	.140 / .170	.016 / .023	.050 / .065	.008 / .015	.753 / .785	.285 / .305	.300 / .320	.100 / BSC	.125 / .180	.150 / —	— / .098	.005 / —	.015 / .060	0° / 15°
C1	16* / MSI	— / .200	.140 / .170	.016 / .023	.050* / .065*	.008 / .015	.753 / .785	.265 / .285	.290 / .310	.100 / BSC	.125 / .180	.150 / —	— / .080	.005 / —	.015 / .060	0° / 15°
C2	16* / LSI	— / .200	.140 / .170	.016 / .023	.050* / .065*	.008 / .015	.753 / .785	.285 / .305	.300 / .320	.100 / BSC	.125 / .180	.150 / —	— / .080	.005 / —	.015 / .060	0° / 15°
D	18 / LSI	— / .200	.140 / .170	.016 / .023	.050* / .065*	.008 / .015	.882 / .915	.285 / .305	.300 / .320	.100 / BSC	.125 / .180	.150 / —	— / .098	.005 / —	.015 / .060	0° / 15°
E	20 / LSI	— / .200	.140 / .170	.016 / .023	.050* / .065*	.008 / .015	.940 / .970	.285 / .305	.300 / .320	.100 / BSC	.125 / .180	.150 / —	— / .080	.005 / —	.015 / .060	0° / 15°

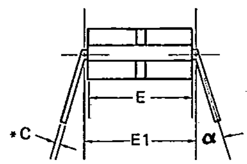
* End leads are half leads where B remains the same and B1 is $\frac{0.035}{0.045}$

** Solder dip finish add +0.003 inches

F .400 CERAMIC DUAL-IN-LINE

G H .600 CERAMIC DUAL-IN-LINE





PKG. CODE	LEAD COUNT	DIM. A	DIM. A1	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. L1	DIM. S	DIM. S1	DIM. Q	DIM. α
F .400	22 / LSI	— / .225	.150 / .180	.016 / .023	.050 / .065	.008 / .015	1.055 / 1.085	.375 / .395	.395 / .415	.100 / BSC	.125 / .180	.150 / —	— / .080	.005 / —	.015 / .060	0° / 15°
G .600	24 / LSI	— / .225	.150 / .180	.016 / .023	.050 / .065	.008 / .015	1.24 / 1.27	.515 / .535	.595 / .615	.100 / BSC	.125 / .180	.150 / —	— / .098	.005 / —	.015 / .060	0° / 15°
H .600	28 / LSI	— / .225	.160 / .190	.016 / .023	.050 / .065	.008 / .015	1.44 / 1.47	.515 / .535	.595 / .615	.100 / BSC	.125 / .180	.150 / —	— / .098	.005 / —	.015 / .060	0° / 15°

* Solder dip finish add +0.003 inches.

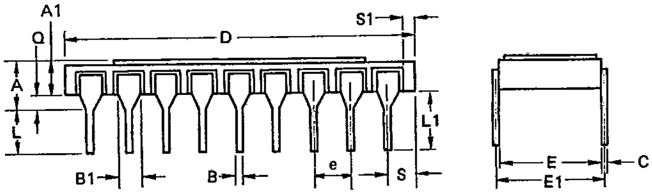
NOTE: Dimensions are $\frac{\text{Min}}{\text{Max}}$. Dimensions are in inches.

BSC means basic spacing between centerlines.

Package Configuration

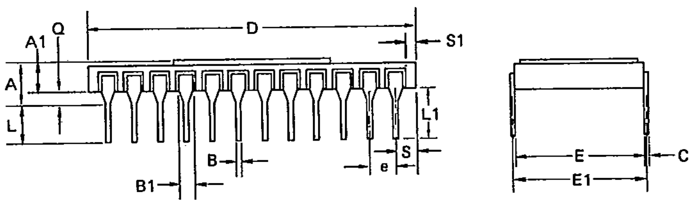
T-90-20

I .300 SIDEBRAZE DUAL-IN-LINE



PKG. CODE	LEAD COUNT	DIM. A	DIM. A1	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. L1	DIM. S	DIM. S1	DIM. Q
I	18	— / .200	.080 / .110	.016 / .023	.045 / .060	.008 / .015	.890 / .910	.280 / .300	.290 / .310	.100 / BSC	.125 / .180	.150 / —	— / .098	.005 / —	.025 / .045

J K L .600 SIDEBRAZE DUAL-IN-LINE



PKG. CODE	LEAD COUNT	DIM. A	DIM. A1	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. L1	DIM. S	DIM. S1	DIM. Q
J	24	— / .225	.080 / .110	.016 / .023	.040 / .054	.008 / .015	1.185 / 1.215	.587 / .603	.598 / .612	.100 / BSC	.125 / .180	.150 / —	— / .080	.005 / —	.040 / .060
K	28	— / .225	.080 / .110	.016 / .023	.040 / .054	.008 / .015	1.385 / 1.415	.587 / .603	.598 / .612	.100 / BSC	.125 / .180	.150 / —	— / .080	.005 / —	.030 / .060
L	40	— / .225	.080 / .110	.016 / .023	.040 / .054	.008 / .015	1.980 / 2.020	.587 / .603	.598 / .612	.100 / BSC	.125 / .180	.150 / —	— / .080	.005 / —	.040 / .060

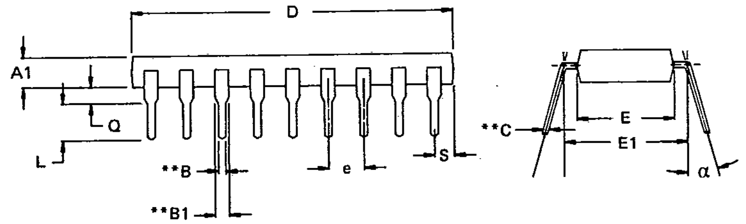
NOTE: Dimensions are $\frac{\text{Min}}{\text{Max}}$. Dimensions are in inches.

BSC means basic spacing between centerlines.

11 PACKAGING

Package Configuration

M N O P Q .300 PLASTIC DUAL-IN-LINE

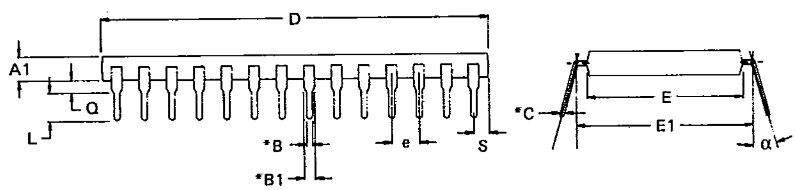


PKG. CODE	LEAD COUNT	DIM. A1	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. S	DIM. Q	DIM. α
M	8	.125/.140	.016/.023	.050/.070	.008/.015	.370/.390	.245/.265	.290/.310	.090/.110	.110/.150	.030/.050	.020/.040	0°/15°
N	14	.125/.140	.016/.023	.050/.070	.008/.015	.750/.770	.245/.265	.290/.310	.090/.110	.110/.150	.030/.050	.020/.040	0°/15°
O	16*	.125/.140	.016/.023	.050/.070	.008/.015	.750/.770	.245/.265	.290/.310	.090/.110	.110/.150	.025/.035	.020/.040	0°/15°
P	18	.125/.140	.016/.023	.050/.070	.008/.015	.900/.920	.245/.265	.290/.310	.090/.110	.110/.150	.040/.060	.020/.040	0°/15°
Q	20	.130/.145	.016/.023	.050/.070	.008/.015	1.030/1.050	.250/.270	.290/.310	.090/.110	.110/.150	.060/.080	.020/.040	0°/15°

* End leads are half leads where B remains the same and B1 is $\frac{0.035}{0.045}$

** Solder dip finish add 0.003 inches.

R S .600 PLASTIC DUAL-IN-LINE



PKG. CODE	LEAD COUNT	DIM. A1	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. S	DIM. Q	DIM. α
R	24	.145/.155	.016/.023	.050/.070	.008/.015	1.24/1.26	.540/.560	.590/.610	.090/.110	.110/.150	.045/.095	.020/.040	0°/15°
S	28	.145/.155	.016/.023	.050/.070	.008/.015	1.54/1.57	.540/.560	.590/.610	.090/.110	.110/.150	.110/.160	.020/.040	0°/15°

* Solder dip finish add 0.003 inches.

NOTE: Dimensions are $\frac{\text{Min}}{\text{Max}}$. Dimensions are in inches.

BSC means basic spacing between centerlines.

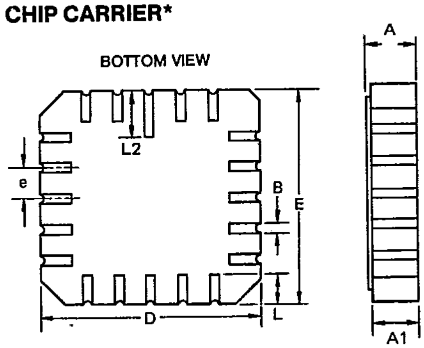
Package Configuration

T-90-20

T .350 CERAMIC LEADLESS CHIP CARRIER*

U .450 CERAMIC LEADLESS CHIP CARRIER*

V .650 CERAMIC LEADLESS CHIP CARRIER*

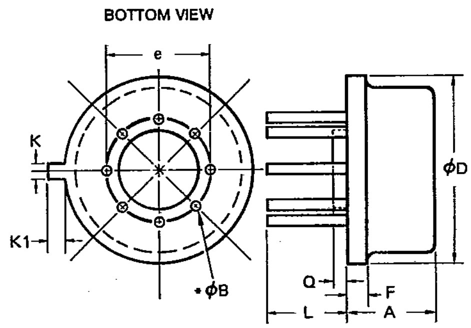


PKG. CODE	LEAD COUNT	DIM. A	DIM. A1	DIM. B	DIM. D	DIM. E	DIM. e	DIM. L	DIM. L2
T	20 / .350 SQ	.073 / .089	.063 / .077	.022 / .028	.342 / .358	.342 / .358	.050 / BSC	.045 / .055	.075 / .095
U	28 / .450 SQ	.074 / .088	.064 / .076	.022 / .028	.442 / .458	.442 / .458	.050 / BSC	.045 / .055	.075 / .095
V	44 / .650 SQ	.073 / .089	.063 / .077	.022 / .028	.643 / .662	.643 / .662	.050 / BSC	.045 / .055	.075 / .095

* Solder dip finish for military parts conform to MIL-M-38510, Type A.

W TO-99 METAL CAN

X TO-100 METAL CAN



PKG. CODE	LEAD COUNT	DIM. A	DIM. ϕB	DIM. ϕD	DIM. e	DIM. F	DIM. K	DIM. K1	DIM. L	DIM. Q
W	8 TO-99	.165 / .185	.016 / .018	.345 / .365	.190 / .210	.020 / .040	.028 / .034	.028 / .040	.505 / .550	.015 / .040
X	10 TO-100	.165 / .185	.016 / .018	.345 / .365	.220 / .240	.020 / .040	.028 / .034	.028 / .040	.505 / .550	.015 / .040

* Solder dip finish add +0.003 inches.

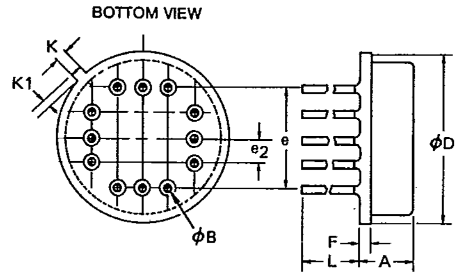
NOTE: Dimensions are $\frac{\text{Min}}{\text{Max}}$. Dimensions are in inches.

BSC means basic spacing between centerlines.

11 PACKAGING

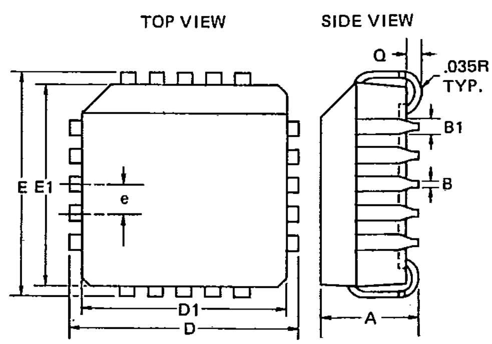
Package Configuration

Y TO-8 METAL CAN



PKG. CODE	LEAD COUNT	DIM. A	DIM. ϕB	DIM. ϕD	DIM. e	DIM. e2	DIM. F	DIM. K	DIM. K1	DIM. L
Y	12 TO-8	.130/.150	.016/.021	.585/.615	.400/BSC	.100/BSC	.020/.040	.027/.034	.027/.045	.500/.550

AA AB AC PLASTIC LEADED CHIP CARRIER



PKG. CODE	LEAD COUNT	DIM. A	DIM. B	DIM. B1	DIM. D/E	DIM. D1/E1	DIM. e	DIM. Q
AA	20	.165/.180	.013/.021	.026/.032	.385/.395	.350/.356	.050/BSC	.020/—
AB	28	.165/.180	.013/.021	.026/.032	.485/.495	.450/.456	.050/BSC	.020/—
AC	44	.165/.180	.013/.021	.026/.032	.685/.695	.650/.656	.050/BSC	.020/—

NOTE: Dimensions are Min/Max. Dimensions are in inches.

BSC means basic spacing between centerlines.