High-Speed CMOS 8K x 36 Block-Allocated Shared-Port RAM with Flexi-Burst™

QS75836

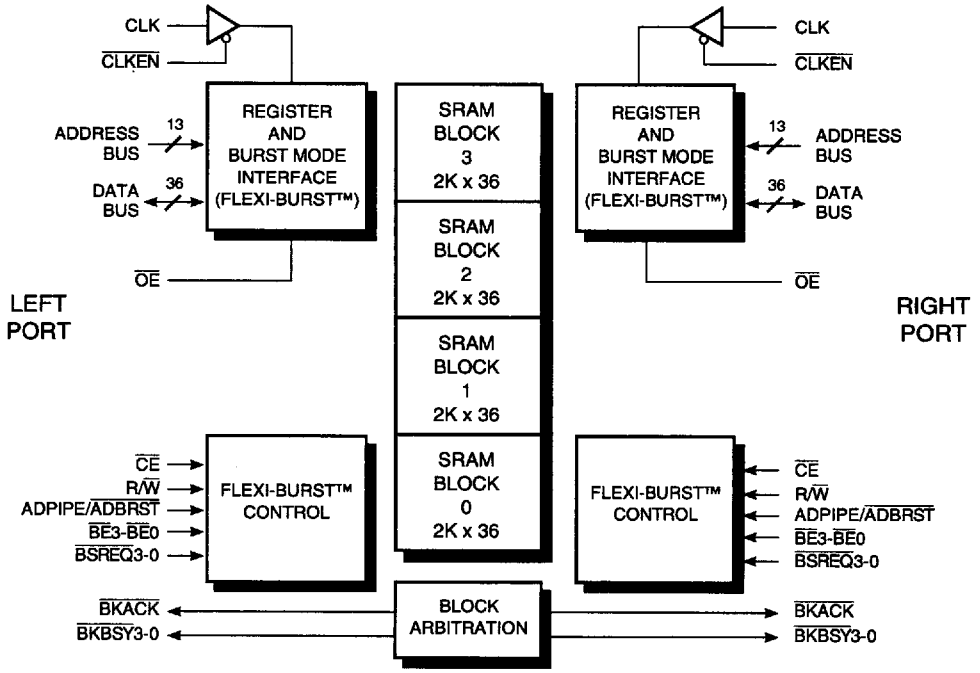
FEATURES

- Four independent 2K x 36-bit blocks
- Independent port controls
- Fast port access times: 20 ns, 25 ns, 30 ns - 50-MHz, 40-MHz, 33-MHz cycle times
- Total bandwidth 3.6 Gbits/sec
- Simultaneous access for different block operations
- Clocked/pipelined and Flexi-Burst™
- Built-in busy arbitration logic for each block
- Low-power QCMOS™ technology
- Separate byte enables for accessing 9-, 18-, 27-, 36-bit words
- Available in 208-pin QFP

DESCRIPTION

This device consists of four blocks of 2K x 36 bits SRAM which can be accessed from either port using the independent port control pins. Each port has a clocked interface in which addresses, data and control are loaded on the rising edge of the relevant clock. The data can be pipelined or burst depending upon the state of the control pins. This can allow for very fast block transfers of 3.6 Gbits/sec in burst mode with both ports active. Arbitration is done on a block basis with a $\overline{BKBSY}$ (Block Busy) flag. This will lock out the losing port and allow access to the winning port to write or read to that block. If non-coincidental blocks are addressed, then both ports can access their respective blocks. Applications for this part are datacomms, ATM, networking, multimedia and graphics.

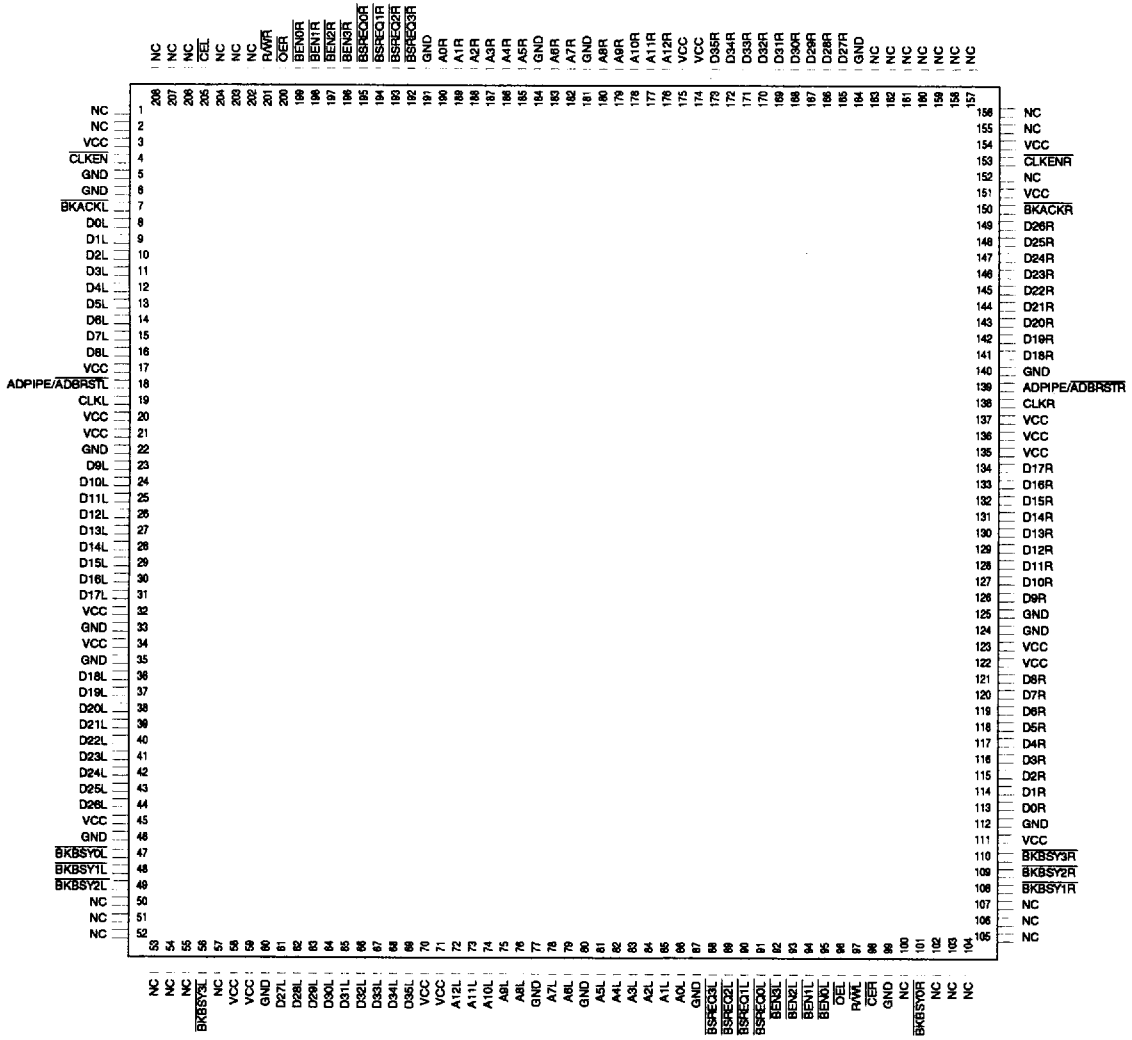
FIGURE 1. FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The QS75836 consists of four blocks of 2K x 36-bit wide SRAM. Each SRAM block is 2K x 36 bits wide and has a synchronous interface with a separate clock input that accepts all control, data and address information on its clock's rising edge, providing $\overline{\text{CLKEN}}$ is LOW. The data bus is 36 bits wide and the address bus is 13 bits wide. The address input register is a loadable counter that can be selected to burst data in or out, depending on the state of ADPIPE/$\overline{\text{ADBRST}}$. The length of burst can be selected by the $\overline{\text{BSREQ}}$ pins and is selectable from two words to the total block size of 2K. The block counter is a full wraparound counter. When the block has finished writing or reading, $\overline{\text{BKACK}}$ asserts, indicating end of block. Non-simultaneous block accesses can be accomplished at full bandwidth; however, if the same block needs to be accessed, then it is arbitrated on a first-come first-served basis using the busy arbitration logic flags (one per block).

FIGURE 2. 208-PIN QFP PINOUT



PIN DESCRIPTIONS

Pin Name Left Port	Pin Name Right Port	Status	Pins/Port	Pin Description
ADD_L	ADD_R	I	13	Address Bus
$DATA_L$	$DATA_R$	I/O	36	Data Bus
$\overline{CE}_L$	$\overline{CE}_R$	I	1	Chip Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	I	1	Read/Write
CLK_L	CLK_R	I	1	Clock
$\overline{CLKEN}_L$	$\overline{CLKEN}_R$	I	1	Clock Enable
$\overline{OE}_L$	$\overline{OE}_R$	I	1	Output Enable
$ADPIPE/\overline{ADBRST}_L$	$ADPIPE/\overline{ADBRST}_R$	I	1	Address Pipelined/Burst Mode Select
$\overline{BE3}$-$\overline{BE0}_L$	$\overline{BE3}$-$\overline{BE0}_R$	I	4	Byte Enable
$\overline{BSREQ}_L$3-0	$\overline{BSREQ}_R$3-0	I	4	Burst Block Size Request
$\overline{BKBSY}_L$3-0	$\overline{BKBSY}_R$3-0	O	4	Block Busy Flag
$\overline{BKACK}_L$	$\overline{BKACK}_R$	O	1	Burst Block Complete Acknowledge

ADDRESS (13-Bit Address Bus, Left and Right Port)
The independent port address bus allows the SRAM blocks to be accessed on the rising edge of the relevant port clock.

DATA (36-Bit Bi-directional Data Ports, Left and Right)
This is a 36-bit wide data bus. The left port data bus is designated $DATA_L$; similarly, the right port is designated $DATA_R$. The data is sampled on the rising edge of the relevant port clock. When $\overline{BSREQ}$3-0 is set to "1111," then the data bus D10-D0 can be used to program the block burst size to any value.

CLK (Clock)
Each port has its own free-running clock. If both port addresses are simultaneously clocked and are of the same value, the $\overline{BKBSY}$ output will be asserted synchronously to the winning port clock.

$\overline{CLKEN}$ (Clock Enable)
Each port has its own clock enable. When asserted, allows the port to be clocked; when de-asserted, no operation is performed.

ADPIPE/$\overline{ADBRST}$ (Address Pipelined/Address Burst Mode Select)
When asserted HIGH with a valid address synchronous with the rising edge of the relevant port clock, the address is clocked in to the relevant SRAM block.

When asserted LOW with a valid address synchronous with the rising edge of the relevant port clock, along with the $\overline{BSREQ}$ value, the data can be burst on every rising edge of the associated port clock. The internal burst counter alleviates the need to provide external subsequent addresses. This counter is a full wraparound counter.

$\overline{BSREQ}$ (Burst Size Request)
This is a 4-bit signal which when asserted in the address phase along with ADPIPE/$\overline{ADBRST}$ sets the value of the burst block size, be it a read or write transaction; (see BURST BLOCK SIZE TRUTH TABLE). When set all to "1," then the value on the data bus preloads the burst size to the binary value.

BURST BLOCK SIZE TRUTH TABLE

$\overline{BSREQ3}$	$\overline{BSREQ2}$	$\overline{BSREQ1}$	$\overline{BSREQ0}$	Burst Block Size x 36-Bit Words
0	0	0	0	2
0	0	0	1	4
0	0	1	0	8
0	0	1	1	16
0	1	0	0	32
0	1	0	1	64
0	1	1	0	128
0	1	1	1	256
1	0	0	0	512
1	0	0	1	1024
1	0	1	0	2048
1	1	1	1	Value placed on the Data Bus D10-D0

EXAMPLE OF FLEXI-BURST

$\overline{BSREQ3}$	$\overline{BSREQ2}$	$\overline{BSREQ1}$	$\overline{BSREQ0}$	Burst Block Size x 36-Bit Words	Data Bus D10-D0
1	1	1	1	48 words	000 0011 0000
1	1	1	1	53 words	000 0011 0101
1	1	1	1	106 words	000 0110 1010

$\overline{OE}$ (Output Enables)
There are two output enables $\overline{OE}_L$ and $\overline{OE}_R$ that are asynchronous active LOW inputs. When asserted LOW, the output buffers place data on the respective data bus.

$\overline{BKACK}$ (Block Acknowledge)
This asserts in burst mode only and indicates when the end of block has been reached.

$\overline{BKBSY}$ (Block Busy)
Whenever any port wins access to an SRAM block, a $\overline{BKBSY}$ signal is asserted to prevent the losing port from accessing the same SRAM block. Each SRAM block has a pair of busy flags, one for each port. This signal is cleared when the winning port relinquishes control of that block by changing the address to a different block or by the use of $\overline{CE}$. This signal is synchronous to the winning port clock.

$\overline{CE}$ (Chip Enable)
Each port has an active LOW synchronous chip enable. This input, when asserted synchronously with the respective port clock, allows access to the RAM array blocks. The busy arbitration is reset when $\overline{CE}$ is clocked HIGH, allowing access to all the blocks.

R/$\overline{W}$ (Read/Write)
Each port has its own synchronous read/write input. Read operations are performed when this signal is HIGH at the rising edge of its respective port clock. Write operations are performed when the signal is sampled in the LOW state.

$\overline{BE}$ (Byte Enables 0..3)
There are four byte enables for each port. All signals are synchronous to its respective port clock. These signals allow byte, half-word, tri-byte and word transfers to and from the SRAM blocks. This method allows for efficient connecting of differing bus sizes of 9, 18, 27, 36 bits.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground	–0.5 to 7.0V
DC Output Voltage V_{OUT}	–0.5 to Vcc +0.5V
DC Input Voltage V_{IN}	–0.5 to Vcc +0.5V
AC Input Voltage (Pulse Width ≤ 10ns)	–1.5V
DC Input Diode Current with V_{IN} < 0	–20 mA
DC Output Diode Current with V_{OUT} < 0	–50 mA
DC Output Current with V_{OUT} > Vcc	50 mA
DC Output Current Max Sink Current/Pin	70 mA
T_{STG} StorageTemperature	–55°C to +125°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device, resulting in functional- or reliability-type failures.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE
Commercial: T_A = 0°C to 70°C, Vcc = 5.0V ± 10%

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{IH}	Input HIGH Voltage	Logic HIGH for all Inputs	2.0	–	V
V_{IL}	Input LOW Voltage	Logic LOW for all Inputs	–	0.8	V
V_{OH}	Output HIGH Voltage	I_{OH} = –4 mA, Vcc = Min.	2.4	–	V
V_{OL}	Output LOW Voltage	I_{OL} = 4 mA, Vcc = Min.	–	0.4	V
$\lvert I_{IL} \rvert$	Input Leakage	Vcc = Max., V_{IN} = GND or Vcc	–	100	µA

Notes:
1. Transient inputs with V_{IL} not more negative than –1.5V are permitted for pulse widths < 10 ns.
2. Input leakage also includes I/Os.

CAPACITANCE
T_A = 25°C, f = 1.0 MHz QFP (QF) package

Name	Description	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	10	15	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	10	15	pF

Note: Capacitance is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

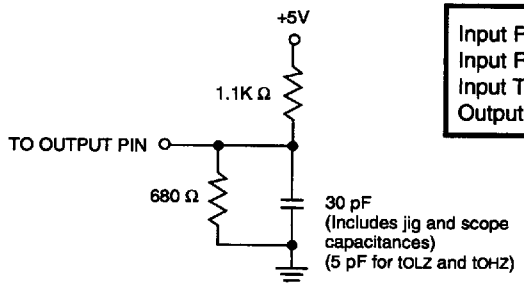
Symbol	Parameter	Cycle Time, ns (MHz)						Units
		-20 (50)		-25 (40)		-30 (33)		
		Typ	Max	Typ	Max	Typ	Max	
I_{CC1}	Operating Current Vcc = Max, Outputs Open f = f_{MAX}	400	450	320	350	264	288	mA

AC CHARACTERISTICS -20 ns (50 MHZ)

Symbol	Parameter	Min	Max	Units
t_{CLKL}	Clock Low Time	8		ns
t_{CLKH}	Clock High Time	8		ns
t_{CYC}	Cycle Time	20		ns
t_{OLZ}	Output Enable to LOW-Z[1]		14	ns
t_{OHZ}	Output Enable to HIGH-Z[1]		14	ns
t_{OE}	Output Enable Time		14	ns
t_{DS}	Data Setup Time	5		ns
t_{DH}	Data Hold Time	2		ns
t_{CDO}	Clock High to Output Valid	4	15	ns
t_{AS}	Address Setup Time	5		ns
t_{AH}	Address Hold Time	2		ns
t_{RWS}	Read/Write Setup Time	5		ns
t_{RWH}	Read/Write Hold Time	2		ns
t_{CKS}	Clock Enable Setup Time	5		ns
t_{CKH}	Clock Enable Hold Time	2		ns
t_{BES}	Byte Enable Setup Time	5		ns
t_{BEH}	Byte Enable Hold Time	2		ns
t_{PBS}	Pipeline/Burst Setup Time	5		ns
t_{PHB}	Pipeline/Burst Hold Time	2		ns
t_{BSY}	Clock to Busy	10	17	ns
t_{CES}	Chip Enable Setup Time	5		ns
t_{CEH}	Chip Enable Hold Time	2		ns

Note:
1. Guaranteed but not tested.

FIGURE 3. AC TEST CONDITIONS



Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	≤ 3 ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V

AC CHARACTERISTICS -25 ns (40 MHZ)

Symbol	Parameter	Min	Max	Units
t_{CLKL}	Clock Low Time	12		ns
t_{CLKH}	Clock High Time	12		ns
t_{CYC}	Cycle Time	25		ns
t_{OLZ}	Output Enable to LOW-Z[1]		16	ns
t_{OHZ}	Output Enable to HIGH-Z[1]		16	ns
t_{OE}	Output Enable Time		16	ns
t_{DS}	Data Setup Time	8		ns
t_{DH}	Data Hold Time	2		ns
t_{CDO}	Clock High to Output Valid	4	17	ns
t_{AS}	Address Setup Time	8		ns
t_{AH}	Address Hold Time	2		ns
t_{RWS}	Read/Write Setup Time	8		ns
t_{RWH}	Read/Write Hold Time	2		ns
t_{CKS}	Clock Enable Setup Time	8		ns
t_{CKH}	Clock Enable Hold Time	2		ns
t_{BES}	Byte Enable Setup Time	8		ns
t_{BEH}	Byte Enable Hold Time	2		ns
t_{PBS}	Pipeline/Burst Setup Time	8		ns
t_{PHB}	Pipeline/Burst Hold Time	2		ns
t_{BSY}	Clock to Busy	9	18	ns
t_{CES}	Chip Enable Setup Time	8		ns
t_{CEH}	Chip Enable Hold Time	2		ns

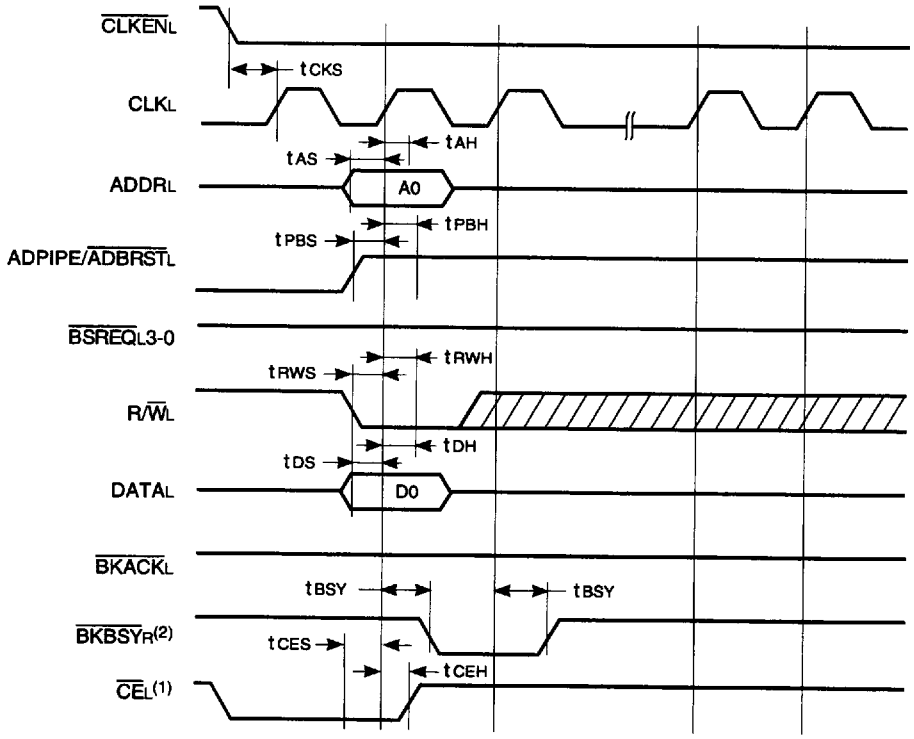
AC CHARACTERISTICS -30 ns (33 MHZ)

Symbol	Parameter	Min	Max	Units
t_{CLKL}	Clock Low Time	15		ns
t_{CLKH}	Clock High Time	15		ns
t_{CYC}	Cycle Time	30		ns
t_{OLZ}	Output Enable to LOW-Z[1]		17	ns
t_{OHZ}	Output Enable to HIGH-Z[1]		17	ns
t_{OE}	Output Enable Time		17	ns
t_{DS}	Data Setup Time	9		ns
t_{DH}	Data Hold Time	1		ns
t_{CDO}	Clock High to Output Valid	4	20	ns
t_{AS}	Address Setup Time	9		ns
t_{AH}	Address Hold Time	1		ns
t_{RWS}	Read/Write Setup Time	9		ns
t_{RWH}	Read/Write Hold Time	1		ns
t_{CKS}	Clock Enable Setup Time	9		ns
t_{CKH}	Clock Enable Hold Time	1		ns
t_{BES}	Byte Enable Setup Time	9		ns
t_{BEH}	Byte Enable Hold Time	1		ns
t_{PBS}	Pipeline/Burst Setup Time	9		ns
t_{PHB}	Pipeline/Burst Hold Time	1		ns
t_{BSY}	Clock to Busy	10	19	ns
t_{CES}	Chip Enable Setup Time	9		ns
t_{CEH}	Chip Enable Hold Time	1		ns

Note:
1. Guaranteed but not tested.

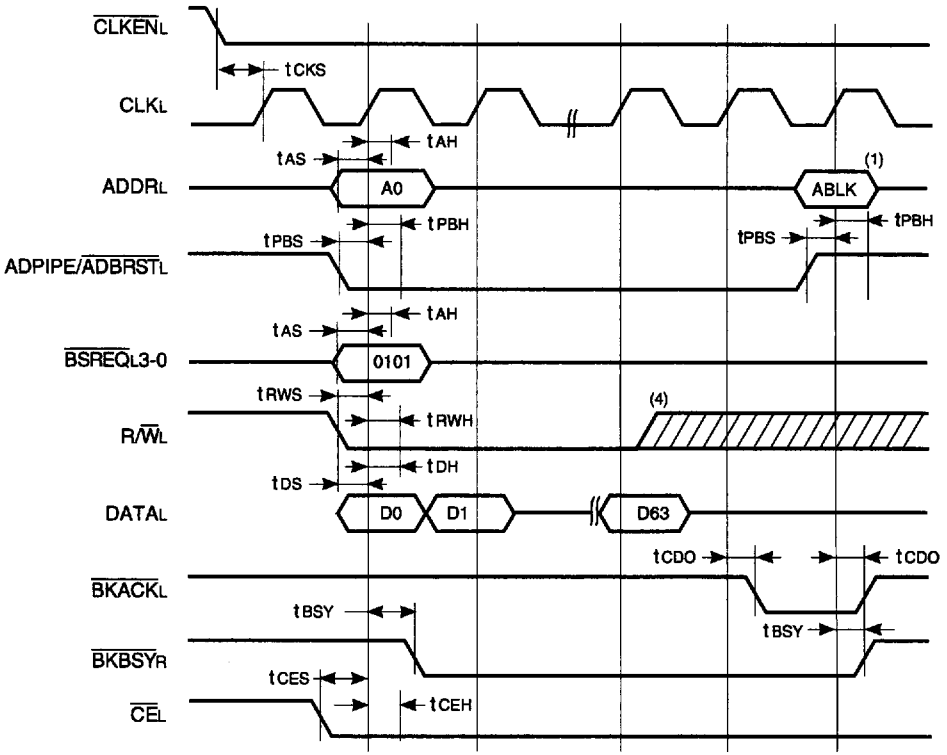
TIMING DIAGRAMS

FIGURE 4. SINGLE WORD WRITE, ONE PORT, ONE BLOCK USING $\overline{CE}$ TO RESET $\overline{BKBSY}$



Notes:
1. If $\overline{CEL}$ = H on the next CLOCKL, the $\overline{BKBSY}_R$ signals will be reset.
2. $\overline{BKBSY}_R$ will also be reset if the port address is moved to another block and clocked.

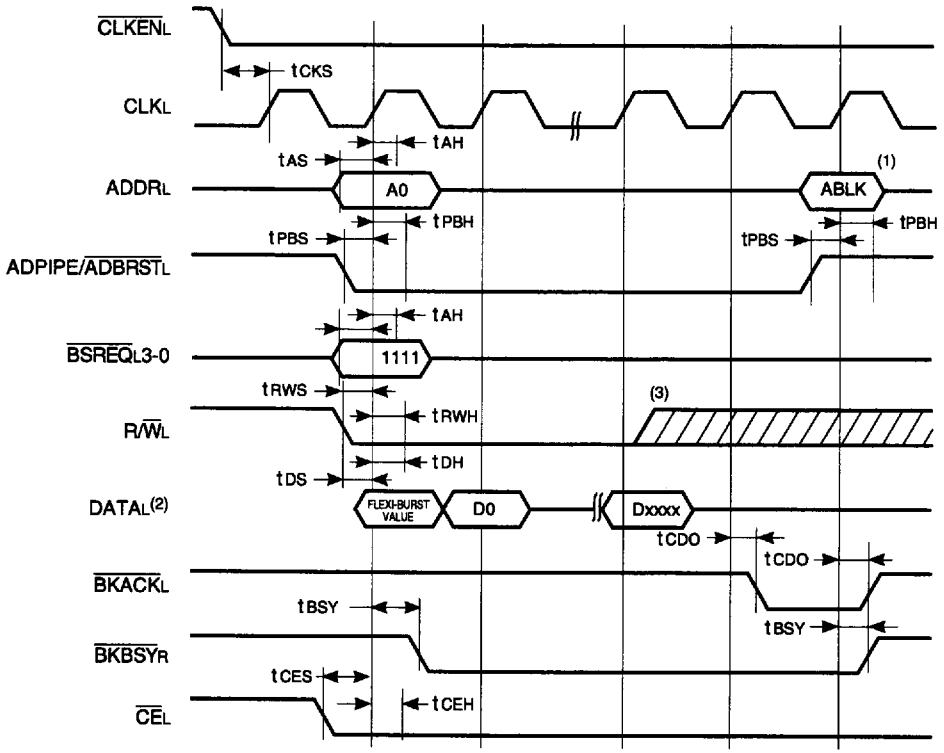
FIGURE 5. BURST WRITE ONE PORT, ONE BLOCK



Notes:

1. The address (ABLK) can be any address which is not in the block to reset control of that respective SRAM block and allow the other port to take control if requested.
2. The burst block size is set up from the BURST BLOCK SIZE TRUTH TABLE, p. 7-6.
3. $\overline{BKACK}_L$ going LOW prevents any further burst writes.
4. Must satisfy t_{RWH} at last burst clock.

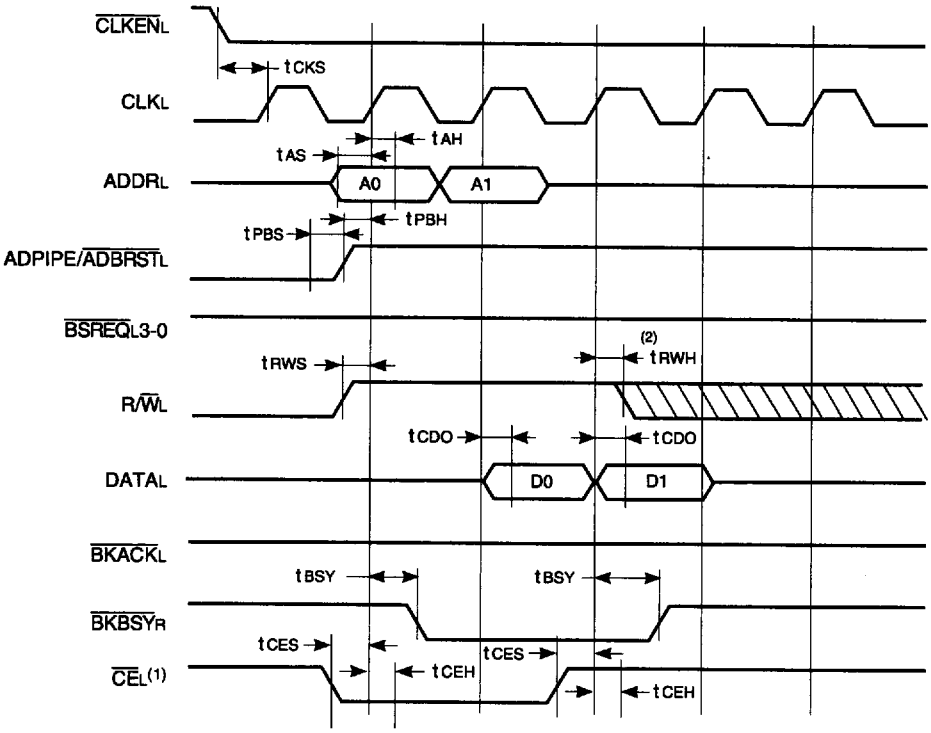
FIGURE 6. FLEXI-BURST WRITE ONE PORT, ONE BLOCK



Notes:

1. The address (ABLK) can be any address which is not in the block to reset control of that respective SRAM block and allow the other port to take control if requested.
2. Binary value placed on data bus D11-D0 sets up burst block size
3. Must satisfy t_{RWH} at last burst clock.

FIGURE 7. SINGLE-WORD PIPELINED READS, ONE BLOCK USING $\overline{CE}$ TO RESET $\overline{BKBSY}$



Notes:
1. If $\overline{CE}_L$ = H on the next CLOCKL the $\overline{BKBSY}_R$ signals will be reset.
2. Must satisfy tRWH at last burst clock.

FIGURE 8. TWO READS FOLLOWED BY A WRITE

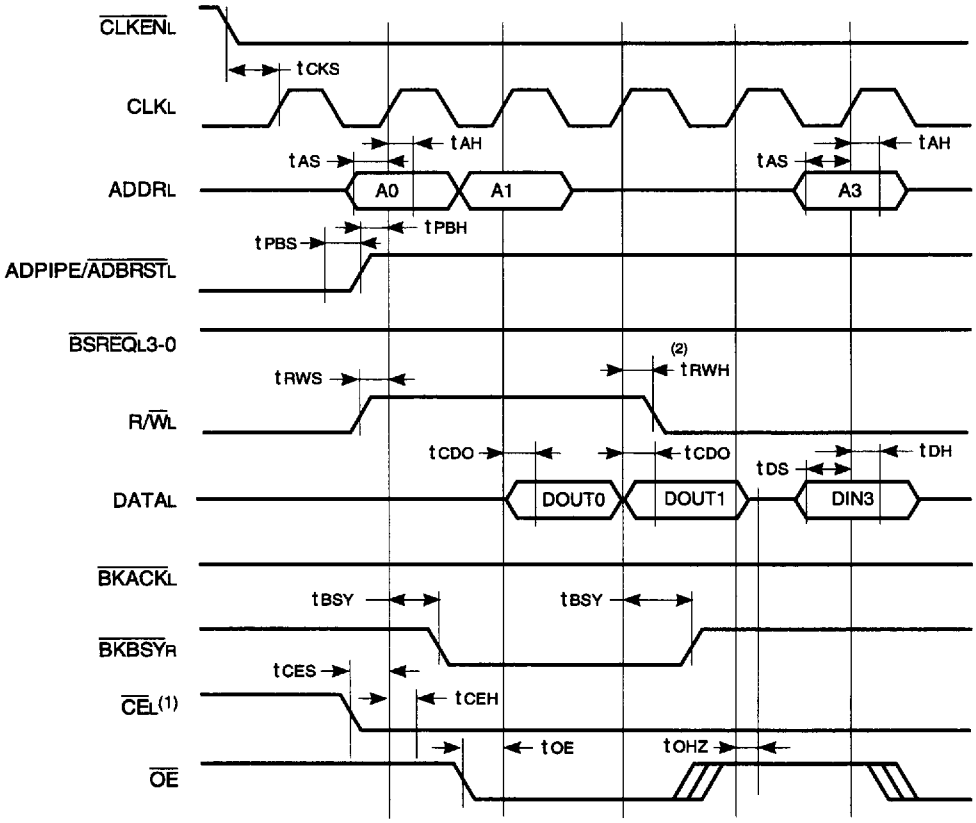
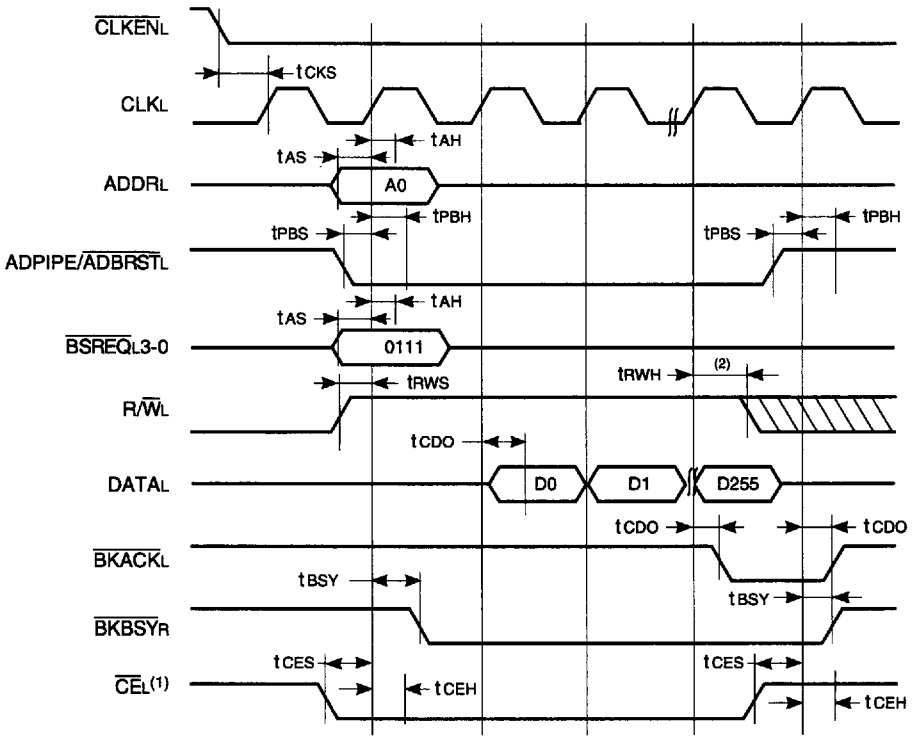
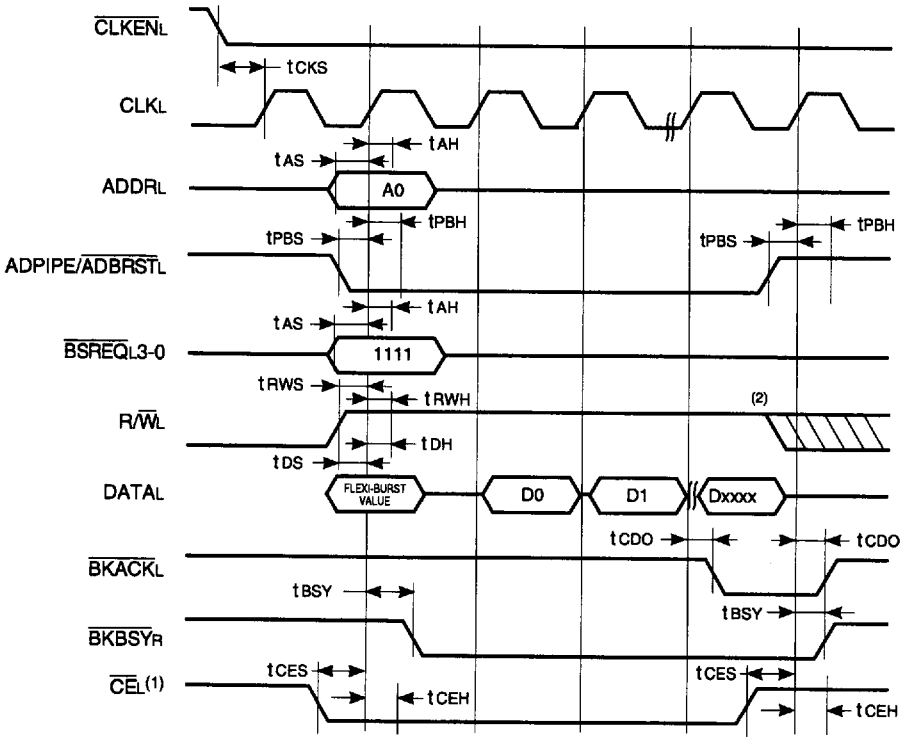


FIGURE 9. BURST READ ONE PORT USING $\overline{CE}$ TO RESET $\overline{BKBSY}$



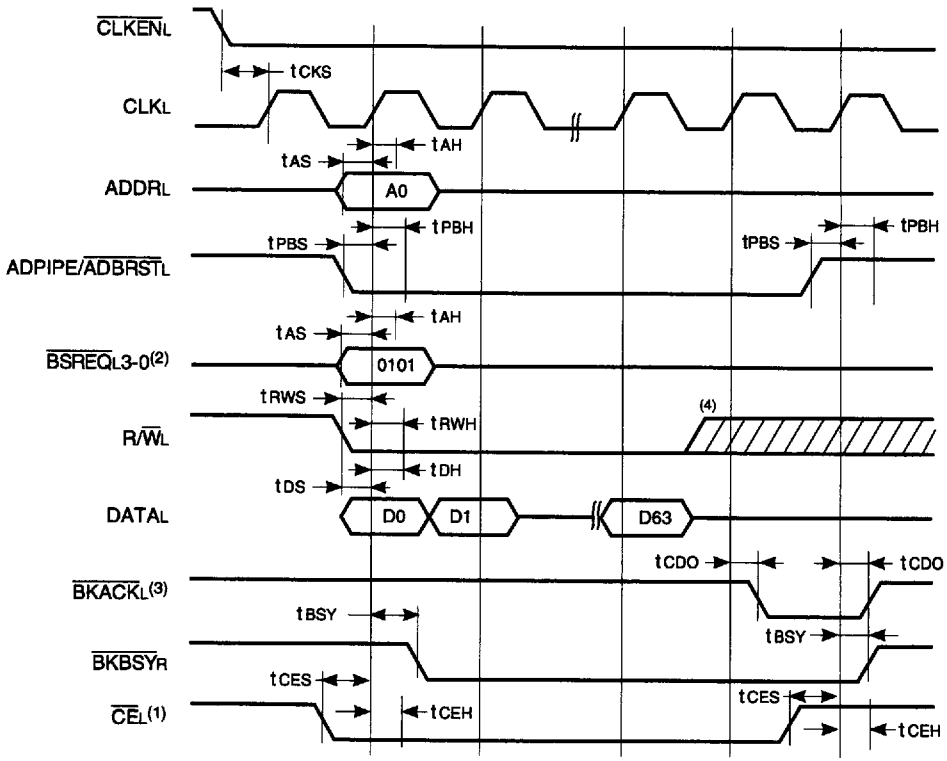
Notes:
1. If $\overline{CE}_L$ = H on the next CLOCK$_L$ the $\overline{BKBSY}_R$ signals will be reset.
2. Must satisfy t_{RWH} at last burst clock.

FIGURE 10. FLEXI-BURST READ ONE PORT USING $\overline{CE}$ TO RESET $\overline{BKBSY}$



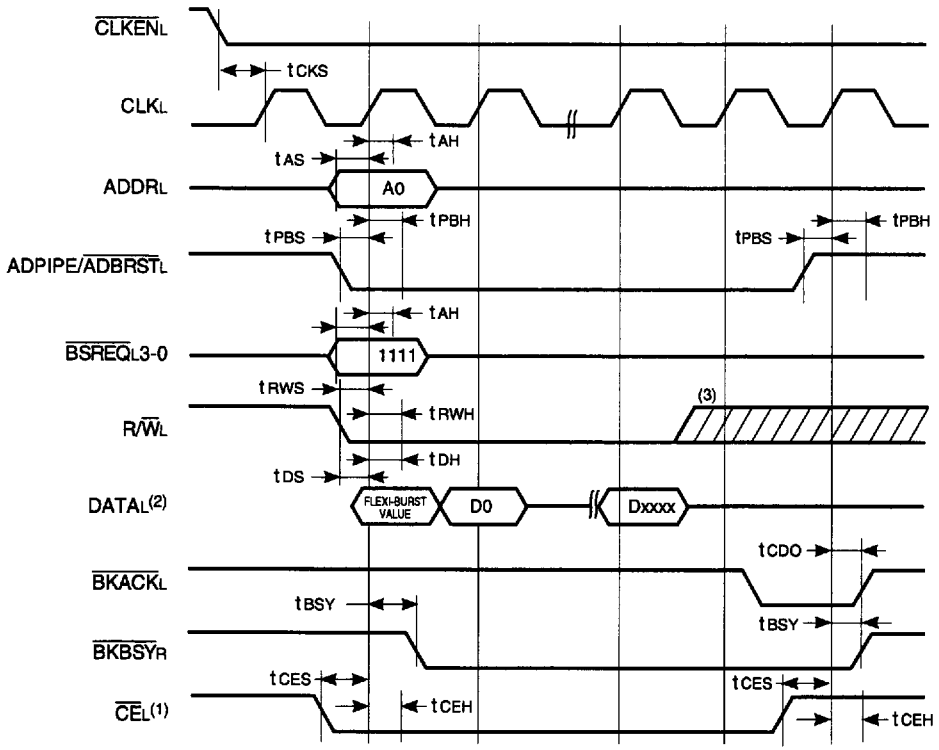
Notes:
1. If $\overline{CE}_L$ = H on the next $CLOCK_L$ the $\overline{BKBSY}_R$ signals will be reset.
2. Must satisfy t_{RWH} at last burst clock.

FIGURE 11. BURST WRITE ONE PORT, ONE BLOCK USING $\overline{CE}$ TO RESET $\overline{BKBSY}$



Notes:
1. If $\overline{CE}_L$ = H on the next CLOCK$_L$ the $\overline{BKBSY}_R$ signals will be reset.
2. The burst block size is set up from the BURST BLOCK SIZE TRUTH TABLE, p. 7-6.
3. $\overline{BKACK}_L$ going LOW prevents any further burst writes.
4. Must satisfy t_{RWH} at last burst clock.

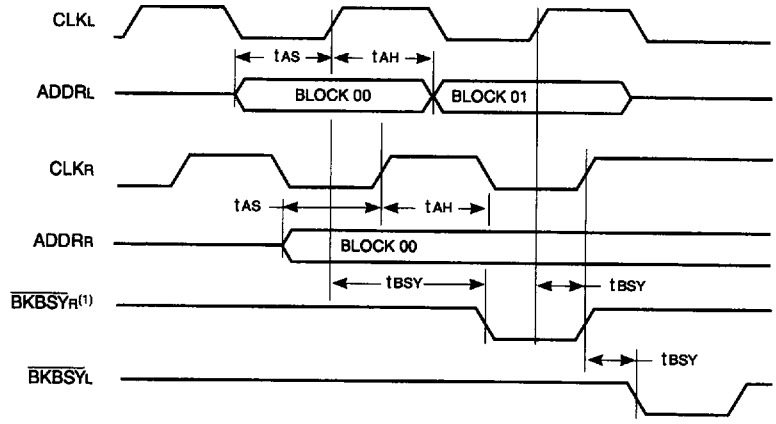
FIGURE 12. FLEXI-BURST WRITE ONE PORT, ONE BLOCK USING $\overline{CE}$ TO RESET $\overline{BKBSY}$



Notes:

1. If $\overline{CE}_L$ = H on the next CLOCK$_L$ the $\overline{BKBSY}_R$ signals will be reset.
2. Binary value placed on data bus D11-D0 sets up burst block size.
3. Must satisfy t_{RWH} at last burst clock.

FIGURE 13. BUSY AND BLOCK ARBITRATION



Note:

1. The address on the left port is clocked before the right port address. Address values are the same. Left port releases control of block address 00 by moving to block address 01. The right port gains access to block address 00 on the second clock.

POWER-ON RESET TRUTH TABLE

CLKL	CLKR	$\overline{CLKEN}_L$	$\overline{CLKEN}_R$	$\overline{CE}_L$	$\overline{CE}_R$
↑	↑	X	X	H	H

Note:
This must be done to reset the arbitration logic. Port clocks can be coincidental or different.

ORDERING INFORMATION

Example:

QS75 836 - 20 QF

Specialty Memory Product Prefix *(QS75)*

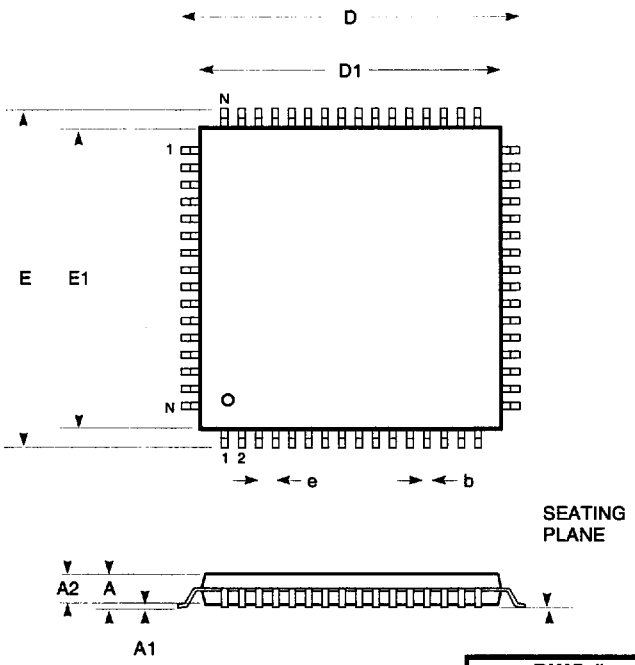
Part Number *836*

Package *QF (208-Pin QFP)*

Speed
-20 ns (50 MHz)
-25 ns (40 MHz)
-30 ns (33 MHz)

208-PIN QUAD FLAT PACK (QFP) PACKAGE DRAWING

Counter-clockwise orientation, top view



Notes:

1. Refer to applicable symbol list.
2. All dimensions are in millimeters, unless otherwise specified.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrustions are:
   D1 and E1 = 0.25 Max.
   D2 and E2 = 0.17 Max.
5. ND and NE represent number of leads in D and E directions, respectively.

DWG #	QF208	
No. of Leads (N)	208	
Symbols	**Min.**	**Max.**
A	—	3.80
A1	0.25	0.45
A2	3.30	3.40
b	0.17	0.23
D	30.40	30.80
D1	27.95	28.05
e	0.45	0.55
E	30.40	30.80
E1	27.95	28.05
L	0.40	0.60
L1	1.20	1.40
θ	0°	10°
ND/NE	52/52	