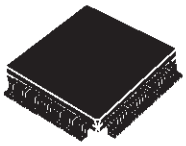
TDA7503

DUAL DSP PLUS MICRO FOR AUDIO APPLICATIONS

PRODUCT PREVIEW

- Dual 24-bit 40 MIPS DSP Cores
- 8 bit Microcontroller
- 4 receive and 5 transmit stereo channels of Serial Audio Interface
- Synchronous Serial Interface for communication with external processor
- FIFO based mailboxes for inter-processor communications
- External Memory Interface to 128Kb SRAM or 1Mb DRAM
- CORDIC co-processor
- Programmable PLL to suite wide range of external crystal oscillation frequencies
- SPI control interface
- Powerful debug interfaces
- 1280 words Program Memory for DSP1, 768 words Program Memory for DSP0
- 256 words X and Y Data RAM and Data ROM for each DSP
- 256 byte Data RAM for Microcontroller
- 768 byte Auxiliary RAM for Microcontroller

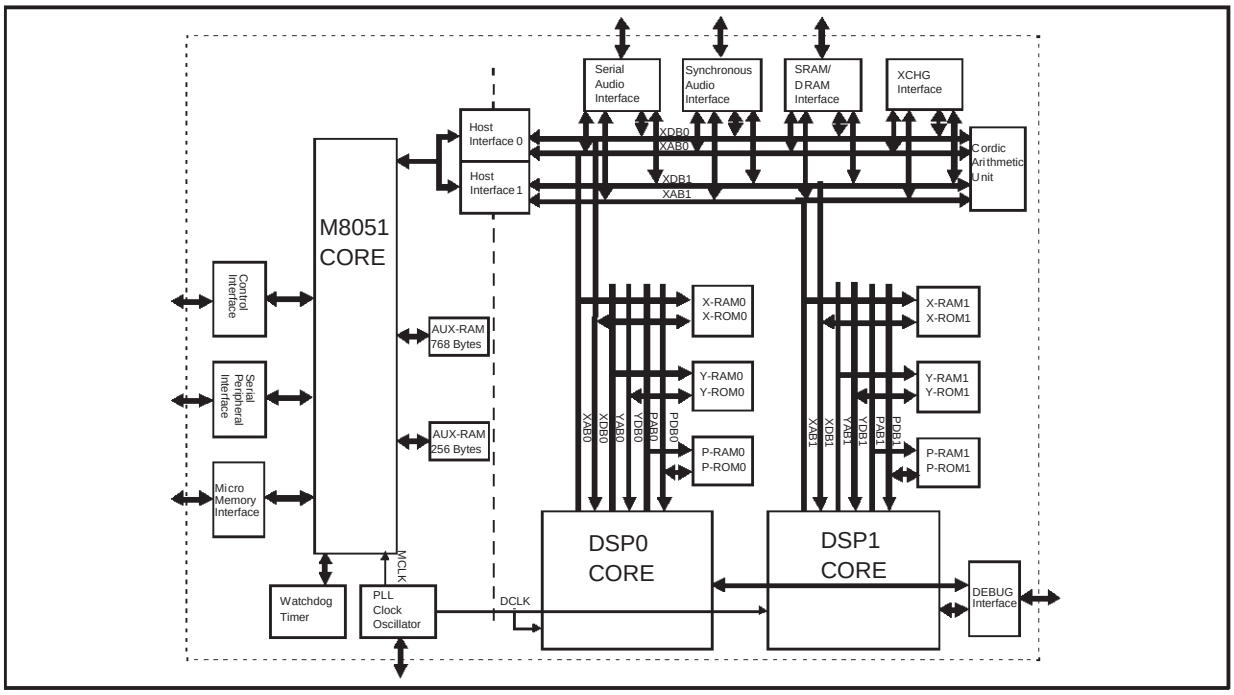


TQFP100

DESCRIPTION

The device is a high-performance Digital Signal Processing IC particularly suited to Audio applications. The device contains two 24-bit 40 MIPS DSP cores delivering a total of 80 MIPS of DSP processing power. There is also an embedded 8-bit Microcontroller to handle all control functions. All data and program memories for both DSP cores are on-chip. A variety of highly programmable and flexible peripheral blocks for both the Microcontroller and the DSPs have been integrated to form a powerful audio processing system on a single chip.

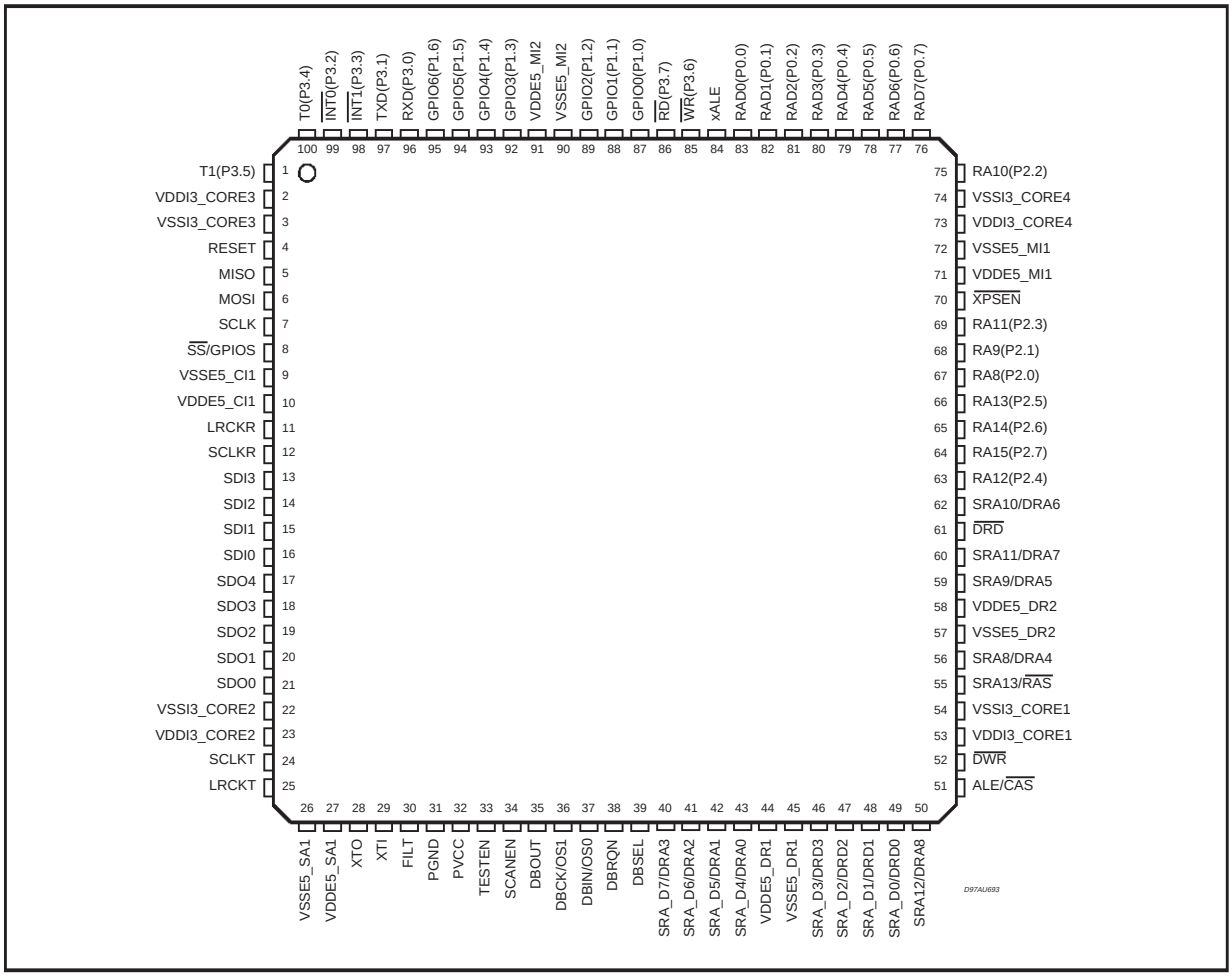
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DDC}	Core DC Supply voltage	-0.5 to 5	V
V_{DDP}	Pads DC Supply voltage	-0.5 to 6.5	V
V_I, V_{IN}	Digital or analog input voltage	-0.5 to (V_{DDP} +0.5)	V
T_{op}	Operative temperature range	-40 to 85	°C
T_{stg}	Storage temperature range (plastic)	-55 to 150	°C

PIN CONNECTION



THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}amb}$	Thermal resistance Junction to Ambient	85	°C/W

PIN DESCRIPTION

N.	Name	Type	Reset Status (1)	Function
11	LRCKR	I	–	Audio Serial Port Receive Left/Right Frame Sync. The Left/Right select signal for received serial audio data. This signal has a frequency equal to the audio sample rate.
12	SCLKR	I	–	Audio Serial Port Receive Bit Clock. SCLK clocks received digital audio data into pins SDI0, SDI1, SDI2, and SDI3
16	SDI0	I	–	Stereo Digital Audio Data. SDI0 is a stereo digital audio data input pin channel 0.
15	SDI1	I	–	Stereo Digital Audio Data. SDI1 is a stereo digital audio data input pin channel 1.
14	SDI2	I	–	Stereo Digital Audio Data. SDI2 is a stereo digital audio data input pin channel 2.
13	SDI3	I	–	Stereo Digital Audio Data / Serial Receive Data. SDI3 is a stereo digital audio data input pin and is multiplexed with the SSI's Serial Receive Data Input channel 3.
25	LRCKT	I	–	Audio Serial Port Transmit Left/Right Frame Sync /Frame Sync. The Left/Right select signal for transmitted serial audio data. This signal has a frequency equal to the audio sample rate. This signal is multiplexed with the SSI's Frame Sync Input.
24	SCLKT	I	–	Audio Serial Port Transmit Bit Clock/SSI Serial Bit Clock. SCLK clocks digital audio data out of pins SDO0, SDO1, SD02, SD03, and SD04. This pin is multiplexed with the SSI's serial bit clock.
21	SDO0	O	High	Stereo Digital Audio Data. SDO0 is a stereo digital audio data output pin channel 0.
20	SDO1	O	High	Stereo Digital Audio Data. SDO1 is a stereo digital audio data output pin channel 1.
19	SDO2	O	High	Stereo Digital Audio Data. SDO2 is a stereo digital audio data output pin channel 2.
18	SDO3	O	High	Stereo Digital Audio Data. SDO3 is a stereo digital audio data output pin channel 3.
17	SDO4	O	High	Stereo Digital Audio Data /Serial Transmit Data. SDO4 is a stereo digital audio data output pin and is multiplexed with the SSI's Serial Transmit Data Output channel 4.
34	SCANEN	I	–	SCAN Enable. Enable SCAN Path and MUXing of SCANIN and SCANOUT Pins.
33	TESTEN	I	–	Test Enable. Enable Scan Mode Clocks. An active low signal will enable the same clock to all scan chains. This pin also makes all latches transparent.
49	SRA_D0/DRD0	I/O	I	DSP SRAM Multiplexed Address/Data Line 0/DSP DRAM Data Line 0.When in SRAM Mode these pins act as the EMI multiplexed address and data line 0. When in DRAM Mode they act as the EMI data line 0.
48	SRA_D1/DRD1	I/O	I	DSP SRAM Multiplexed Address/Data Line 1/DSP DRAM Data Line 1.When in SRAM Mode these pins act as the EMI multiplexed address and data line 1. When in DRAM Mode they act as the EMI data line 1.
47	SRA_D2/DRD2	I/O	I	DSP SRAM Multiplexed Address/Data Line 2/DSP DRAM Data Line 2.When in SRAM Mode these pins act as the EMI multiplexed address and data line 2. When in DRAM Mode they act as the EMI data line 2.
46	SRA_D3/DRD3	I/O	I	DSP SRAM Multiplexed Address/Data Line 3/DSP DRAM Data Line 3.When in SRAM Mode these pins act as the EMI multiplexed address and data line 3. When in DRAM Mode they act as the EMI data line 3.
43	SRA_D4/DRA0	I/O	O, High	DSP SRAM Multiplexed Address/Data Line 4/DSP DRAM Address Line 0. When in SRAM Mode these pins act as the EMI multiplexed address and data line 4. When in DRAM Mode they act as the EMI address line 0.

PIN DESCRIPTION (continued)

N.	Name	Type	Reset Status (1)	Function
42	SRA_D5/DRA1	I/O	O, High	DSP SRAM Multiplexed Address/Data Line 5/DSP DRAM Address Line 1. When in SRAM Mode these pins act as the EMI multiplexed address and data line 5. When in DRAM Mode they act as the EMI address line 1.
41	SRA_D6/DRA2	I/O	O, High	DSP SRAM Multiplexed Address/Data Line 6/DSP DRAM Address Line 2. When in SRAM Mode these pins act as the EMI multiplexed address and data line 6. When in DRAM Mode they act as the EMI address line 2.
40	SRA_D7/DRA3	I/O	O, High	DSP SRAM Multiplexed Address/Data Line 7/DSP DRAM Address Line 3. When in SRAM Mode these pins act as the EMI multiplexed address and data line 7. When in DRAM Mode they act as the EMI address line 3.
56	SRA8/DRA4	O	High	DSP SRAM Address Line 8/DSP DRAM Address Line 4. When in SRAM Mode these pins act as the EMI address line 8. When in DRAM Mode they act as the EMI address line 4.
59	SRA9/DRA5	O	High	DSP SRAM Address Line 9/DSP DRAM Address Line 5. When in SRAM Mode these pins act as the EMI address line 9. When in DRAM Mode they act as the EMI address line 5.
62	SRA10/DRA6	O	High	DSP SRAM Address Line 10/DSP DRAM Address Line 6. When in SRAM Mode these pins act as the EMI address line 10.When in DRAM Mode they act as the EMI address line 6.
60	SRA11/DRA7	O	High	DSP SRAM Address Line 11/DSP DRAM Address Line 7. When in SRAM Mode these pins act as the EMI address line 11. When in DRAM Mode they act as the EMI address line 7.
50	SRA12/DRA8	O	High	DSP SRAM Address Line 12/DSP DRAM Address Line 8. When in SRAM Mode these pins act as the EMI address line 12. When in DRAM Mode they act as the EMI address line 8.
55	SRA13/$\overline{RAS}$	O	High	DSP SRAM Address Line 13/DRAM Row Address Strobe. When in SRAM Mode this pin acts as the EMI address lines 13. When in DRAM Mode this pin acts as the row address strobe.
51	ALE/$\overline{CAS}$	O	High	DSP SRAM Address latch enable/colomn Address. When in SRAM Mode this pin acts as the EMI Address Latch Enable. When in DRAM Mode this pin acts as the column address strobe.
52	$\overline{DWR}$	O	High	DSP SRAM Write Enable/DRAM Write Enable. This pin serves as the write enable for the EMI when in DRAM and SRAM Modes.
61	$\overline{DRD}$	O	High	DSP SRAM Read Enable/DRAM Read Enable. This pin serves as the read enable for the EMI when in DRAM and SRAM Modes.
36	DBCK/OS1	I/O	I	Debug Port Bit Clock/Chip Status 1. The serial clock for the Debug Port is provided when an input. When an output, together with OS0 provides information about the chip status. Can also be used as GPIO for the 8051.
37	DBIN/OS0	I/O	I	Debug Port Serial Input/Chip Status 0. The serial data input for the Debug Port is provided when an input. When an output, together with OS1 provides information about the chip status. Can also be used as GPIO for the 8051.
35	DBOUT	I/O	I	Debug Port Serial Output. The serial data output for the Debug Port. Can also be used as a GPIO for the 8051.
38	DBRQN	I	–	Debug Port Request Input. Means of entering the Debug mode of operation.
39	DBSEL	I	–	Debug Port MUX Selection. Selects either DSP0 or DSP1 to be connected to the Debug Port pins.
67	RA8(P2.0)	I/O	I	Microcontroller High Byte Address Lines. This pin is the address line 8 of a 16 bit address, for external EPROM and memory mapped devices. It can also act as GPIO using the P2 and P2DIR registers.
68	RA9(P2.1)	I/O	I	Microcontroller High Byte Address Lines. This pin is the address line 9 of a 16 bit address, for external EPROM and memory mapped devices. It can also act as GPIO using the P2 and P2DIR registers.

PIN DESCRIPTION (continued)

N.	Name	Type	Reset Status (1)	Function
75	RA10(P2.2)	I/O	I	Microcontroller High Byte Address Lines. This pin is the address line 10 of a 16 bit address, for external EPROM and memory mapped devices. It can also act as GPIO using the P2 and P2DIR registers.
69	RA11(P2.3)	I/O	I	Microcontroller High Byte Address Lines. This pin is the address line 11 of a 16 bit address, for external EPROM and memory mapped devices. It can also act as GPIO using the P2 and P2DIR registers.
63	RA12(P2.4)	I/O	I	Microcontroller High Byte Address Lines. This pin is the address line 12 of a 16 bit address, for external EPROM and memory mapped devices. It can also act as GPIO using the P2 and P2DIR registers.
66	RA13(P2.5)	I/O	I	Microcontroller High Byte Address Lines. This pin is the address line 13 of a 16 bit address, for external EPROM and memory mapped devices. It can also act as GPIO using the P2 and P2DIR registers.
65	RA14(P2.6)	I/O	I	Microcontroller High Byte Address Lines. This pin is the address line 14 of a 16 bit address, for external EPROM and memory mapped devices. It can also act as GPIO using the P2 and P2DIR registers.
64	RA15(P2.7)	I/O	I	Microcontroller High Byte Address Lines. This pin is the address line 15 of a 16 bit address, for external EPROM and memory mapped devices. It can also act as GPIO using the P2 and P2DIR registers.
83	RAD0(P0.0)	I/O	I	Microcontroller Address/Data Pins. This pin is the multiplexed address and data line bit 0 for external EPROM and memory mapped peripherals. It can also act as GPIO using the P0 and P0DIR registers.
82	RAD1(P0.1)	I/O	I	Microcontroller Address/Data Pins. This pin is the multiplexed address and data line bit 1 for external EPROM and memory mapped peripherals. It can also act as GPIO using the P0 and P0DIR registers.
81	RAD2(P0.2)	I/O	I	Microcontroller Address/Data Pins. This pin is the multiplexed address and data line bit 2 for external EPROM and memory mapped peripherals. It can also act as GPIO using the P0 and P0DIR registers.
80	RAD3(P0.3)	I/O	I	Microcontroller Address/Data Pins. This pin is the multiplexed address and data line bit 3 for external EPROM and memory mapped peripherals. It can also act as GPIO using the P0 and P0DIR registers.
79	RAD4(P0.4)	I/O	I	Microcontroller Address/Data Pins. This pin is the multiplexed address and data line bit 4 for external EPROM and memory mapped peripherals. It can also act as GPIO using the P0 and P0DIR registers.
78	RAD5(P0.5)	I/O	I	Microcontroller Address/Data Pins. This pin is the multiplexed address and data line bit 5 for external EPROM and memory mapped peripherals. It can also act as GPIO using the P0 and P0DIR registers.
77	RAD6(P0.6)	I/O	I	Microcontroller Address/Data Pins. This pin is the multiplexed address and data line bit 6 for external EPROM and memory mapped peripherals. It can also act as GPIO using the P0 and P0DIR registers.
76	RAD7(P0.7)	I/O	I	Microcontroller Address/Data Pins. This pin is the multiplexed address and data line bit 7 for external EPROM and memory mapped peripherals. It can also act as GPIO using the P0 and P0DIR registers.
84	xALE	I/O	I	Microcontroller External Address Latch Enable. This pin is the address latch enable. A logic high indicates that address/data lines 7 through 0 represent an address. Inactive for Program/Data fetches from internal AUX.
85	$\overline{WR}$(P3.6)	I/O	I	Microcontroller Write Strobe. External data memory write strobe. This pin can also act as GPIO using the P3 and P3DIR registers.
86	$\overline{RD}$(P3.7)	I/O	I	Microcontroller Read Strobe. External data memory read strobe. Active Low, or GPIO. This pin can also act as GPIO using the P3 and P3DIR registers. Disabled by setting the RDSEL bit in the PINCTL register.
70	$\overline{XPSEN}$	I/O	I	Microcontroller External Program Memory Enable. External program memory enable pin. Active Low. Changes functionality to RD when Microcontroller is fetching instructions out of internal AUX ram. Controlled by the PSSEL and PSBIT bits in the PINCTL register.

PIN DESCRIPTION (continued)

N.	Name	Type	Reset Status (1)	Function
4	RESET	I/O	I	System Reset. A logic low level applied to RESET input initializes the microcontroller. The micro is responsible for initializing the DSPs. If the watchdog timer overflow occurs this pin is driven low for 1 watchdog timer cycle. During Debug Mode if this pin is pulled low in while the DBRQN line is pulled low then the DSP pointed to by the DBSEL pin will be reset.
96	RXD(P3.0)	I/O	I	Microcontroller Standard Serial Interface (Asynchronous) Input Data. Or GPIO. This pin can also act as GPIO using the P3 and P3DIR registers.
97	TXD(P3.1)	I/O	I	Microcontroller Standard Serial Interface (Asynchronous) Output Data. Or GPIO. This pin can also act as GPIO using the P3 and P3DIR registers.
99	$\overline{\text{INT0}}$(P3.2)	I/O	I	Microcontroller Interrupt 0. When pulled low, INT0 asserts a microcontroller external interrupt. In addition, if this pin is pulled low during powerdown this allows the M8051 to resume executing intructions where it left off. This pin can also act as GPIO using the P3 and P3DIR registers.
98	$\overline{\text{INT1}}$(P3.3)	I/O	I	Microcontroller Interrupt 1. When pulled low, INT1 asserts a microcontroller external interrupt. In addition, if this pin is pulled low during powerdown this allows the M8051 to resume executing intructions where it left off. This pin can also act as GPIO using the P3 and P3DIR registers.
100	T0(P3.4)	I/O	I	Microcontroller Timer 0 External Input. Input event clock for timer 0, or GPIO. This pin can also act as GPIO using the P3 and P3DIR registers.
1	T1(P3.5)	I/O	I	Microcontroller Timer 1 External Input. Input event clock for timer 1, or GPIO. This pin can also act as GPIO using the P3 and P3DIR registers.
87	GPIO0(P1.0)	I/O	I	Microcontroller General Purpose. This GPIO line can be configured to be digital input or output by writing to the P1 and P1DIR registers.This pin is tri-stated while the RESET pin is held low and is pulled low when RESET is released. This pin will be pulled high when in IDLE or PWRDN modes.
88	GPIO1(P1.1)	I/O	I	Microcontroller General Purpose. This GPIO line can be configured to be digital input or output by writing to the P1 and P1DIR registers. At reset it is configured as an input with the output tri-stated.
89	GPIO2(P1.2)	I/O	I	Microcontroller General Purpose. This GPIO line can be configured to be digital input or output by writing to the P1 and P1DIR registers. At reset it is configured as an input with the output tri-stated.
92	GPIO3(P1.3)	I/O	I	Microcontroller General Purpose. This GPIO line can be configured to be digital input or output by writing to the P1 and P1DIR registers. At reset it is configured as an input with the output tri-stated.
93	GPIO4(P1.4)	I/O	I	Microcontroller General Purpose. This GPIO line can be configured to be digital input or output by writing to the P1 and P1DIR registers. At reset it is configured as an input with the output tri-stated.
94	GPIO5(P1.5)	I/O	I	Microcontroller General Purpose. This GPIO line can be configured to be digital input or output by writing to the P1 and P1DIR registers. At reset it is configured as an input with the output tri-stated.
95	GPIO6(P1.6)	I/O	I	Microcontroller General Purpose. This GPIO line can be configured to be digital input or output by writing to the P1 and P1DIR registers. At reset it is configured as an input with the output tri-stated.
7	SCLK	I/O	I	Microcontroller General Purpose. Each of the six GPIO lines can be individually configured to be digital input or output by writing to the P1 and P1DIR registers. All GPIOs are configured to be inputs with the outputs tri-stated except for P1.0. This pin is tri-stated during while the RESET pin is held low and is pulled low when RESET is released. This pin will be pulled high when in IDLE or PWRDN modes.
6	MOSI	I/O	I	Microcontroller SPI Master Output Slave Input Serial Data . Serial Data Output for SPI type serial port when in SPI Master Mode and Serial Data Input when in SPI Slave Mode.

PIN DESCRIPTION (continued)

N.	Name	Type	Reset Status (1)	Function
5	MISO	I/O	I	Microcontroller SPI Master Input Slave Output Serial Data . Serial Data Input for SPI style serial port when in SPI Master Mode and Serial Data Output when in SPI Slave Mode.
8	$\overline{SS}$/GPIOS	I/O	I	Microcontroller SPI Slave Select . Slave Select Input for SPI type serial port. This pin can be used as a GPIO when the SPI is disabled or in master mode.
32	PVCC	I	–	PLL Clock Power Supply . Vdd Pin for PLL Clock Oscillator.
28	XTO	O	High	Crystal Oscillator Output. Crystal Oscillator output drive.
29	XTI	I	–	Crystal Oscillator Input. External Clock Input or crystal connection.
30	FILT	O	High	PLL Loop Filter Capacitor Output. Capacitor connected between FILT and XGND establishes primary PLL.
31	PGND	I	–	PLL Clock Ground Input. Ground connection for oscillator circuit.
53	VDDI3_CORE1	PWR	–	3.3V core supply.
23	VDDI3_CORE2	PWR	–	3.3V core supply.
2	VDDI3_CORE3	PWR	–	3.3V core supply.
73	VDDI3_CORE4	PWR	–	3.3V core supply.
54	VSSI3_CORE1	GND	–	Core ground.
22	VSSI3_CORE2	GND	–	Core ground.
3	VSSI3_CORE3	GND	–	Core ground.
74	VSSI3_CORE4	GND	–	Core ground.
27	VDDE5_SA1	PWR	–	5V supply for SAI pads.
26	VSSE5_SA1	GND	–	Ground for SAI pads.
10	VDDE5_CI1	PWR	–	5V supply for Control Interface Pads.
9	VSSE5_CI1	GND	–	Ground for Control Interface Pads.
71	VDDE5_MI1	PWR	–	5V supply for Micro Memory Interface Pads.
91	VDDE5_MI2	PWR	–	5V supply for Micro Memory Interface Pads.
72	VSSE5_MI1	GND	–	Ground for Micro Memory Interface Pads.
90	VSSE5_MI2	GND	–	Ground for Micro Memory Interface Pads.
44	VDDE5_DR1	PWR	–	5V supply for DSP EMI Interface Pads.
58	VDDE5_DR2	PWR	–	5V supply for DSP EMI Interface Pads.
45	VSSE5_DR1	GND	–	Ground for DSP EMI Interface Pads.
57	VSSE5_DR2	GND	–	Ground for DSP EMI Interface Pads.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{DDC}	3.3V Power Supply Voltage		3	3.3	3.6	V
V_{DDP}	5V Power Supply Voltage		4.5	5	5.5	V
Tj	Operating Junction Temperature		-40		125	°C

GENERAL INTERFACE ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Note
I_{il}	Low Level Input Current Without pull-up device	V_i = 0V			1	µA	1
I_{ih}	High Level Input Current Without pull-down device	Vi = V_{DDP}			1	µA	1
I_{oz}	Tri-state Output leakage Without pullup/down device	Vo = 0V or V_{DDP}			1	µA	1
C_{in}	Input capacitance				10	pF	2
$I_{latchup}$	I/O Latch-up Current	V < 0V, V > V_{DDP}	200			mA	
V_{esd}	Electrostatic Protection	Leakage < 1µA	2000			V	3

Note 1: The leakage currents are generally very small, < 1nA. The value given here, 1mA, is a maximum that can occur after an Electrostatic Stress on the pin.

Note 2: Guaranteed by design.

Note 3: Human Body Model.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Note
V_{il}	Low Level Input Voltage				$0.25 \cdot V_{DDP}$	V	
V_{ih}	High Level Input Voltage		$0.7 \cdot V_{DDP}$			V	
V_{ol}	Low Level Output Voltage	I_{ol} = 2mA			0.4	V	1
V_{oh}	High Level Output Voltage	I_{ol} = -2mA	V_{DDP}-0.4			V	1

Note 1: Takes into account 200mV voltage drop in both supply lines.

POWER CONSUMPTION

Symbol	Parameter	Value	Unit
P_{tot}	Maximum current for core power supply @ 3.3V	320	mA

Note: 40MHz internal DSP clock at Tamb

EXTERNAL CLOCKS (XTI Pin)

The TDA7503 system clock is externally supplied via the XTI pin.
Timings shown in this document are valid for clock rise and fall times of 3ns maximum.

Symbol	Characteristics	Value	Unit
F_{ext}	Max. Frequency @ XTI when PLL is disabled	20	MHz

When PLL is enabled see constraints for Internal Clocks.

INTERNAL CLOCKS

Symbol	Characteristics	Expression
f_{DSP_MAX}	Maximum DSP Internal Operation Frequency (dclk)	40MHz
$f_{\mu P\_MAX}$	Maximum µP (8051) Internal Operation Frequency (mclk)	20MHz
f_{DSP}	Internal DSP Clock Cycle Frequency (dclk)	$\frac{MF \cdot F_{ext}}{2 \cdot DF}$
$f_{\mu P}$	Inernal µP (8051) Clock Cycle Frequency (mclk)	$\frac{MF \cdot F_{ext}}{4 \cdot DF}$
I_{cyc_DSP}	DSP Machine Cycle Time	dclk
$I_{cyc\_\mu P}$	µP (8051) Machine Cycle Time	mclk/12

Note 1: If the DCKSRC bit of the clock control register is 0 then dclk = Fext/2.
Note 2: If the MCKSRC bit of the clock control register is 1 then mclk = Fext else of MCKSRC0 is 0 then MCLK = Fext/4.
Note 3: DF is PLL input devide factor, bits IDF [4:0] of PLL control register one.
Note 4: MF is PLL multiply devide factor, bits MP [6:0] of PLL control register zero.

PHASE LOCKED LOOP (PLL) CHARACTERISTICS

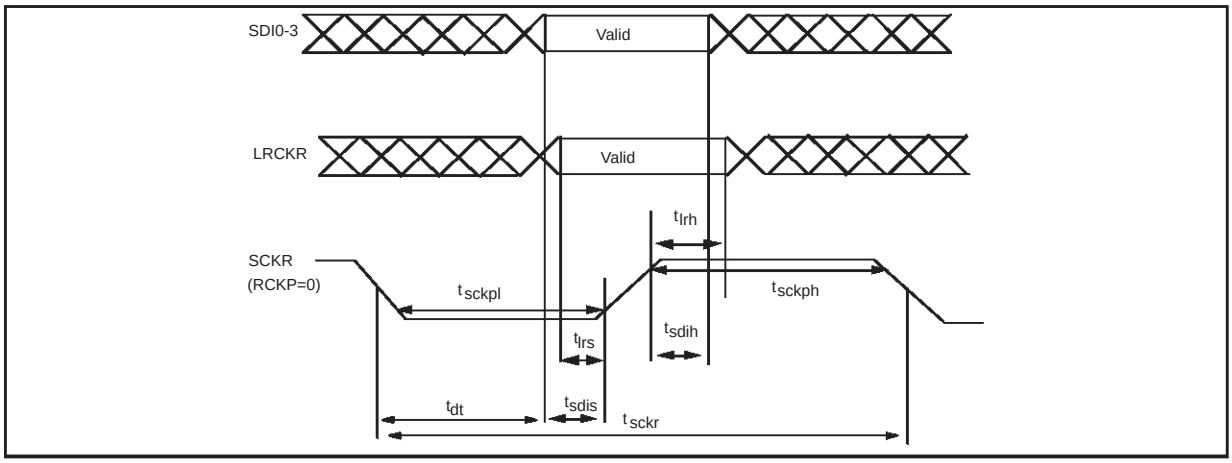
Characteristics	Expression	Value	Unit
VCO frequency when PLL enabled	$\frac{MF \cdot Fext}{DF}$	40 to 80	MHz
Recommended PLL external capacitor (pin FILT)		3.3	nF

RESET

Characteristics	Expression	Unit
Minimum RESET assertion	100/Fext	ns

SAI/SSI INTERFACE

Figure 1. SAI and SSI Timings



Timing	Description	Value	Unit
t_{sckr}	Minimum Clock Cycle	$3T_{DSP}+5$	ns
t_{dt}	SCKR active edge to data out valid	40	ns
t_{lrs}	LRCK setup time	5	ns
t_{lrh}	LRCK hold time	5	ns
t_{sdid}	SDI setup time	5	ns
t_{sdih}	SDI hold time	5	ns
t_{sckph}	Minimum SCK high time	0.35 t_{sckr}	ns
t_{sckpl}	Minimum SCK low time	0.35 t_{sckr}	ns

Note T_{DSP} = dsp master clock cycle time = $1/F_{DSP}$

Figure 2. SAI Interrupt protocol

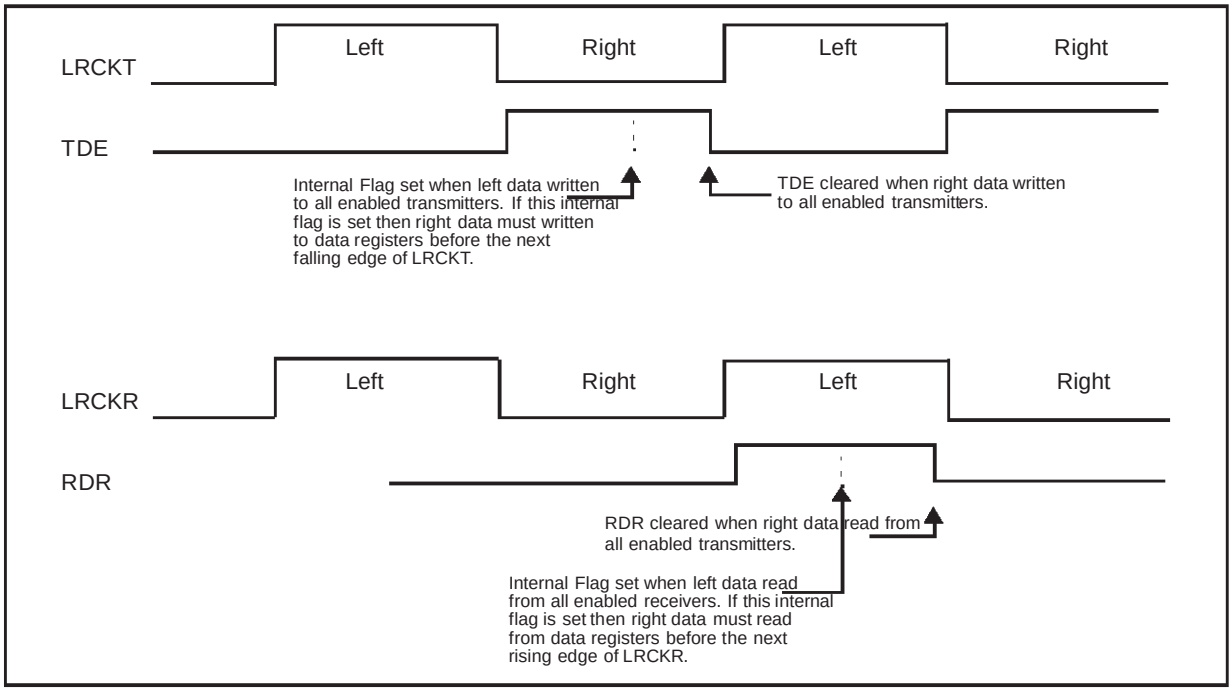


Figure 3. SAI protocol when RLRS=0; RREL=0; RCKP=1; RDIR=0.

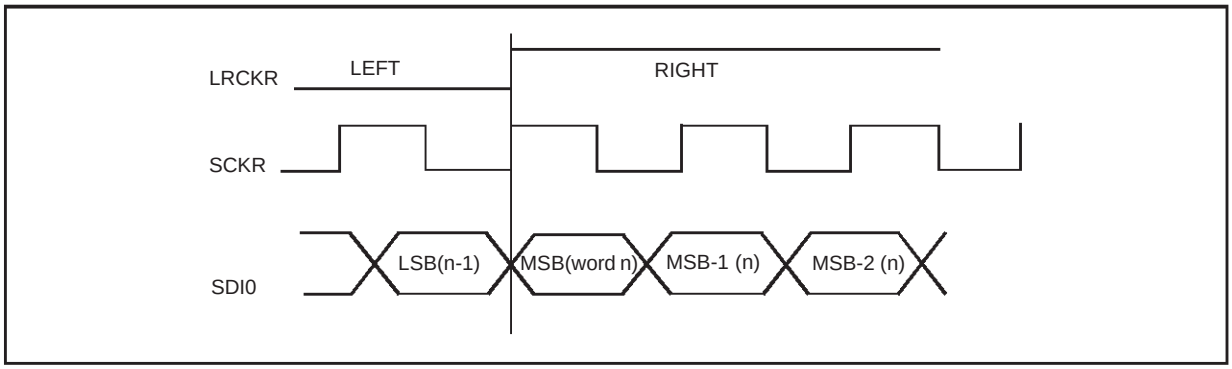


Figure 4. SAI protocol when RLRS=1; RREL=0; RCKP=1; RDIR=1.

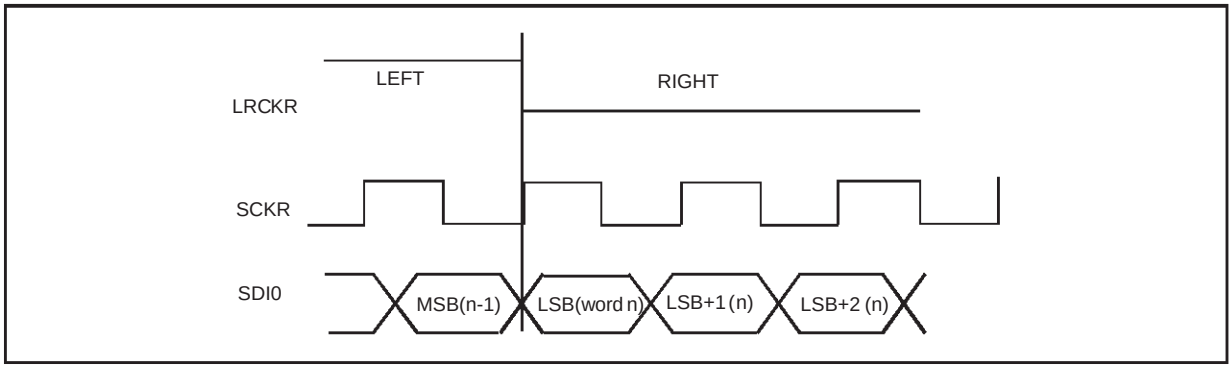


Figure 5. SAI protocol when RLRS=0; RREL=0; RCKP=0; RDIR=0.

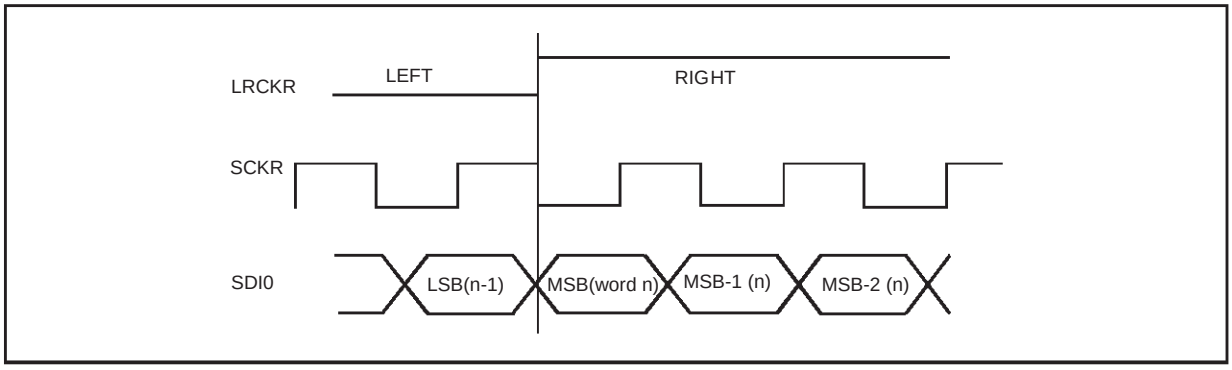


Figure 6. SAI protocol when RLRS=0; RREL=1; RCKP=1; RDIR=0.

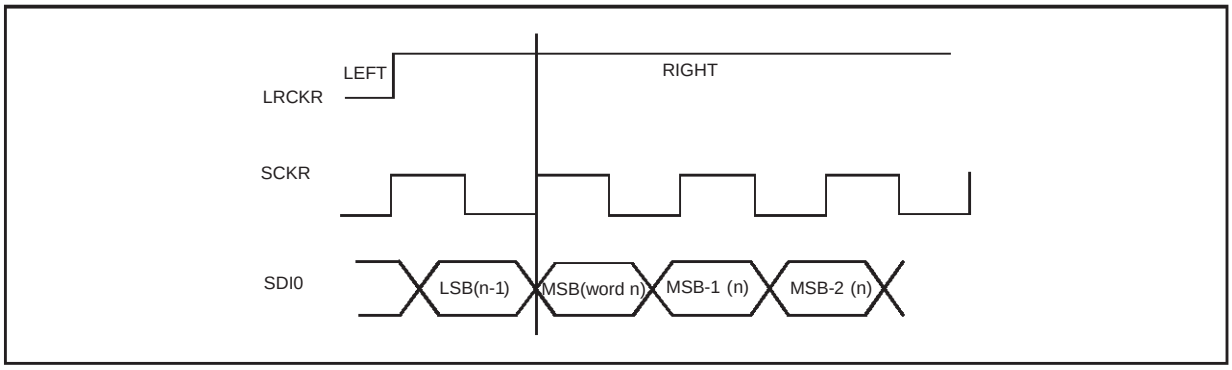
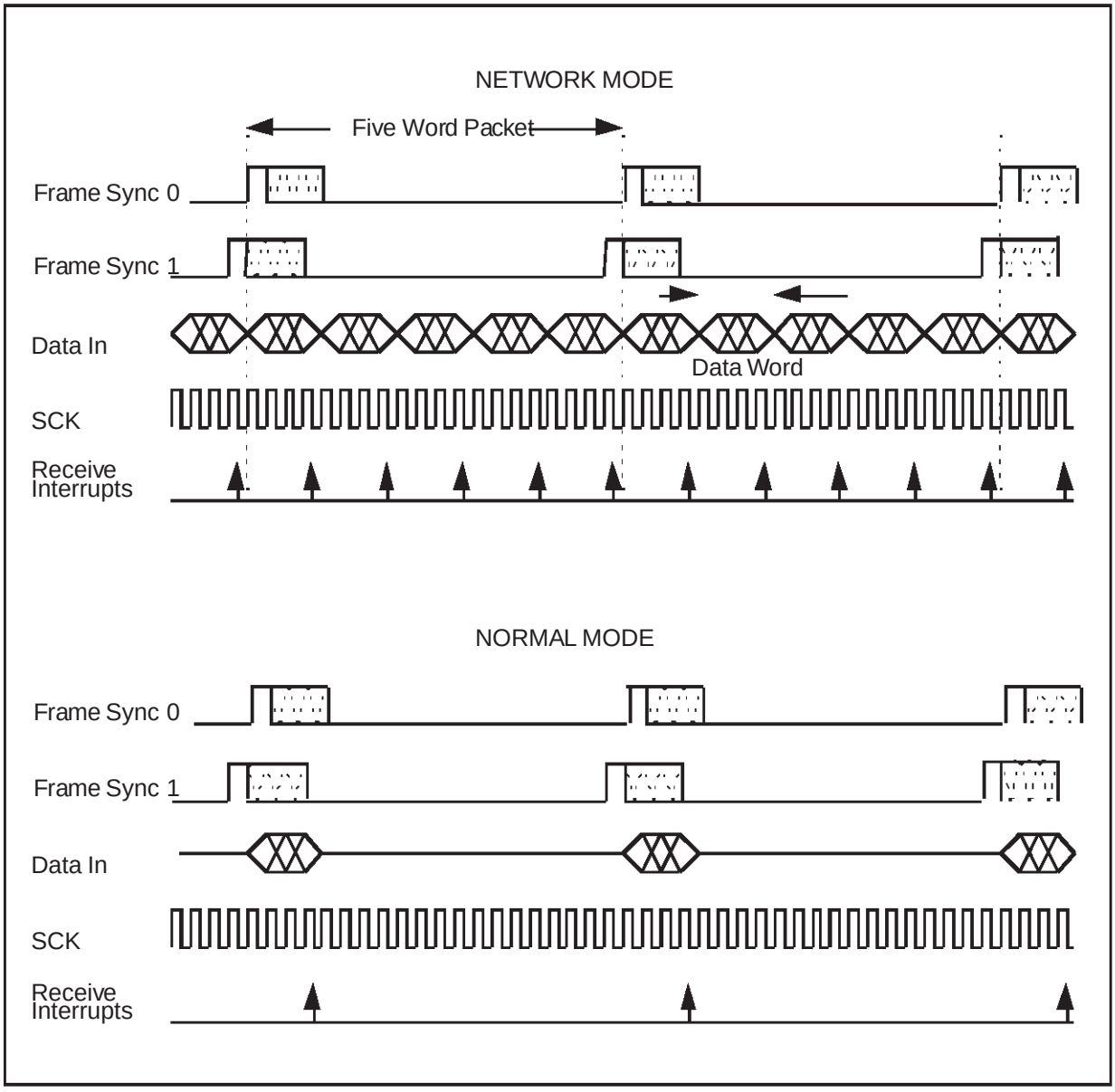


Figure 7. SSI Protocol.



The timing diagrams for the SSI Interface are shown in Figure 7 for both Network and Normal modes.

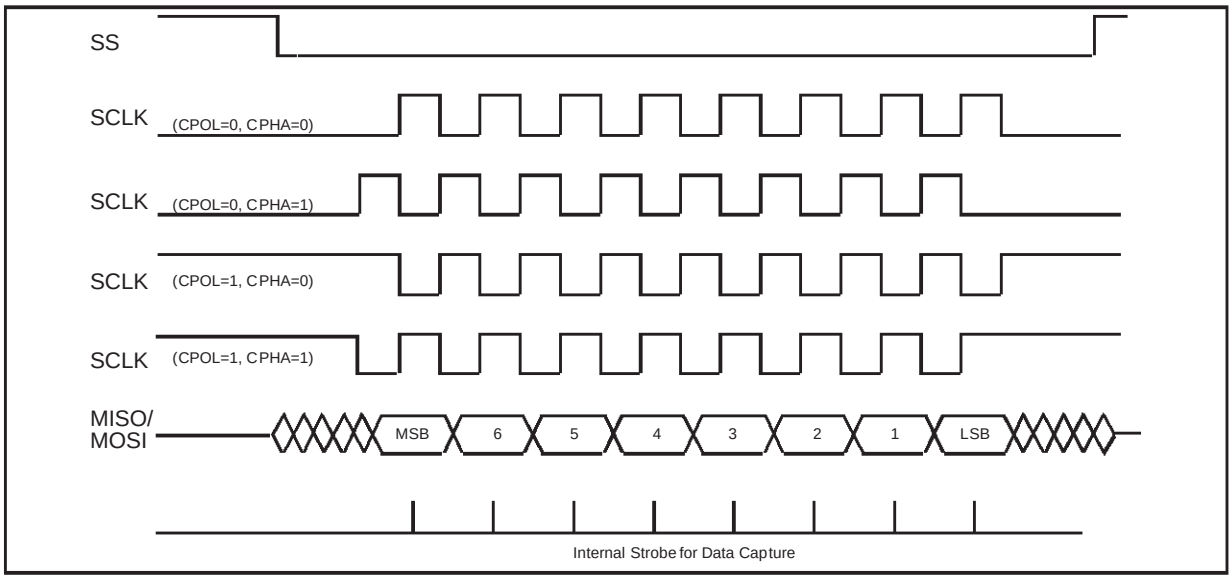
In Normal Mode the rising edge FSYNC starts the internal bit counter to allow data to be clocked in or out. When bit count is equal to the programmed word length the counter is reset and the shift register is broadside loaded into the data register. Additional SCK pulses are ignored after the counter is reset. The next word is clocked in or out starting with the next rising edge of FSYNC.

In Network Mode the rising edge FSYNC starts the internal bit counter to allow data to be clocked in or out. When bit count is equal to the programmed word length the counter is reset and the shift register is broadside loaded into the data register. At this point the FSRSD bit is set indicating that a frame sync was received with that word. After being reset the counter continues counting, clocking in the next word. Only when the next rising edge of FSYNC is detected is the packet considered complete.

SPI INTERFACE

Symbol	Description	Min Value	Unit
	MASTER		
t_{sclk}	Clock Cycle	mclk/12	µs
t_{dtr}	Sclk edge to MOSI valid	40	µs
t_{dts}	MISO setup time	5	µs
	SLAVE		
t_{sclk}	Clock Cycle	mclk/6	µs
t_{dtr}	Sclk edge to MOSI valid	40	µs
t_{dts}	MISO setup time	5	µs
t_{sckph}	Minimum SCK high time	mclk/12	µs
t_{sckpl}	Minimum SCK low time	mclk/12	µs

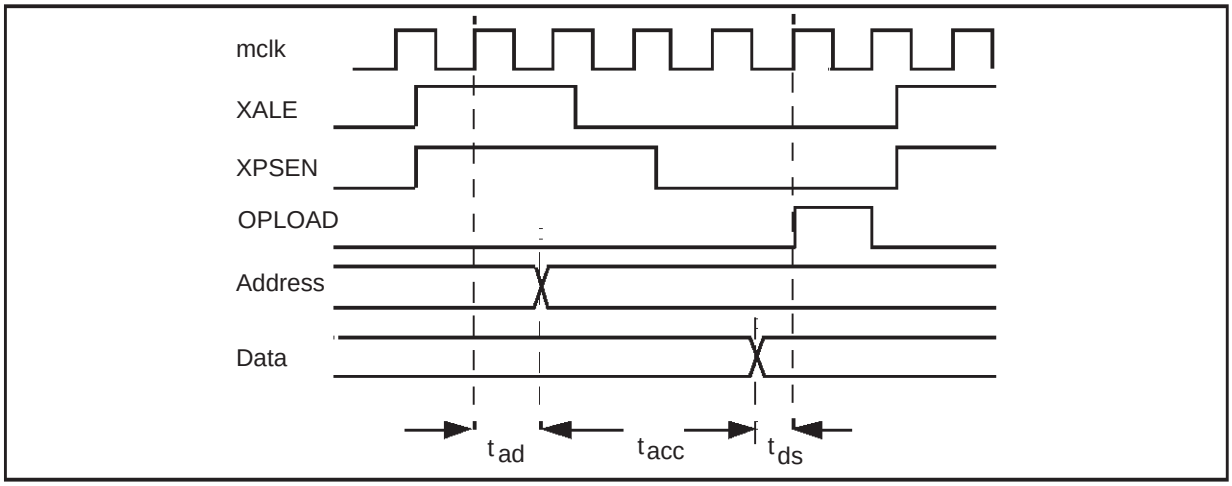
Figure 8. SPI Clocking scheme.



MICRO MEMORY INTERFACE

Figure 9. Timing diagram for External Memory Interface

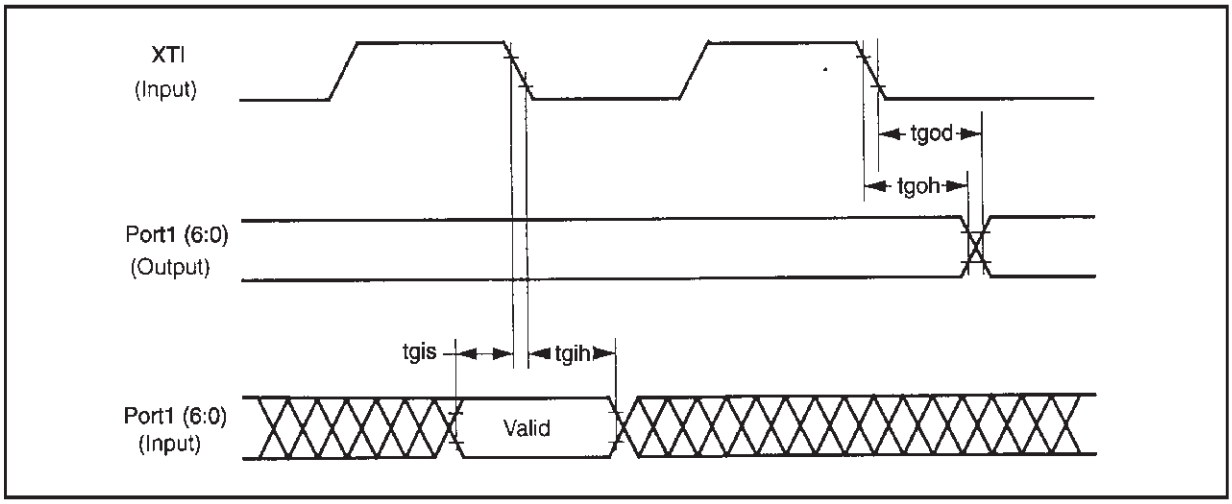
For the calculation of slowest access time allowed for a memory attached to the M8051, the following diagram illustrates the timing constraints. Slowest access time allowed, t_{acc} = 4*mclk - t_{ad} - t_{ds}, where the worst case address delay, t_{ad} = 30 ns, and the worst case data setup time, t_{ds} = 20 ns.



GENERAL PURPOSE I/O (GPIO) INTERFACE

Timing	Characteristics	mclk = 20MHz		Unit
		Min.	Max.	
t_{god}	XTI Edge to GPIO Out Valid (GPIO Out Delay Time)	--	26	ns
t_{goh}	XTI Edge to GPIO Out Not Valid (GPIO Out Hold Time)	2	--	ns
t_{gis}	GPIO In Valid to XTI Edge (GPIO In Set-up Time)	10	--	ns
t_{gih}	XTI Edge to GPIO In Not Valid (GPIO In Hold Time)	6	--	ns

Figure 10. GPIO Timing



Debug Port Interface

No.	Characteristics	dclk = 40MHz		Unit
		Min.	Max.	
1	DBCK rise time	--	3	ns
2	DBCK fall time	--	3	ns
3	DBCK Low	40	--	ns
4	DBCK High	40	--	ns
5	DBCK Cycle Time	200	--	ns
6	$\overline{\text{DBRQN}}$ Asserted to DBOUT ($\overline{\text{ACK}}$) Asserted	5 T_{DSP}	--	ns
7	DBCK High to DBOUT Valid	--	42	ns
8	DBCK High to DBOUT Invalid	3	--	ns
9	DBIN Valid to DBCK Low (Set-up)	15	--	ns
10	DBCK Low to DBIN Invalid (Hold)	3	--	ns
	DBOUT ($\overline{\text{ACK}}$) Asserted to First DBCK High	2 Tc	--	ns
	DBOUT ($\overline{\text{ACK}}$) Assertion Width	4.5 T_{DSP} - 3	5 T_{DSP} + 7	ns
11	Last DBCK Low of Read Register to First DBCK High of Next Command	7 T_{DSP} + 10	--	ns
12	Last DBCK Low to DBOUT Invalid (Hold)	3	--	ns
	DBSEL setup to DBCK	T_{DSP}		ns

Figure 11. Debug Port Serial Clock Timing.

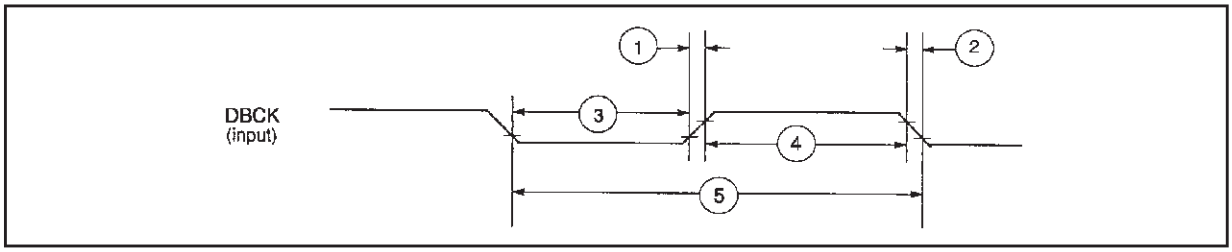


Figure 12. Debug Port Acknowledge Timing.

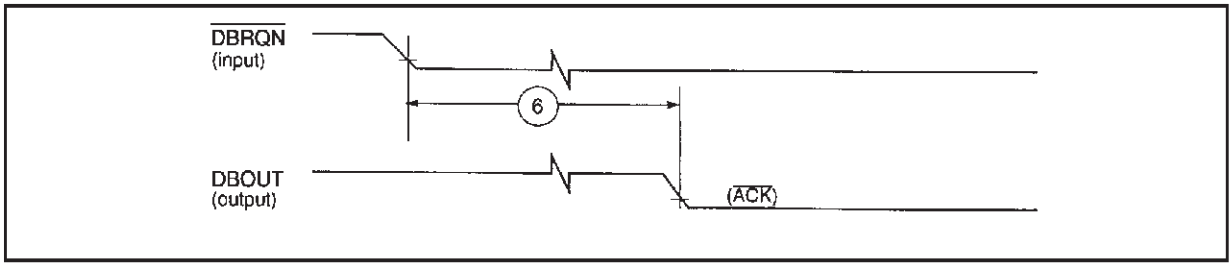


Figure 13. Debug Port Data I/O to Status Timing.

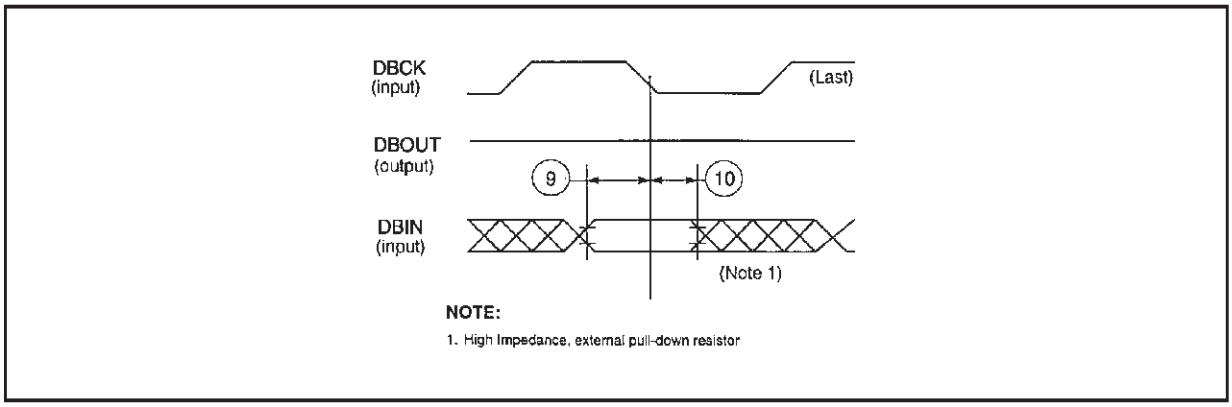


Figure 14. Debug Port Read Timing.

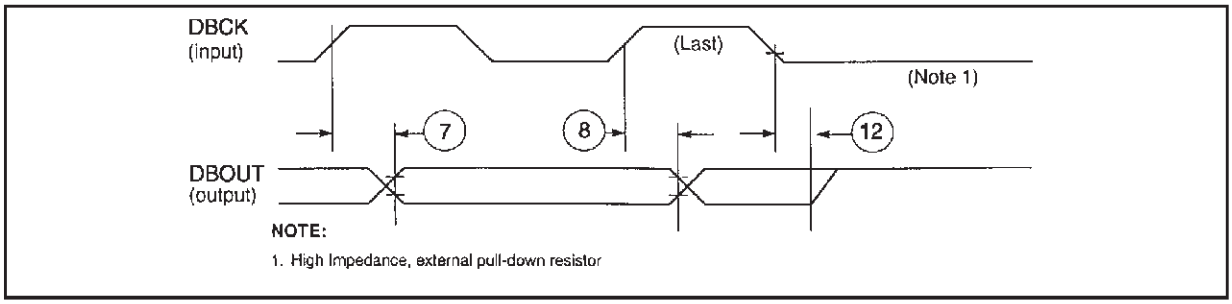
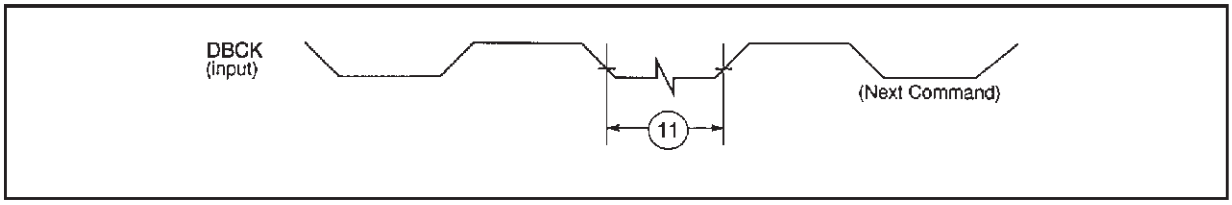


Figure 15. Debug Port DBCK Next Command After Read Register Timing.



EXTERNAL MEMORY INTERFACE (EMI) DRAM MODE

Characteristics	Timing Mode	40MHz		Unit
		Min.	Max.	
Page Mode Cycle Time	slow fast	100 75	-- --	ns ns
$\overline{RAS}$ or $\overline{RD}$ Assertion to Data Valid	slow fast	-- --	159 109	ns ns
$\overline{CAS}$ Assertion to Data Valid	slow fast	-- --	65 40	ns ns
Column Address Valid to Data Valid	slow fast	-- --	80 55	ns ns
$\overline{CAS}$ Assertion to Data Active		0	--	ns
$\overline{RAS}$ Assertion Pulse Width (Note 1) (Page Mode Access Only)	slow fast	264 189	-- --	ns ns
$\overline{RAS}$ Assertion Pulse Width (Single Access Only)	slow fast	164 114	-- --	ns ns
$\overline{RAS}$ or $\overline{CAS}$ Negation to $\overline{RAS}$ Assertion	slow fast	120 70	-- --	ns ns
$\overline{CAS}$ Assertion Pulse Width	slow fast	65 40	-- --	ns ns
Last $\overline{CAS}$ Assertion to $\overline{RAS}$ Negation (Page Mode Access Only)	slow fast	60 35	-- --	ns ns

Note: 1. n is the number of successive accesses. n = 2, 3, 4, or 6.

DRAM Refresh Timing

Characteristics	Timing Mode	40MHz		Unit
		Min.	Max.	
$\overline{RAS}$ Negation to $\overline{RAS}$ Assertion	slow fast	143 93	-- --	ns ns
$\overline{CAS}$ Negation to $\overline{CAS}$ Assertion	slow fast	118 68	-- --	ns ns
Refresh Cycle Time	slow fast	325 225	-- --	ns ns
$\overline{RAS}$ Assertion Pulse Width	slow fast	166 116	-- --	ns ns
$\overline{RAS}$ Negation to $\overline{RAS}$ Assertion for Refresh Cycle (Note 1)	slow fast	120 70	-- --	ns ns
$\overline{CAS}$ Assertion to $\overline{RAS}$ Assertion on Refresh Cycle		18	--	ns
$\overline{RAS}$ Assertion to $\overline{CAS}$ Negation on Refresh Cycle	slow fast	160 110	-- --	ns ns
$\overline{RAS}$ Negation to $\overline{CAS}$ Assertion on a Refresh Cycle	slow fast	114 64	-- --	ns ns
$\overline{CAS}$ Negation to Data Not Valid		0	--	ns

Note: 1. Happens when a Refresh Cycle is followed by an Access Cycle.

EXTERNAL MEMORY INTERFACE (EMI) SRAM MODE

Characteristics	40MHz		Unit
	Min.	Max.	
Address Valid and $\overline{CS}$ Assertion Pulse Width	89	--	ns
Address Valid to $\overline{RD}$ or $\overline{WR}$ Assertion	23	--	ns
$\overline{RD}$ or $\overline{WR}$ Assertion Pulse Width	45	--	ns
$\overline{RD}$ or $\overline{WR}$ Negation to $\overline{RD}$ or $\overline{WR}$ Assertion	39	--	ns
$\overline{RD}$ or $\overline{WR}$ Negation to Address not Valid	5	--	ns
Address Valid to Input Data Valid	--	72	ns
$\overline{RD}$ Assertion to Input Data Valid	--	35	ns
$\overline{RD}$ Negation to Data Not Valid (Data Hold Time)	0	--	ns
Address Valid to $\overline{WR}$ Negation	73	--	ns
Data Setup Time to $\overline{WR}$ Negation	32	--	ns
Data Hold Time from $\overline{WR}$ Negation	5	--	ns
$\overline{WR}$ Assertion to Data Valid	--	18	ns
$\overline{WR}$ Negation to Data High-Z (Note 1)	--	23	ns
$\overline{WR}$ Assertion to Data Active	5	--	ns

Figure 16. External Memory Interface SRAM Read Cycle.

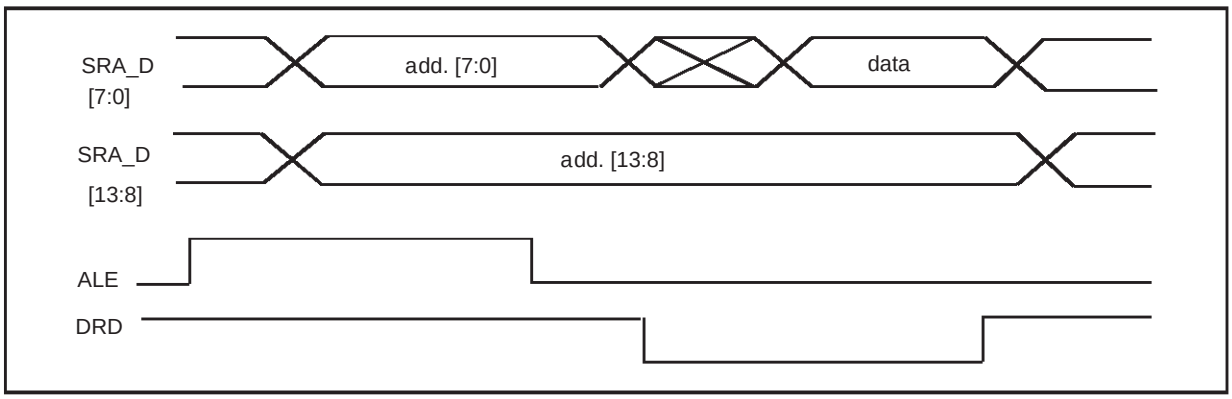


Figure 17. External Memory Interface SRAM Write Cycle.

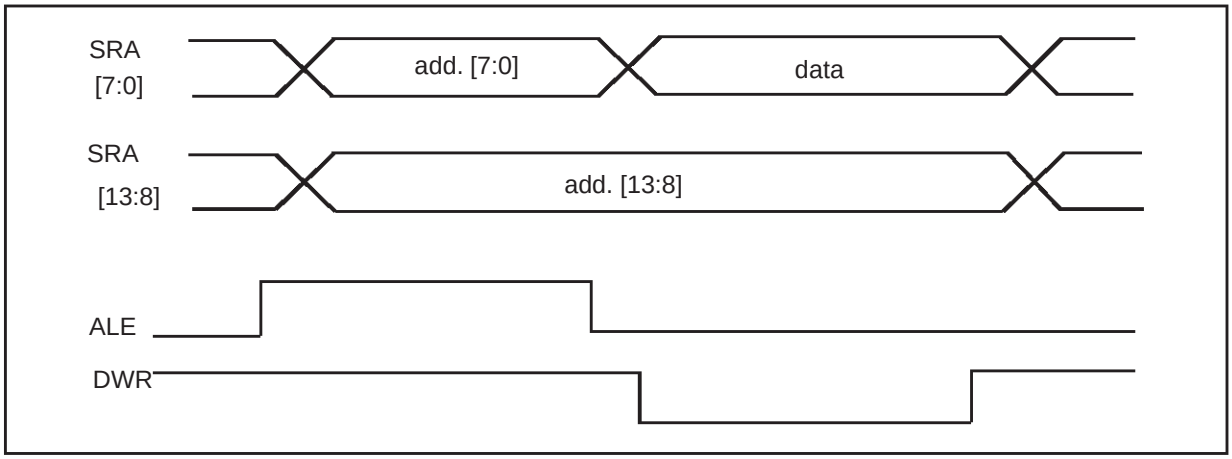


Figure 18. DRAM Read Cycle.

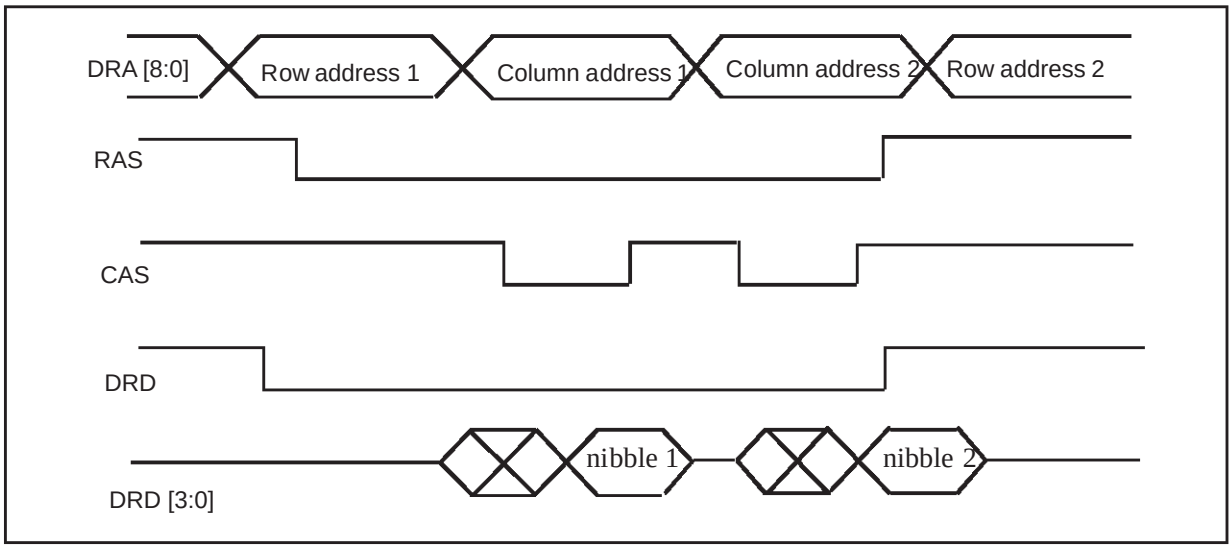
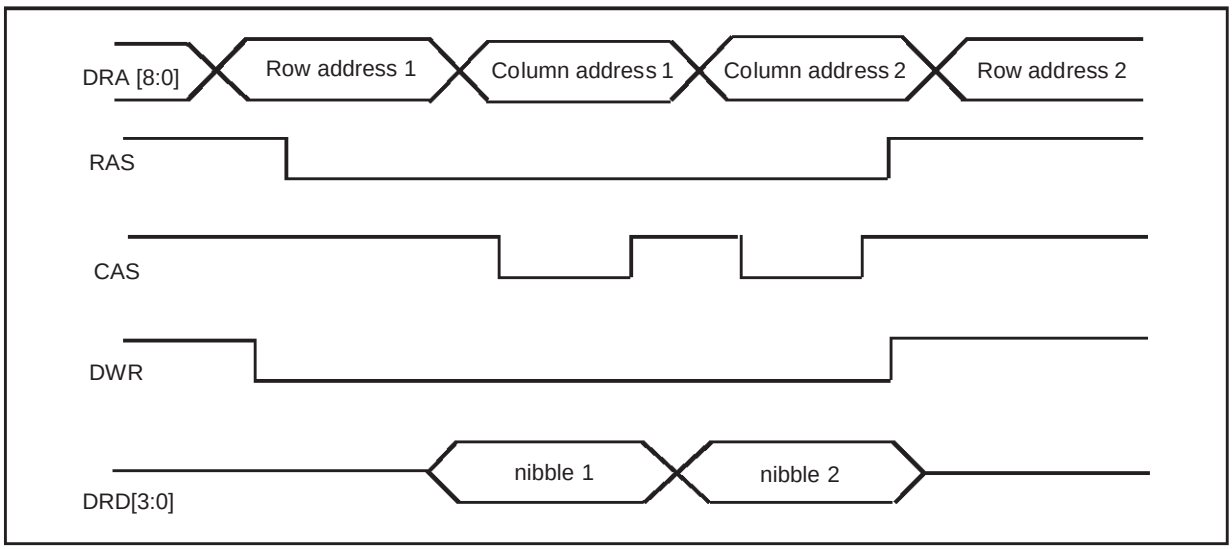


Figure 19. DRAM Write Cycle.



FUNCTIONAL DESCRIPTION.

The Aladdin IC broken up into two distinct blocks. One block contains the two DSP Cores and their associated peripherals. The other contains the M8051 Core and its associated peripherals. The interface between the two blocks is the Host Interface.

24-BIT DSP CORE.

The two DSP cores are used to process the converted analog audio data coming from the CODEC chip via the SAI and return it for analog conversion. Functions such as volume, tone, balance, and fader control, as well as spatial enhancement and general purpose signal processing may be performed by the DSPs.

Some capabilities of the DSPs are listed below:

- Single cycle multiply and accumulate with convergent rounding and condition code generation
- 2 x 56-bit Accumulators
- Double precision multiply
- Scaling and saturation arithmetic
- 48-bit or 2 x 24-bit parallel moves
- 64 interrupt vector locations
- Fast or long interrupts possible
- Programmable interrupt priorities and masking
- 8 each of Address Registers, Address Offset Registers and Address Modulo Registers
- Linear, Reverse Carry, Multiple Buffer Modulo, Multiple Wrap-around Modulo address arithmetic
- Post-increment or decrement by 1 or by offset, Index by offset, predecrement address
- Repeat instruction and zero overhead DO loops
- Hardware stack capable of nesting combinations of 7 DO loops or 15 interrupts/subroutines
- Bit manipulation instructions possible on all registers and memory locations. Also Jump on bit test.
- 4 pin serial debug interface
- Debug ccess to all internal registers, buses and memory locations
- 5 word deep program address history FIFO
- Hardware and software breakpoints for both program and data memory accesses
- Debug Single stepping, Instruction injection and Disassembly of program memory

DSP PERIPHERALS

There are a number of peripherals that are tightly coupled to the two DSP Cores. Except for the memories and the Host Interface, a single peripheral is multiplexed to both of the DSP Cores. In the case of the Host Interface(HI), for DSP to Micro communication, there are two identical peripheral blocks providing the same function to both DSP Cores. Each of the peripherals are listed below and described in the following sections.

- 256 x 24-Bit X-RAM.
- 256 x 24-Bit Y-RAM.
- 768 x 24-Bit Program RAM (1280 x 24 for DSP1)
- 256 x 24-Bit Data X-ROM.
- 256 x 24-Bit Data Y-ROM.

- 64 x 24-Bit Boot ROM.
- Serial Audio Interface (SAI) multiplexed to both DSPs.
- Synchronous Serial Interface (SSI) multiplexed to both DSPs.
- XCHG Interface for DSP to DSP communication.
- Host Interface (HI) for DSP to Micro communication.
- External Memory Interface (DRAM/SRAM) multiplexed to both DSPs for time-delay.
- Single Debug Port multiplexed to both DSPs.
- Cordic Arithmetic Unit

DATA AND PROGRAM MEMORY

Both DSP0 and DSP1 have an identical set of Data and Program memories attached them. Each of the memories are described below and it is implied that there are two of each type, one set connected to DSP0 and the other to DSP1. The only exception is the case of the P-RAM where DSP0 has a 768 x 24-Bit PRAM and DSP1 has a 1280 x 24-Bit PRAM.

256 x 24-Bit X-RAM (XRAM)

This is a 256 x 24-Bit Single Port SRAM used for storing coefficients. The 16-Bit XRAM address, XABx(15:0) is generated by the Address Generation Unit of the DSP core. The 24-Bit XRAM Data, XDBx(23:0), may be written to and read from the Data ALU of the DSP core. The XDBx Bus is also connected to the Internal Bus Switch so that it can be routed to and from all peripheral blocks.

256 x 24 Bit Y-RAM (YRAM)

This is a 256 x 24-Bit Single Port SRAM used for storing coefficients. The 16-Bit address, YABx(15:0) is generated by the Address Generation Unit of the DSP core. The 24-Bit Data, YDBx(23:0), is written to and read from the Data ALU of the DSP core. The YDBx Bus is also connected to the Internal Bus Switch so that it can be routed to and from other blocks.

768 x 24-Bit Program RAM (PRAM 1280 x 24-bit for DSP1)

This is a 768 x 24-Bit Single Port SRAM used for storing and executing program code. The 16-Bit PRAM Address, PABx(15:0) is generated by the Program Address Generator of the DSP core for Instruction Fetching, and by the AGU in the case of the Move Program Memory (MOVEM) Instruction. The 24-Bit PRAM Data (Program Code), PDBx(23:0), can only be written to using the MOVEM instruction. During instruction fetching the PDBx Bus is routed to the Program Decode Controller of the DSP core for instruction decoding.

256 x 24-Bit X-ROM (XROM)

This is a 256 x 24-Bit factory programmed X-ROM. The 16-Bit address, XABx(15:0) is generated by the AGU Unit. The 24-Bit Data is multiplexed onto the XDBx Bus when the address is valid.

256 x 24-Bit Y-ROM (YROM)

This is a 256 x 24-Bit factory programmed Y-ROM. The 16-Bit address, YABx(15:0) is generated by the AGU Unit. The 24-Bit Data is multiplexed onto the YDBx Bus when the address is valid.

128 x 24-Bit Bootstrap ROM (PROM)

This is a 128 x 24-Bit factory programmed Boot ROM used for storing the program sequence for initializing the DSP. Essentially this consists of a routine that is called when the M8051 requests that a DSP image be sent via the Host Interface. It is the task of the Boot code to read the data being sent by the micro from the Host Interface FIFO and store it in PRAM, XRAM, YRAM, and/or external DRAM.

Operating Mode Register

The operating mode register contains one bit to choose between boot mode (always from the Host Interface) or normal mode (execution from PRAM). This bit will be set when the DSP is reset (by writing to the RSDSPx bit in the CLKCNTL register). It must be cleared by the boot code to enable execution from PRAM.

DSP Memory Maps

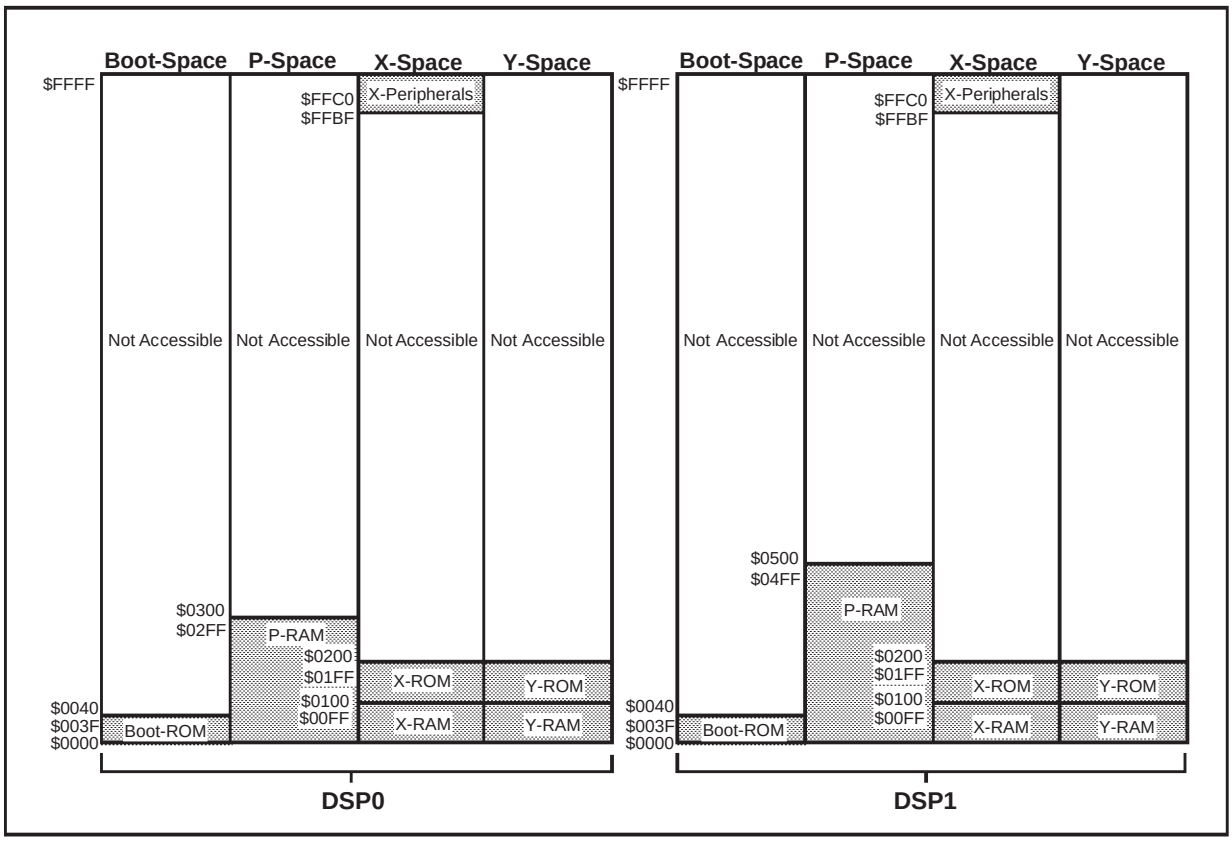
The DSP memory Maps are shown in Figure 26.

Serial Audio Interface (SAI)

The SAI is used to deliver digital audio to the DSPs from an external source. Once processed by the DSPs, it can be returned through this interface. There is only one SAI on the chip that can be accessed by either DSP. The features of the SAI are listed below.

- Five Synchronized Stereo Data Transmission Lines
- Four Synchronized Stereo Data Reception Lines
- Slave operating mode, all clock lines are inputs

Figure 20. DSP1 and DSP0 Memory Spaces.



- Transmit and Receive Interrupt Logic triggers on Left/Right data pairs
- Receive and Transmit Data Registers have two locations to hold left and right data.

Synchronous Serial Interface (SSI)

The SSI is used for communication with devices with a conventional serial interface (not I2S stereo serial audio interface). The SSI shares some pins with the SAI. When the SSI is activated, some of the SAI pins are switched from the SAI to the SSI. The SAI and SSI can operate in parallel.

The features of the SSI are listed below.

- Slave operating mode, FSYNC and SSISCK are inputs.
- Data sizes of 8, 16, and 24 bits are supported.
- Frame Sync (FSYNC) and SCK (SSISCK) signals connected to both the receiver and transmitter.
- Normal mode or Network mode possible.

XCHG Interface (DSP to DSP Exchange Interface)

The Exchange Interface peripheral provides bidirectional communication between DSP0 and DSP1. Both 24 bit word data and four bit Flag data can be exchanged. A FIFO is utilized for received data. It minimizes the number of times an Exchange Interrupt Service Routine would have to be called if multi-word blocks of data were to be received. The Transmit FIFO is in effect the Receive FIFO of the other DSP and is written directly by the transmitting DSP. The features of the XCHG are listed below.

- 10 Word XCHG Receive FIFO on both DSPs
- Four Flags for each XCHG for DSP to DSP signaling
- Condition flags can optionally trigger interrupts on both DSPs

Host Interface(HI)

The DSPs communicate with the 8051 through the Host Interface. There is a separate HI for each of the DSPs. Two Host Interfaces are included. HI0 for Host to DSP0 communication, and HI1 for Host to DSP1 communication. The

features of the HI are listed below.
- 8 Word Host Receive FIFO - DSP Side
- 4 Word Host Receive FIFO - Host (8051) Side
- Two Flags for each HI for DSP to Host signaling (can optionally trigger interrupts)
- Command Vector Register allows Host to trigger any DSP vectored interrupt

DRAM/SRAM Interface (EMI)

The External DRAM/SRAM Interface is viewed as a memory mapped peripheral. Data transfers are performed by moving data into/from data registers and the control is exercised by polling status flags in the control/status register or by servicing interrupts. An external memory write is executed by writing data into the EMI Data Write Register. An external memory read operation is executed by either writing to the offset register or reading the EMI Data Read Register, depending on the configuration.

The features of the EMI are listed below.
- Data bus width fixed at 4 bits for DRAM and 8 bits for SRAM.
- Data word length choices of 16 or 24 bits.
- Nine DRAM address lines means 218 = 256KB addressable DRAM.
- Refresh rate for DRAM can be chosen among eight divider factor.
- SRAM relative addressing mode with multiplexed address/data lines; 214= 16KB addressable SRAM.
- Four SRAM Timing choices.
- Two Read Offset Registers.

Debug Interface

The Debug Port is multiplexed to both of the DSP Cores via a select pin. Only one DSP can be debugged at a time. The debug logic is contained in the core design of the DSP. The features of the Debug Port are listed below:
- Breakpoint Logic
- Trace Logic
- Single stepping
- Instruction Injection
- Program Disassembly

CORDIC Co-Processor

The CORDIC Co-Processor is used to convert rectangular to polar coordinates. .

The CORDIC Unit has an 18 Bit data path throughout. When reading 24 bit words from the DSP the upper 6 bits are truncated. When writing to the DSP the upper 6 bits are zeroed.

Either DSP may write an X and Y coordinate to the CORDIC unit and, 17 clock cycles later, the magnitude and angle information will be available from the CORDIC Unit.

8051 Embedded Microcontroller

The microcontroller serves as the on-chip system controller and operates from 64K of external EPROM with 1K of internal RAM. In addition, it contains a small program in internal RAM that allows the micro to program the external EPROM. The micro will boot a network interface program from external EPROM. If a command to program the EPROM is received from the network then the following sequence will be initiated: The micro will read a ROM image from the network via a network chip attached to the micro's SPI. Then the micro will switch to running out of internal RAM and begin programming the external EPROM with the image read from the network. This allows the personality of the system to be set after the system has been manufactured. The external EPROM also holds the DSP programs and initializing values. The micro will copy these images to the DSP via an on-chip host interface (HI).

In addition to the 8051 Core the following memory and control functions are required:
- Internal Memory Interface to 256 Bytes of Single Port Static RAM and 768 Bytes of AUX-RAM
- External Memory Interface to EPROM and Memory Mapped Peripheral I/O
- Host Interface for Micro to DSP Communication
- Serial Peripheral Interface (SPI)
- Control Interface for Interrupts and GPIO
- PLL Clock Oscillator

Internal Memory Interface

The 8051 requires an internal memory interface to connect to the internal 256 RAM locations and the 768 Auxiliary RAM.

Micro Memory Interface

The 8051 core requires an external memory interface to connect to external program memory and memory mapped peripherals. This is implemented like the standard 80C51 Port 2/Port 0 Multiplexed 16 Bit Address/8 Bit Data Bus. . The signals RD, WR, XPSEN, and XALE will also be output. The External Memory Interface must also have circuitry to program the external EPROM (or any non-volatile memory) in-circuit. This means that the normal operation of the external memory interface must be altered to handle the program timing of the EPROM. By treating the Port 2/Port 0 pins as GPIO the programming can be

achieved in software. When this mode is entered instruction execution is switched to internal AUX-RAM.

Serial Peripheral Interface

The 8051 core requires a serial interface to receive commands and data over the LAN. During an SPI transfer, data is transmitted and received simultaneously. A serial clock line synchronizes shifting and sampling of the information on the two serial data lines. A slave select line allows individual selection of a slave SPI device. The SS Pin will act as a GPIO when the SPI is in master mode or the SPI is disabled.

When an SPI transfer occurs an 8-bit word is shifted out one data pin while another 8-bit character is simultaneously shifted in a second data pin. The central element in the SPI system is the shift register and the read data buffer. The system is single buffered in the transfer direction and double buffered in the receive direction.

Control Interface

The 8051 requires a set of external general purpose input/output lines, two external interrupt lines, and a reset line. These signals are used by external devices to signal events to the 8051. The GPIO lines are implemented as the 8051's Port 1 GPIO. The two external interrupts are connected to the INT0 and INT1 lines on the micro. The RESET pin is used to reset the micro.

PLL Clock Oscillator

The PLL Clock Oscillator can accept an external clock at XTI or it can be configured to run an internal oscillator when a crystal is connected across pins XTI & XTO. There is an input divide block IDF (1 -> 32) at the XTI clock input and a multiply block MF (33 -> 128) in the PLL loop. Hence the PLL can multiply the external input clock by a ratio MF/IDF to generate the internal clock. This allows the internal clock to be within 1 MHz of any desired frequency even when XTI is much greater than 1 MHz. It is recommended that the input clock is not divided down to less than 1 MHz as this reduces the Phase Detector's update rate.

The clocks to the DSP and the 8051 can be selected to be either the VCO output divided by 2 or 4 respectively, or be driven by the XTI pin directly.

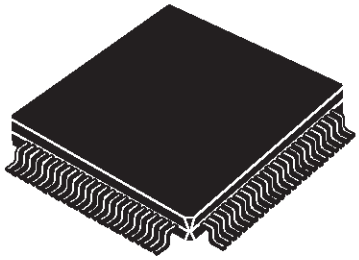
The crystal oscillator and the PLL will be gated off when entering the power-down mode (by setting bit 1 of the PCON Register).

M8051 Interrupts

The M8051 Core provides for 5 interrupt sources, INT1, INT0, TIMER1, TIMER0, and SERIAL Data. There exists a corresponding Interrupt Enable register and Interrupt Priority Register.

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.17	0.22	0.27	0.007	0.009	0.011
C	0.09		0.20	0.003		0.008
D		16.00			0.630	
D1		14.00			0.551	
D3		12.00			0.472	
e		0.50			0.019	
E		16.00			0.630	
E1		14.00			0.551	
E3		12.00			0.472	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.0393	
K	3.5°(min.), 7°(max.)					

OUTLINE AND MECHANICAL DATA



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