

VR4121 64-BIT MIPS RISC MICROPROCESSOR

FOR WINDOWS CE

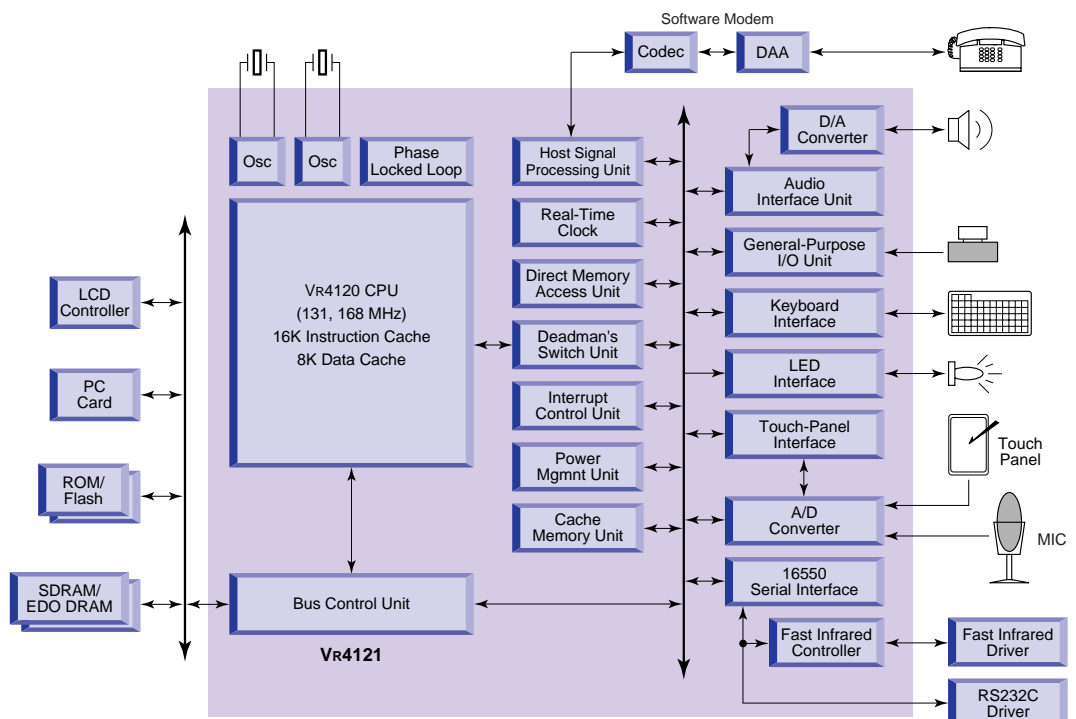
The 64-bit VR4121™ (μPD30121) microprocessor is a member of NEC's VR Series™ devices created for Windows® CE embedded consumer applications. Designed around the MIPS® RISC architecture developed by MIPS Technologies, the VR4121 offers excellent power consumption and performance in a highly integrated, low-cost system on a chip.

This microprocessor is the second NEC device to use the ultra-low-power-consuming VR4120™ CPU core based on advanced 0.25-micron technology. The VR4120 CPU has an optimized five-stage pipeline, 16-KB instruction cache, 8-KB data cache, multiply-accumulate (MAC) unit, and memory management unit that enable high performance in a compact, low-cost chip. Integrated peripherals include a power management unit, direct memory access unit, interrupt control unit, timers, real-time clock, 16550-compatible serial interface, IrDA® interface, keyboard interface, touch-panel interface, host signal processing unit (software modem), and A/D and D/A converters.

The VR4121 is compatible with MIPS III instruction set architecture (ISA) and MIPS16 application-specific extension (ASE). The MIPS16 ASE compatibility enables the VR4121 to incorporate 16-bit-long instructions with conventional 32-bit-long instructions, resulting in compact code size, a smaller memory requirement, and lower system cost.

The VR4121 provides an easy choice for VR4111™ customers in terms of upgrade, since the VR4121 and VR4111 are fully pin compatible. The VR4121 microprocessor's high speed, compact size, and low power consumption make it ideal for use in a battery-driven, portable handheld systems.

BLOCK DIAGRAM



FEATURES

VR4120 CPU CORE

- MIPS III ISA-compliant
- MIPS 16 ASE-compliant for compact code density (40% denser code than MIPS32)
- Five-stage pipeline running up to 168 MHz
- Single-cycle 32-bit MAC instruction for digital signal processing operations

MEMORY MANAGEMENT UNIT

- 32-bit physical address range of 4 GB with 40-bit virtual address space
- 32 double-entry TLBs supporting 1~256 KB page sizes
- Up to 64 MB of SDRAM/EDO/fast-page DRAM and 64 MB of SROM/flash memory/mask ROM
- Up to 66-MHz operation

CACHE MEMORY UNIT

- 16-KB direct-mapped instruction cache
- 8-KB direct-mapped data cache
- Write-back cache for reducing store operations

BUS CONTROL UNIT

- 32-bit and 16-bit addressing
- Dynamic bus sizing; subset of ISA bus

POWER MANAGEMENT UNIT WITH FOUR POWER-SAVING MODES

- Full speed
- Standby
- Suspend
- Hibernate

CLOCK GENERATOR UNIT

- Built-in PPL for frequency multiplication
- External bus frequency of 16/33 MHz

SERIAL INTERFACE UNIT

- 16550-compatible
- RS-232C compliant
- Up to 115 kbps
- Separate debugging serial port

OTHER PERIPHERALS

- Real-time clock with four built-in timers
- Interrupt control unit with internal and external interrupts
- DMA address unit and DMA control unit with five different channels
- General-purpose I/O unit with 49 general-purpose I/O pins
- 96-key keyboard and touch-panel interface
- 10-bit A/D converter for touch-panel and audio input
- Fast IR unit: 0.5 to 4 Mbps IrDA 1.1 standard communication
- Audio interface unit and 10-bit D/A converter for audio output
- Host signal processing unit with glueless interface to telecom codec for software modem implementation

AC/DC SPECIFICATIONS

- 131 and 168 MHz maximum frequency
- 2.5- and 3.3-volt operation
- 131 MHz at 300-mW typical power consumption (target specification)
- 168 MHz at 385-mW typical power consumption (target specification)

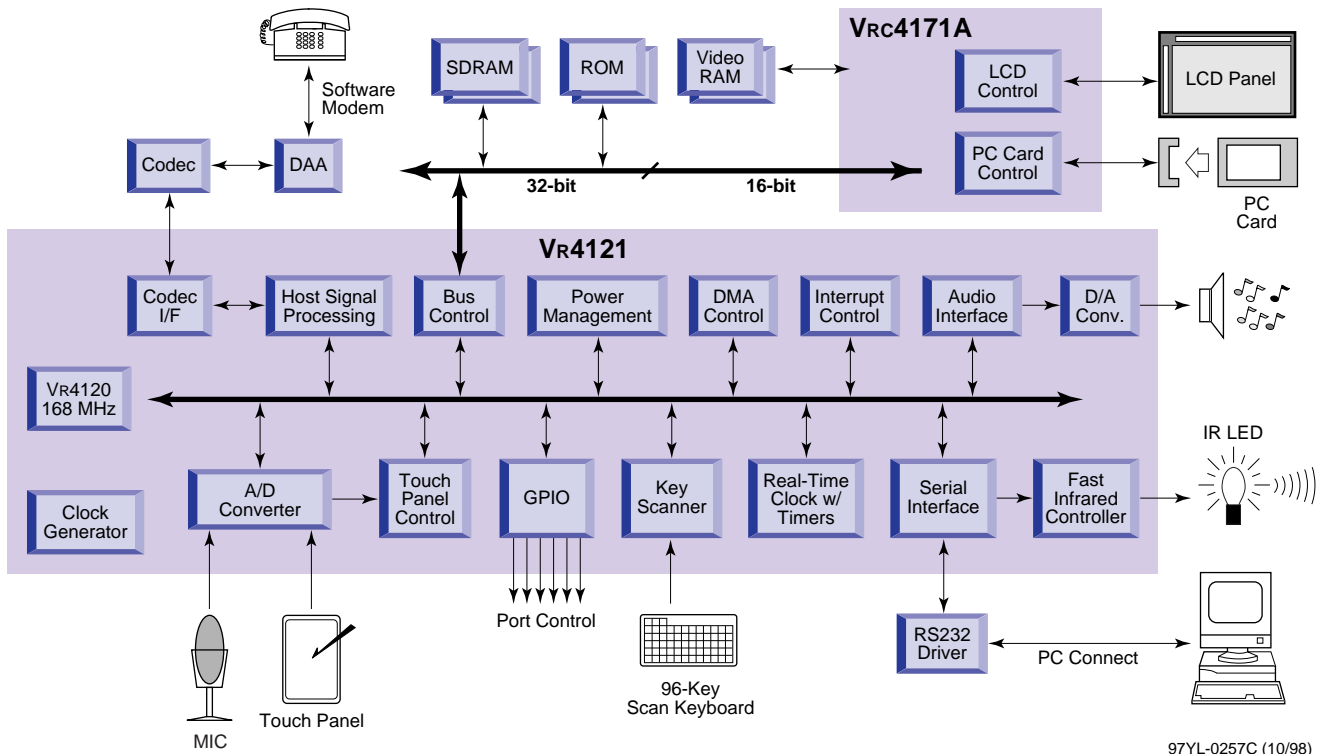
PACKAGE

- Compact size: 16 x 16 x 1.3 mm
- 224-pin FPBGA
- VR4102™ and VR4111 pin compatibility

ORDERING INFORMATION

PART NUMBER	PACKAGE	MAXIMUM OPERATING FREQUENCY
μPD30121S1-131-3C	224-pin FPBGA	131 MHz
μPD30121S1-168-3C	224-pin FPBGA	168 MHz

EXAMPLE HANDHELD PC APPLICATION WITH VRC4171A



VR4102, VR4111, AND VR4121 COMPARISON

	VR4102	VR4111	VR4121
CPU	VR4100	VR4110	VR4120
Max. Pipeline Clock	54 MHz	90 MHz	168 MHz
Cache Size	Instruction: 4KB/Data: 1KB	Instruction: 16KB/Data: 8KB	Instruction: 16KB/Data: 8KB
Performance	60 Dhrystone MIPS	115 Dhrystone MIPS	224 Dhrystone MIPS
Instruction Set	MIPS III	MIPS III, 16	MIPS III, 16
MAC Instruction	16-bit	16-bit	32-bit
Operating Voltage	3.3 V	2.5 V (core); 3.3 V (I/O)	2.5 V (core); 3.3 V (I/O)
Integrated Peripherals	Same	Same	Same
Memory Interface	32 MB DRAM 32 MB ROM	64 MB DRAM 64 MB ROM	64 MB DRAM (SDRAM) 64 MB ROM
Power Consumption	250 mW	200 mW	385 mW
Package	216-pin LQFP 224-pin FPBGA	224-pin FPBGA	224-pin FPBGA
Process Technology	0.35-micron UC1 process	0.25-micron UC2 process	0.25-micron UR2 process



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