100MHZ AGP CLOCK FOR VIA CHIPSET

W83194R-58A

Data Sheet Revision History

	Pages	Dates	Version	Version On Web	Main Contents
1	n.a.			n.a.	All of the versions before 0.50 are for internal use.
2	n.a.	02/Apr	1.0	1.0	Change version and version on web site to 1.0
3					
4					
5					
6					
7					
8					
9					
10					

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.

1.0 GENERAL DESCRIPTION

The W83194R-58A is a Clock Synthesizer for VIA chipset. W83194R-58A provides all clocks required for high-speed RISC or CISC microprocessor such as Intel PentiumII and also provides 16 different frequencies of CPU clocks by software setting. AGP and PCI clocks are externally selectable with smooth transitions. The W83194R-58A provides AGP clocks especially for clone chipset, and makes SDRAM in synchronous frequency with CPU or AGP clocks.

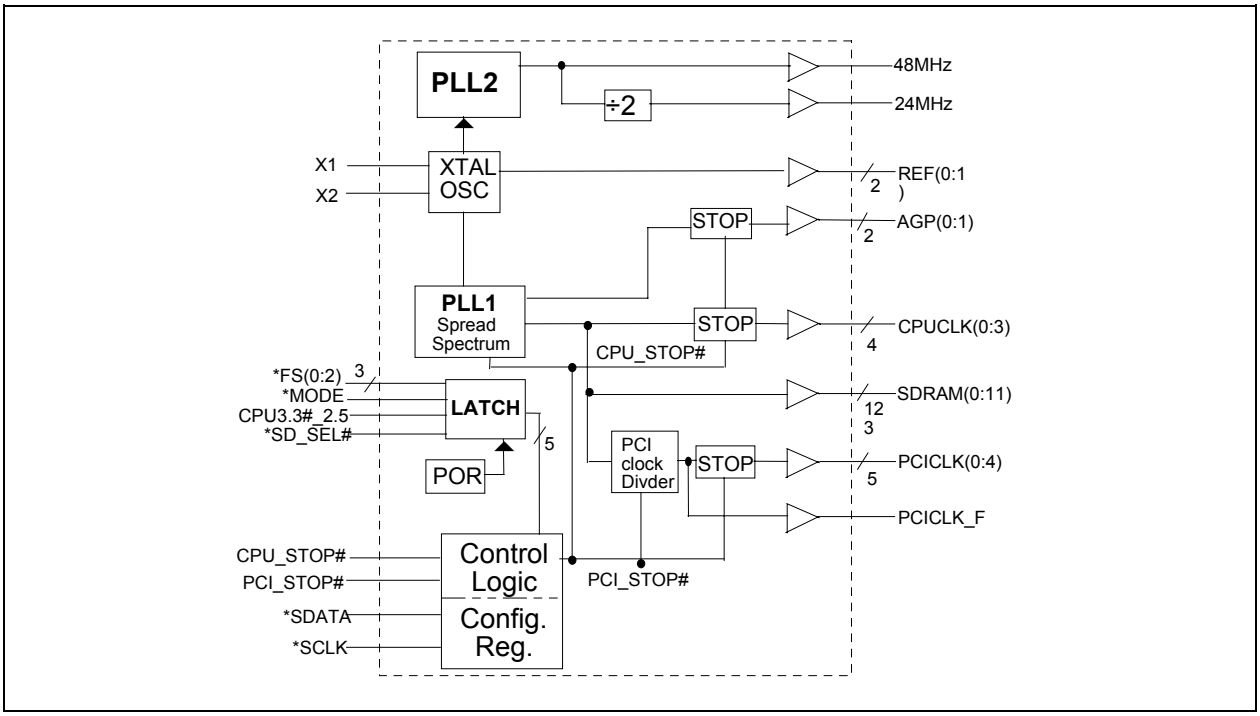
The W83194R-58A provides I^2C serial bus interface to program the registers to enable or disable each clock outputs and choose the 0.25%, 0.5% or 0.5%,1.5% center type spread spectrum to reduce EMI.

The W83194R-58A accepts a 14.318 MHz reference crystal as its input and runs on a 3.3V supply. High drive PCI and SDRAM CLOCK outputs typically provide greater than 1 V /ns slew rate into 30 pF loads. CPU CLOCK outputs typically provide better than 1 V /ns slew rate into 20 pF loads when maintaining 50± 5% duty cycle. The fixed frequency outputs as REF, 24MHz, and 48 MHz provide better than 0.5V /ns slew rate.

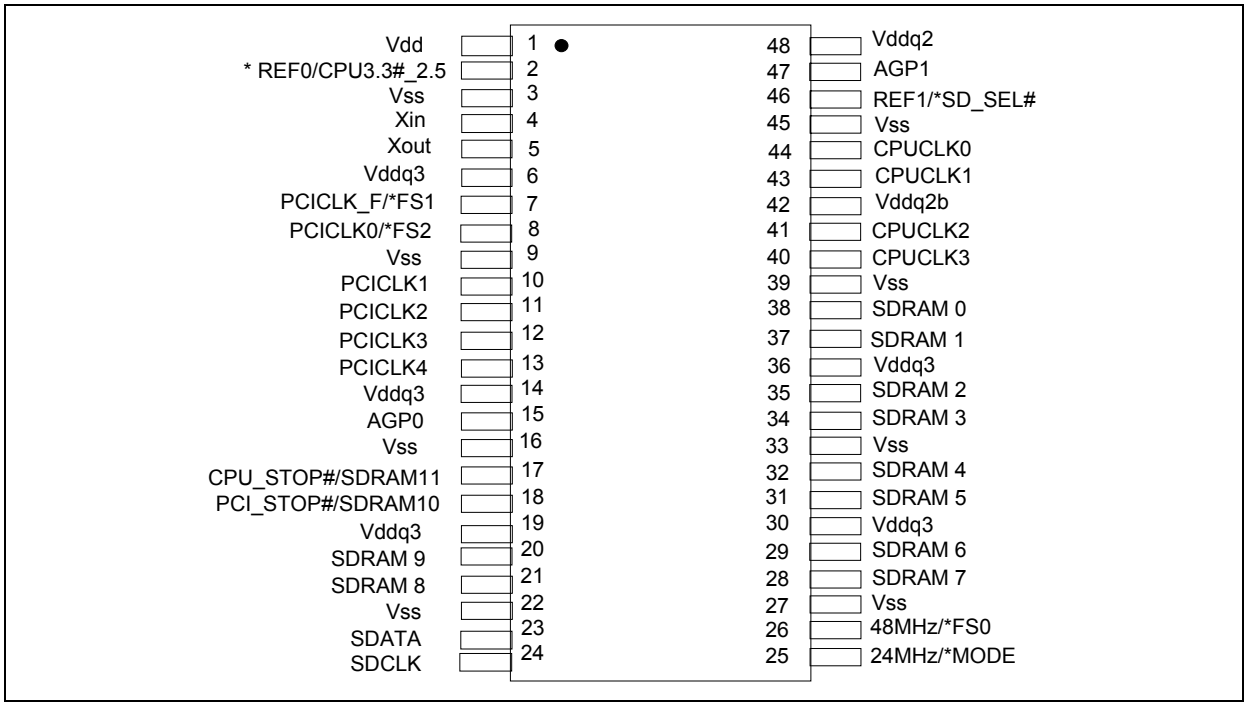
2.0 PRODUCT FEATURES

- Supports Pentium™, Pentium™ Pro, Pentium™ II, AMD and Cyrix CPUs with I^2C.
- 4 CPU clocks
- 12 SDRAM clocks for 3 DIMs
- Two AGP clocks
- 6 PCI synchronous clocks.
- Optional single or mixed supply:
  (Vdd = Vddq3 = Vddq2 = Vddq2b = 3.3V) or (Vdd = Vddq3 = Vddq2 = 3.3V, Vdq2b = 2.5V)
- Skew form CPU to PCI clock -1 to 4 ns, center 2.6 ns, AGP to CPU sync. skew 0 ns (250 ps)
- SDRAM frequency synchronous to CPU or AGP clocks
- Smooth frequency switch with selections from 60 to 100 MHz CPU(-37) and 66 to 150MHz(-58)
- I^2C 2-Wire serial interface and I^2C read back
- 0~0.5% down type and 0.25%, 0.5% center type spread spectrum to reduce EMI
- Programmable registers to enable/stop each output and select modes
  (mode as Tri-state or Normal)
- MODE pin for power Management
- 48 MHz for USB
- 24 MHz for super I/O
- 48-pin SSOP package

3.0 BLOCK DIAGRAM



4.0 PIN CONFIGURATION



5.0 PIN DESCRIPTION

IN - Input

OUT - Output

I/O - Bi-directional Pin

- Active Low

* - Internal 250kΩ pull-up

5.1 Crystal I/O

SYMBOL	PIN	I/O	FUNCTION
Xin	4	IN	Crystal input with internal loading capacitors and feedback resistors.
Xout	5	OUT	Crystal output at 14.318MHz nominally.

5.2 CPU, SDRAM, PCI Clock Outputs

SYMBOL	PIN	I/O	FUNCTION
CPUCLK [0:3]	40,41,43,44	OUT	Low skew (< 250ps) clock outputs for host frequencies such as CPU, Chipset and Cache. Vddq2b is the supply voltage for these outputs.
AGP[0:1]	15,47	OUT	Accelerate Graphic Port clock outputs
SDRAM11/ CPU_STOP#	17	I/O	If MODE =1 (default), then this pin is a SDRAM clock buffered output of the crystal. If MODE = 0 , then this pin is CPU_STOP# input used in power management mode for synchronously stopping the all CPU clocks.
SDRAM10/ PCI_STOP#	18	I/O	If MODE = 1 (default), then this pin is a SDRAM clock output. If MODE = 0 , then this pin is PCI_STOP # and used in power management mode for synchronously stopping the all PCI clocks.
SDRAM [0:9]	20,21,28,29,31 ,32,34, 35,37,38	O	SDRAM clock outputs which have the same frequency as CPU clocks.
PCICLK_F/ *FS1	7	I/O	Latched input for FS1 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks. Free running PCI clock during normal operation.

5.2 CPU, SDRAM, PCI Clock Outputs, continued

SYMBOL	PIN	I/O	FUNCTION
PCICLK 0 / *FS2	8	I/O	Latched input for FS2 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks. PCI clock during normal operation.
PCICLK [1:4]	10,11,12,13	OUT	Low skew (< 250ps) PCI clock outputs.

5.3 I^2C Control Interface

SYMBOL	PIN	I/O	FUNCTION
SDATA	23	I/O	Serial data of I^2C 2-wire control interface
SDCLK	24	IN	Serial clock of I^2C 2-wire control interface

5.4 Fixed Frequency Outputs

SYMBOL	PIN	I/O	FUNCTION
REF0 / CPU3.3#_2.5	2	I/O	Internal 250kΩ pull-up. Latched input for CPU3.3#_2.5 at initial power up. Reference clock during normal operation. Latched high - Vddq2b = 2.5V Latched low - Vddq2b = 3.3V
REF1 /*SD_SEL#	46	I/O	Internal 250kΩ pull-up. Latched input at Power On selects either CPU(SDSEL=1) or AGP(SD_SEL=0) frequencies for SDRAM clock outputs.
24MHz / *MODE	25	I/O	Internal 250kΩ pull-up. Latched input for MODE at initial power up. 24MHz output for super I/O during normal operation.
48MHz / *FS0	26	I/O	Internal 250kΩ pull-up. Latched input for FS0 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks. 48MHz output for USB during normal operation.

5.5 Power Pins

SYMBOL	PIN	FUNCTION
Vdd	1	Power supply for Ref [0:1] crystal and core logic.
Vddq2	42	Power supply for AGP1 and REF1 output, either 2.5V or 3.3V.
Vddq2b	48	Power supply for CPUCLK[0:3], either 2.5V or 3.3V.
Vddq3	6,14,19, 30, 36	Power supply for SDRAM, PCICLK and 48/24MHz outputs.
Vss	3,9,16,22,27, 33,39,45	Circuit Ground.

6.0 FREQUENCY SELECTION BY HARDWARE

6.2 W83194R-58 Frequency Selection Table

FS2	FS1	FS0	CPU(MHz)	SDRAM (MHz)		PCI (MHz)	AGP (MHz)	REF (MHz)
				SD_SEL=1	SD_SEL=0			
0	0	0	112	112	74.7	37.3	74.7	14.318
0	0	1	66.8	66.8	66.8	33.4	66.8	14.318
0	**1**	**0**	**97.0**	**97.0**	**64.67**	**32.33**	**64.67**	**14.318**
0	1	1	75	75	75	37.5	75	14.318
1	0	0	133.3	133.3	88.7	44.3	88.7	14.318
1	0	1	83.3	83.3	66.6	33.3	66.6	14.318
1	1	0	95.25	95.25	63.5	31.75	63.5	14.318
1	1	1	100.2	100.2	66.8	33.4	66.8	14.318

7.0 CPU 3.3#_2.5 BUFFER SELECTION

CPU 3.3#_2.5 (Pin 2) Input Level	CPU Operate at
1	VDD = 2.5V
0	VDD = 3.3V

8.3 SERIAL CONTROL REGISTERS

The Pin column lists the affected pin number and the @PowerUp column gives the state at true power up. Registers are set to the values shown only on true power up. "Command Code" byte and "Byte Count" byte must be sent following the acknowledge of the Address Byte. Although the data (bits) in these two bytes are considered "don't care", they must be sent and will be acknowledge. After that, the below described sequence (Register 0, Register 1, Register 2, ...) will be valid and acknowledged.

8.3.1 Register 0: CPU Frequency Select Register

Bit	@PowerUp	Pin	Description
7	0	-	0 = ±0.25% Spread Spectrum Modulation 1 = ±0.5% Spread Spectrum Modulation(W83194R-58)
6	0	-	SSEL2 (Frequency table selection by software via I^2C)
5	0	-	SSEL1 (Frequency table selection by software via I^2C)
4	0	-	SSEL0 (Frequency table selection by software via I^2C)
3	0	-	0 = Selection by hardware 1 = Selection by software I^2C - Bit 6:4
2	0	-	SSEL3 (Frequency table selection by software via I^2C for W83194R-58)
1	0	-	0 = Normal 1 = Spread Spectrum enabled
0	0	-	0 = Running 1 = Tristate all outputs

W83194R-58 Frequency table selection by software via I^2C

SSEL2	SSEL1	SSEL0	Register0 Bit2	CPU (MHz)	SDRAM (MHz)		PCI (MHz)	AGP (MHz)	REF (MHz)
			SSEL3		SD_SEL=1	SD_SEL=0			
0	0	0	0	112	112	74.7	37.3	74.7	14.318
0	0	1	0	66.8	66.8	66.8	33.4	66.8	14.318
0	**1**	**0**	**0**	**97.0**	**97.0**	**64.67**	**32.33**	**64.67**	**14.318**
0	1	1	0	75	75	75	37.5	75	14.318
1	0	0	0	133.3	133.3	88.7	44..3	88.7	14.318
1	0	1	0	83.3	83.3	66.6	33.3	66.6	14.318
1	1	0	0	95.25	95.25	63.5	31.75	63.5	14.318
1	1	1	0	100.2	100.2	66.8	33.4	66.8	14.318
0	0	0	1	103	103	68.7	34.3	68.7	14.318
0	0	1	1	112	112	74.7	37.3	74.7	14.318
0	1	0	1	115	115	76.6	38.3	76.6	14.318
0	1	1	1	120	120	80	40	80	14.318
1	0	0	1	124	124	82	31	62	14.318
1	0	1	1	133.3	133.3	66.6	33.3	66.6	14.318
1	1	0	1	140	140	70	35	70	14.318
1	1	1	1	150	150	75	37.5	75	14.318

FUNCTION TABLE

Function	Outputs				
Description	CPU	PCI	SDRAM	REF	IOAPIC
Tri-State	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Normal	see table	see table	CPU	14.318	14.318

8.3.2 Register 1 : CPU , 48/24 MHz Clock Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description

7	**1**	**-**	**0 = 0.5% down type spread, overrides Byte0-bit7.** **1= Center type spread.**
6	1	-	Reserved
5	1	-	Reserved
4	1	-	Reserved
3	1	40	CPUCLK3 (Active / Inactive)
2	1	41	CPUCLK2 (Active / Inactive)
1	1	43	CPUCLK1 (Active / Inactive)
0	1	44	CPUCLK0 (Active / Inactive)

8.3.3 Register 2: PCI Clock Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	x	-	Reserved
6	1	7	PCICLK_F (Active / Inactive)
5	1	15	AGP0 (Active / Inactive)
4	1	14	PCICLK4 (Active / Inactive)
3	1	12	PCICLK3 (Active / Inactive)
2	1	11	PCICLK2 (Active / Inactive)
1	1	10	PCICLk1 (Active / Inactive)
0	1	8	PCICLK0 (Active / Inactive)

8.3.4 Register 3: SDRAM Clock Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	28	SDRAM7 (Active / Inactive)
6	1	29	SDRAM6 (Active / Inactive)
5	1	31	SDRAM5 (Active / Inactive)
4	1	32	SDRAM4 (Active / Inactive)
3	1	34	SDRAM3 (Active / Inactive)
2	1	35	SDRAM2 (Active / Inactive)
1	1	37	SDRAM1 (Active / Inactive)
0	1	38	SDRAM0 (Active / Inactive)

8.3.5 Register 4: Additional SDRAM Clock Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	x	-	Reserved
6	x	-	Reserved
5	x	-	Reserved

4	x	-	Reserved
3	1	17	SDRAM11 (Active / Inactive)
2	1	18	SDRAM10 (Active / Inactive)
1	1	20	SDRAM9 (Active / Inactive)
0	1	21	SDRAM8 (Active / Inactive)

8.3.6 Register 5: Peripheral Control (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	x	-	Reserved
6	x	-	Reserved
5	x	-	Reserved
4	1	47	AGP1 (Active / Inactive)
3	x	-	Reserved
2	x	-	Reserved
1	1	46	REF1 (Active / Inactive)
0	1	2	REF0 (Active / Inactive)

8.3.7 Register 6: Reserved Register

Bit	@PowerUp	Pin	Description
7	x	-	Reserved
6	x	-	Reserved
5	x	-	Reserved
4	x	-	Reserved
3	x	-	Reserved
2	x	-	Reserved
1	x	-	Reserved
0	x	-	Reserved