AKD4395
Evaluation board Rev.C for AK4395

General Description

The AKD4395 is an evaluation board for AK4395, which is 192kHz sampling 24Bit ΔΣ DAC. The AKD4395 includes a LPF which can add differential analog outputs from the AK4395 and also has a digital interface with AKM's wave generator using ROM data and AKM's ADC evaluation boards. Therefore, it is easy to evaluate the AK4395.

■ **Ordering Guide**

AKD4395 Rev.C --- Evaluation board Rev.C for AK4395: differential output

Function

■ On-board differential output buffer circuit

■ On-board clock generator

■ BNC connector for an external clock input

■ Compatible with 3types of interface

1. Direct interface with evaluation boards for AKM's A/D converter (AKD539X, AKD535X)
2. Interface with a signal generator (AKD43XX)
3. On-board CS8414 as DIR which accepts optical input.

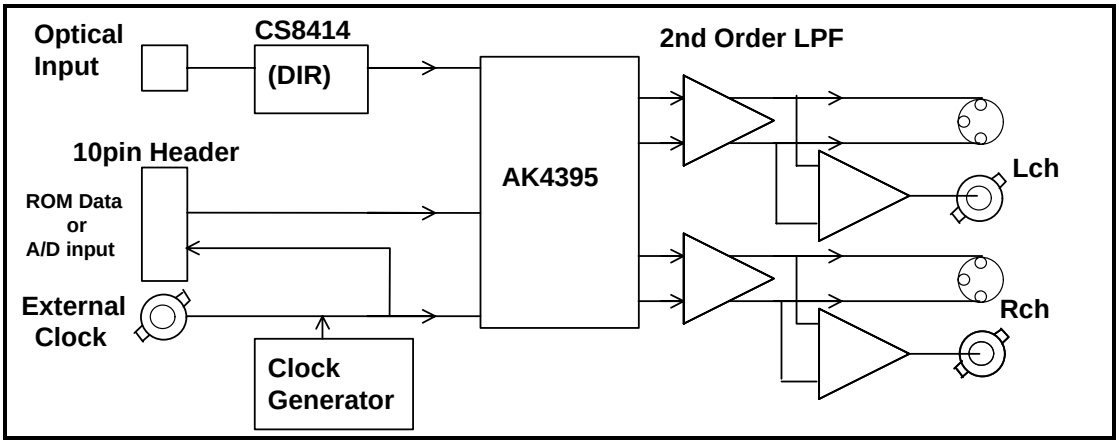


Fig.1 Block diagram

* Circuit diagram and PCB layout are attached at the end of this manual.
(AKD4395 Rev.C is same as AKD4393 Rev.C.)

■ External Analog Circuit (Rev.C)

The differential output circuit and LPF is implemented on board. The differential outputs of AK4395 is buffered by non-inverted circuit and output via Cannon connector(differential output). LPF adds differential outputs. NJM5534D is used for op-amp on this board that has low noise and high voltage torelance characteristics. Analog signal is output via Cannon and BNC connectors on the board. The output level is about 2.73Vrms (typ@VREF=5.0V) by Cannon and 2Vrms (typ@VREF=5.0V) by BNC.

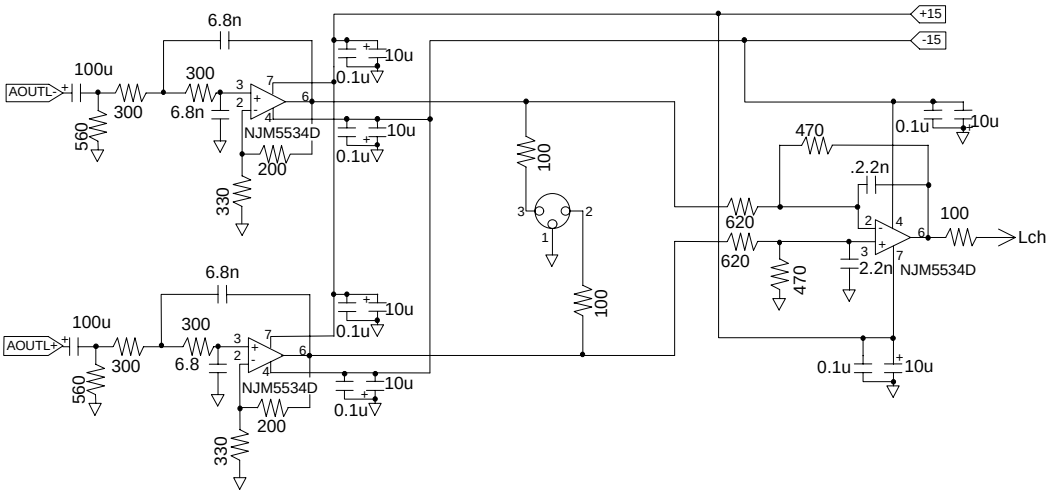


Fig.2 External Analog Filter

■ Operation sequence

1. Set up the jumpers for power supply.

   [JP15(REG)] selects power supply for AVDD pin of AK4395.

   short: 5V is supplied from regulator. (default)
   Nothing should be connected to A5V jack.

   open: 5V is supplied from A5V.

2. Set up the power supply lines.

   +15V=15V, -15V=-15V: Power supply for op-amp. AVDD of AK4395 is supplied from "+15V" through regulator (JP15: short).

   A5V=5V: This jack is used when AVDD of AK4395 is supplied from this. In this case, JP15 should be open.

   DVDD=5V: Power supply for logic circuit on this board.

   VP=3V~5.25V: Digital (set JP10 to VP),

   AGND=DGND=0V .

   Each supply line should be distributed from the power unit.

3. Set up the evaluation modes by jumper pins and DIP switches.(See next item.)

4. Power on.(The AK4395 should be reset once by bringing PD "L" upon power-up.)

   *SW1 resets the AK4395 during operation.

   The AK4395 is reset at SW1="L" and exits resetting at SW1="H".

■ The evaluation modes and corresponding jumper pins setting

1. Evaluation Modes

•Applicable Evaluation Mode

(1) DIR(Optical Link)
(2) Ideal sine wave generated by ROM data
(3) Using AD converted data
(4)All interface signals including master clock are fed externally.

(1) DIR(Optical Link) (default)

PORT2 is used for the evaluation using such as CD test disk. The DIR generates MCLK, BICK and LRCK SDATA from the received data through optical connector(PORT2: TORX176).

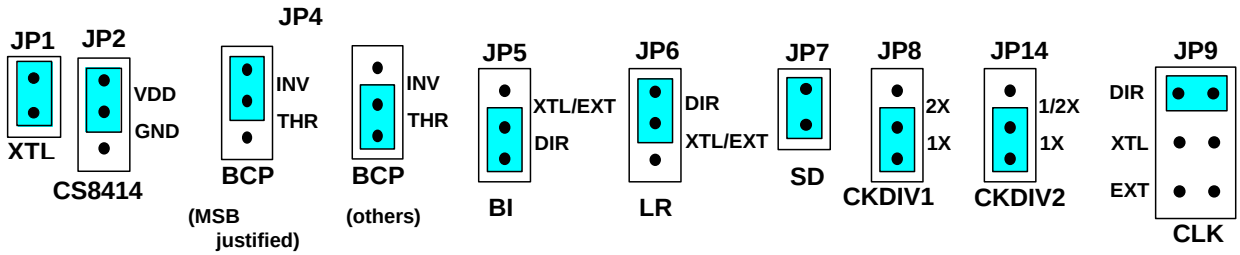


Fig.3 Jumper set-up (DIR)

(2) Ideal sine wave generated by ROM data

Digital signal generated by AKD43XX are used. PORT1 is used for the interface with AKD43XX. Master clock is sent from AKD4395 to AKD43XX then LRCK, BICK and SDATA are sent from AKD43XX to AKD4395.

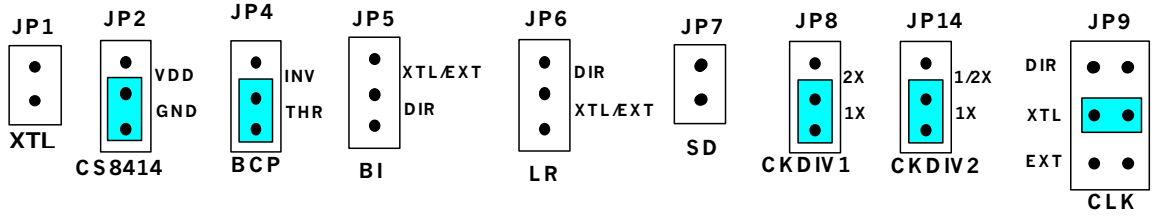


Fig.4 Jumper set-up (ROM data)

(3) Using AD converted data

AD converted data from AKM's AD evaluation boards(AKD539X, AKD535X) is used through PORT1.

* In case of using external clock through a BNC connector, select EXT of JP9 and short JP1.

* In case of using the double speed sampling mode, select 1/2X of JP8 and set S2-2(DFS) on.

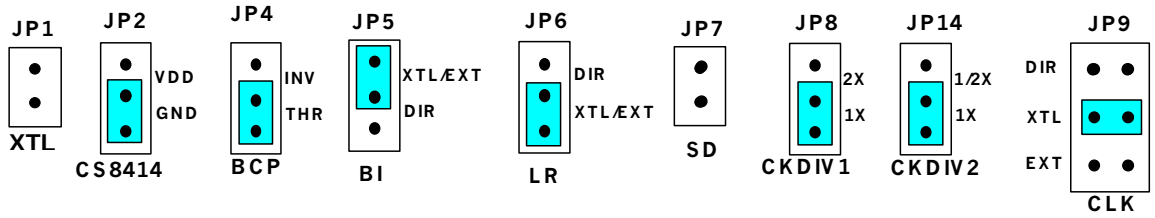


Fig.5 Jumper set-up (A/D)

(4) All interface signals including master clock are fed externally.

Under the following set-up, MCLK, LRCK and SCLK signals needed for the D/A to operate could be fed through PORT1.

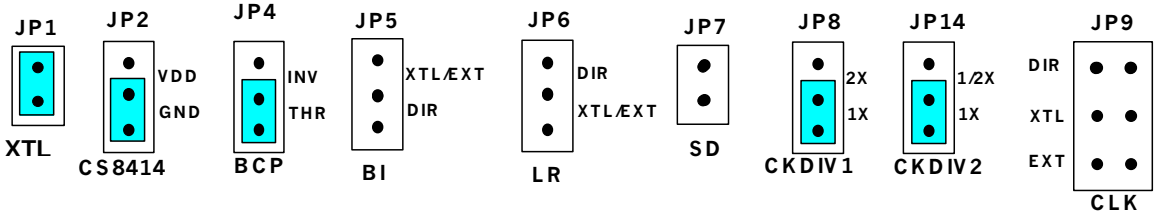


Fig.6 Jumper set-up (ext.)

2. MCLK set-up

When the LRCK is fed from the 74HC4040 on the board, The ratio of MCLK to LRCK can be selected by JP8 and JP14.

JP14	JP8	X'tal	MCLK	fs	MCLK/LRCK
1X	1X	12.288MHz	12.288MHz	48kHz	256
1X	2X	24.576MHz	24.576MHz	48kHz	512
1/2X	1X	24.576MHz	12.288MHz	96kHz	128
1/2X	2X	49.152MHz	12.288MHz	96kHz	128

Table.1 set-up example

3. BICK set-up

When BICK is supplied from U1(74HC4040), either 32fs or 64fs could be selected. Fig.8 shows 64fs mode. 64fs mode is recommended.

*Only mode 0(LSB justified 16bit mode) can correspond to 32fs.

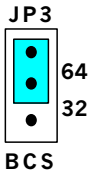


Fig.7 Jumper Set-up (BCS)

4. DIP switch set-up

Confirm the set-up of the DIP switch before the operation. “ON” means “H” and “OFF” means “L”.

4-1.System Clock

There are two methods to set MCLK frequency. In Manual Setting Mode (ACKS = “0”: Register 00H), the sampling speed is set by DFS0/1(Table 1,4). CKS0/1/2 set the frequency of MCLK at each sampling speed (Table 2,5). In Auto Setting Mode (ACKS = “1”: Default), as MCLK frequency is detected automatically (Table 9), and the internal master clock becomes the appropriate frequency, it is not necessary to set DFS0/1 and CKS0/1/2. In parallel mode, CKS2 and DFS1 are fixed to “0”.

All external clocks (MCLK, BICK and LRCK) should always be present whenever the AK4395 is in normal operation mode (PD = “H”). If these clocks are not provided, the AK4395 may draw excess current because the device utilizes dynamic refreshed logic internally. If the external clocks are not present, the AK4395 should be in the power-down mode (PDN = “L”) or in the reset mode (RSTN = “0”). After exiting reset at power-up etc., the AK4395 is in power-down mode until MCLK and LRCK are input.

Parallel Mode :

DFS0 (SW3-1)	Sampling Rate (fs)		
OFF	Normal Speed Mode	30kHz~54kHz	Default
ON	Double Speed Mode	60kHz~108kHz	

Table 1.Sampling Speed (Manual Setting Mode)
Note: DFS1(Register 00H) can be set at only serial mode.

Mode	ACKS (SW4-3)	CKS1 (SW4-2)	CKS0 (SW4-1)	Normal	Double	Quad	
0	OFF	OFF	OFF	256fs	128fs	N/A	Default
1	OFF	OFF	ON	256fs	256fs	N/A	
2	OFF	ON	OFF	384fs	192fs	N/A	
3	OFF	ON	ON	384fs	384fs	N/A	
*	ON	*	*	512fs /768fs	256fs /384fs	128fs /192fs	

Table 2. Master Clock (Manual Setting Mode)
Note: When ACKS is ON, Auto Setting Mode is enabled.

Serial Mode :

CAD0 (SW3-1)	DZFR (SW4-3)	CAD1 (SW4-2)	DZFL (SW4-1)	
OFF	OFF	OFF	OFF	Default

Table 3. Set up of SW3-1 and SW4
Note: SW4-1 and SW4-3 must be always OFF.
SW3-1 and SW4-2 are chip addresses of uP I/F.

DFS1	DFS0	Sampling Rate (fs)		
OFF	OFF	Normal Speed Mode	30kHz~54kHz	Default
OFF	ON	Double Speed Mode	60kHz~108kHz	
ON	OFF	Quad Speed Mode	120kHz~216kHz	

Table 4. Sampling Speed (Manual Setting Mode)

Mode	CKS2	CKS1	CKS0	Normal	Double	Quad	
0	OFF	OFF	OFF	256fs	128fs	N/A	Default
1	OFF	OFF	ON	256fs	256fs	N/A	
2	OFF	ON	OFF	384fs	192fs	N/A	
3	OFF	ON	ON	384fs	384fs	N/A	
4	ON	OFF	OFF	512fs	256fs	128fs	
5	ON	OFF	ON	512fs	N/A	N/A	
6	ON	ON	OFF	768fs	384fs	192fs	
7	ON	ON	ON	768fs	N/A	N/A	

Table 5. Master Clock (Manual Setting Mode)
Note: The master clock at quad speed support only 128fs or 192fs.

RCK	MCLK				BICK
fs	256fs	384fs	512fs	768fs	64fs
32.0kHz	8.1920MHz	12.288MHz	16.3840MHz	24.576MHz	2.0480MHz
44.1kHz	11.2896MHz	16.9344MHz	22.5792MHz	33.8688MHz	2.8224MHz
48.0kHz	12.2880MHz	18.4320MHz	24.5760MHz	36.8640MHz	3.0720MHz

Table 6. System Clock example (Normal Speed Mode @Manual Setting Mode)

LRCK	MCLK				BICK
fs	128fs	192fs	256fs	384fs	64fs
88.2kHz	11.2896MHz	16.9344MHz	22.5792MHz	33.8688MHz	5.6448MHz
96.0kHz	12.2880MHz	18.4320MHz	24.5760MHz	36.8640MHz	6.1440MHz

Table 7. System Clock example (Double Speed Mode @Manual Setting Mode)

LRCK	MCLK		BICK
fs	128fs	192fs	64fs
176.4kHz	22.5792MHz	33.8688MHz	11.2896MHz
192.0kHz	24.5760MHz	36.8640MHz	12.2880MHz

Table 8. System Clock example (Quad Speed Mode @Manual Setting Mode)

MCLK		Sampling Speed
512fs	768fs	Normal
256fs	384fs	Double
128fs	192fs	Quad

Table 9. Sampling Speed (Auto Setting Mode)

LRCK	MCLK (MHz)						Sampling Speed
fs	128fs	192fs	256fs	384fs	512fs	768fs	
32.0kHz	-	-	-	-	16.3840	24.5760	Normal
44.1kHz	-	-	-	-	22.5792	33.8688	
48.0kHz	-	-	-	-	24.5760	36.8640	
88.2kHz	-	-	22.5792	33.8688	-	-	Double
96.0kHz	-	-	24.5760	36.8640	-	-	
176.4kHz	22.5792	33.8688	-	-	-	-	Quad
192.0kHz	24.5760	36.8640	-	-	-	-	

Table 10. System Clock example (Auto Setting Mode)

4-2. Set-up of SW3,(Mode set-up of AK4395: see the datasheet of AK4395)

Mode	DIF2 (SW3-2)	DIF1 (SW3-3)	DIF0 (SW3-4)	Mode	BICK	
0	OFF	OFF	OFF	0: 16bit LSB Justified	≥32fs	
1	OFF	OFF	ON	1: 20bit LSB Justified	≥40fs	
2	OFF	ON	OFF	2: 24bit MSB Justified	≥48fs	
3	OFF	ON	ON	3: I^2S Compatible	≥48fs	(default)
4	ON	OFF	OFF	4: 24bit LSB Justified	≥48fs	

Table 11. Audio Serial Interface Format Select pins (SW3-2,3,4)

4-3.Set-up of SW6(Mode set-up of CS8414. About details, see the datasheet of CS8414)

Adjust the audio format of CS8414(DIR) to AK4395. CS8414 does not match the LSB justified 20bit/24bit mode of AK4395.

M3 (SW6-2)	M2 (SW6-3)	M1 (SW6-4)	M0 (SW6-5)	Format	JP4	
OFF	OFF	OFF	OFF	24bit MSB Justified	INV	
OFF	OFF	ON	OFF	I^2S Compatible	THR	(default)
OFF	ON	OFF	ON	16bit LSB Justified	THR	

Table 12. Set-up SW6

SW6-1(SEL) :Usually ON.
SW6-6(CS12): Select the channel for indicating the channel status.
ON: Rch, OFF: Lch(default)

5. Parallel/Serial Control

SW5: set up P/S pin of AK4395.
"H": Parallel mode. Nothing should be connected to PORT3. JP11, 12 and 13 should be short.
"L": Serial mode. PORT3 is used. JP11, 12 and 13 should be open. SW4-1 and SW4-3 must be OFF.

6. Other set-up

SW1: Reset of AK4395. Select "H" during operation.
SW2: Soft-mute of AK4395. The soft-mute is executed during SW2 pushed.
LE1 : This LED shows pre-emphasis status. It turns on when the data is pre-emphasized.
LE2 : This LED shows the output of VERF pin in CS8414. It turns on when the error is occured in CS8414.

■ AK4395 Measurement Example

Conditions:

AVDD =DVDD= 5.0V (AVDD is supplied by regulator)
Interface = DIR (44.1kHz, 96kHz)
MCLK = 256fs(fs=44.1kHz, 96kHz)
BICK = 64fs
fs = 44.1kHz, 96kHz,
Input data = 24bit
Room Temperature
Measurement unit: Audio Precision System Two Cascade (fs=44.1kHz, 96kHz)

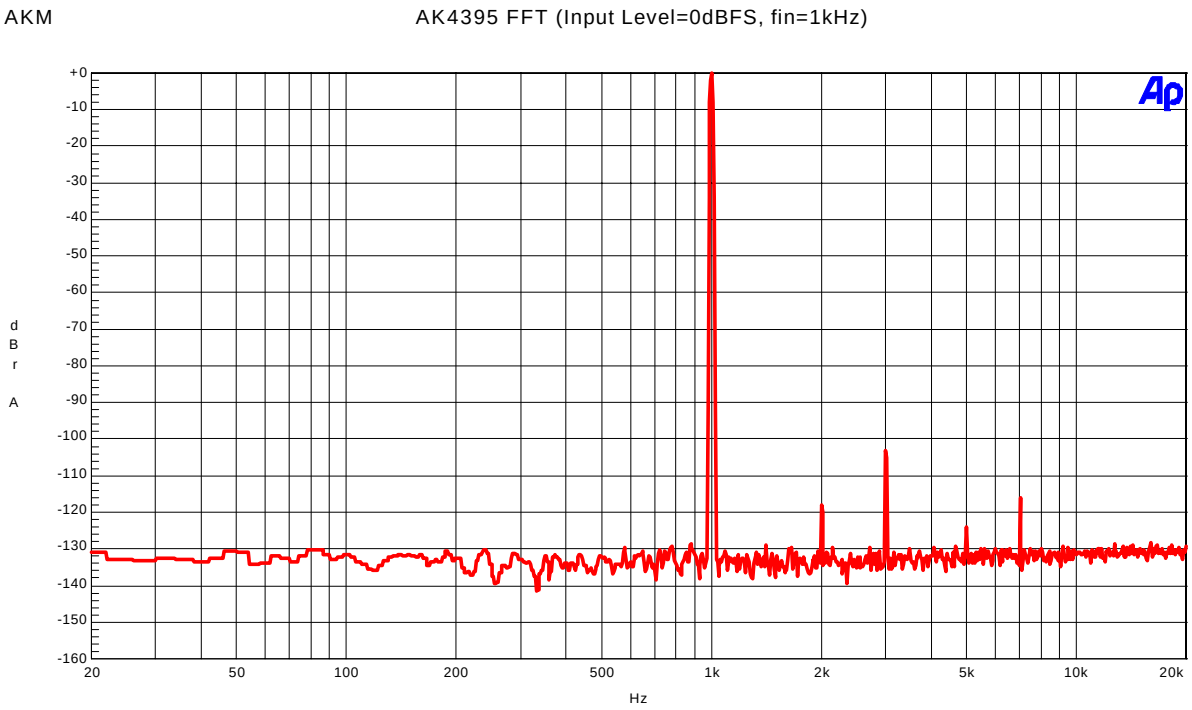
fs=44.1kHz

Parameter	Input signal	Measurement filter	Lch	Rch
S/(N+D)	1kHz, 0dB	20kLPF	102.0dB	102.1dB
DR	1kHz, -60dB	20kLPF	116.9dB	116.8dB
		22kLPF, A-weighted	119.2dB	119.2dB
S/N	no signal	20kLPF	117.8dB	117.8dB
		22kLPF, A-weighted	120.1dB	120.1dB

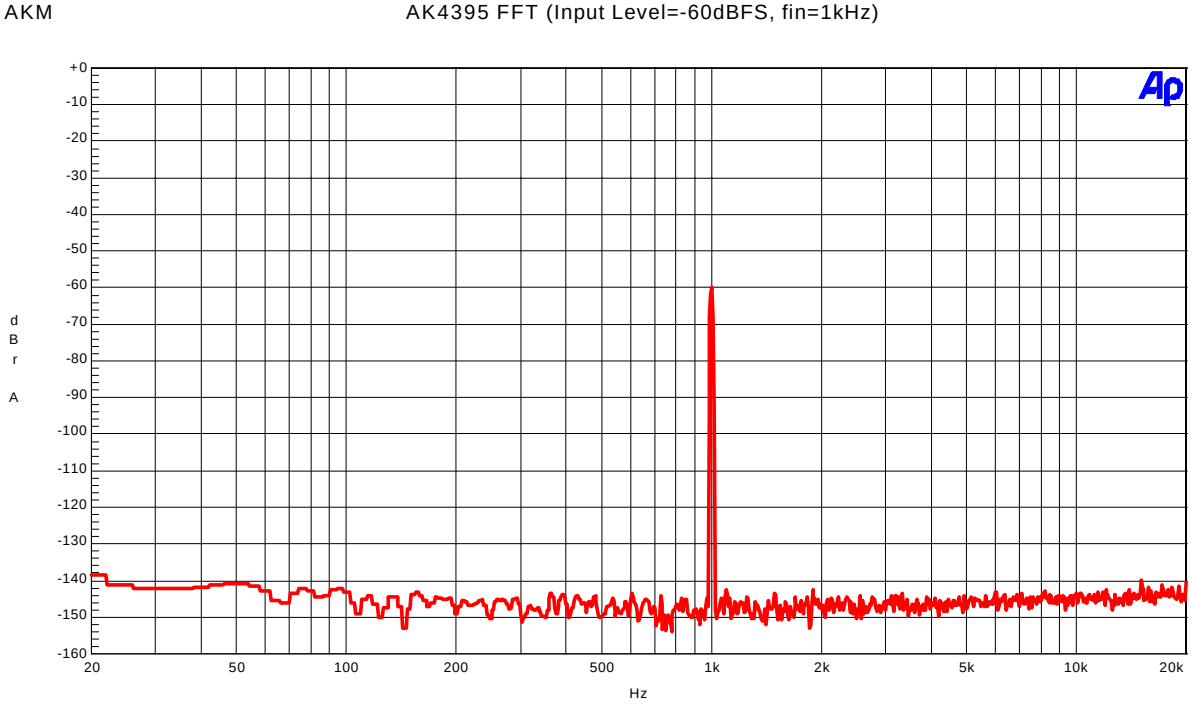
fs=96kHz

Parameter	Input signal	Measurement filter	Lch	Rch
S/(N+D)	1kHz, 0dB	40kLPF	100.0dB	100.0dB
DR	1kHz, -60dB	40kLPF	114.4dB	114.4dB
		80kLPF, A-weighted	119.9dB	119.5dB
S/N	no signal	40kLPF	114.6dB	114.4dB
		80kLPF, A-weighted	119.7dB	119.5dB

(fs=44.1kHz)

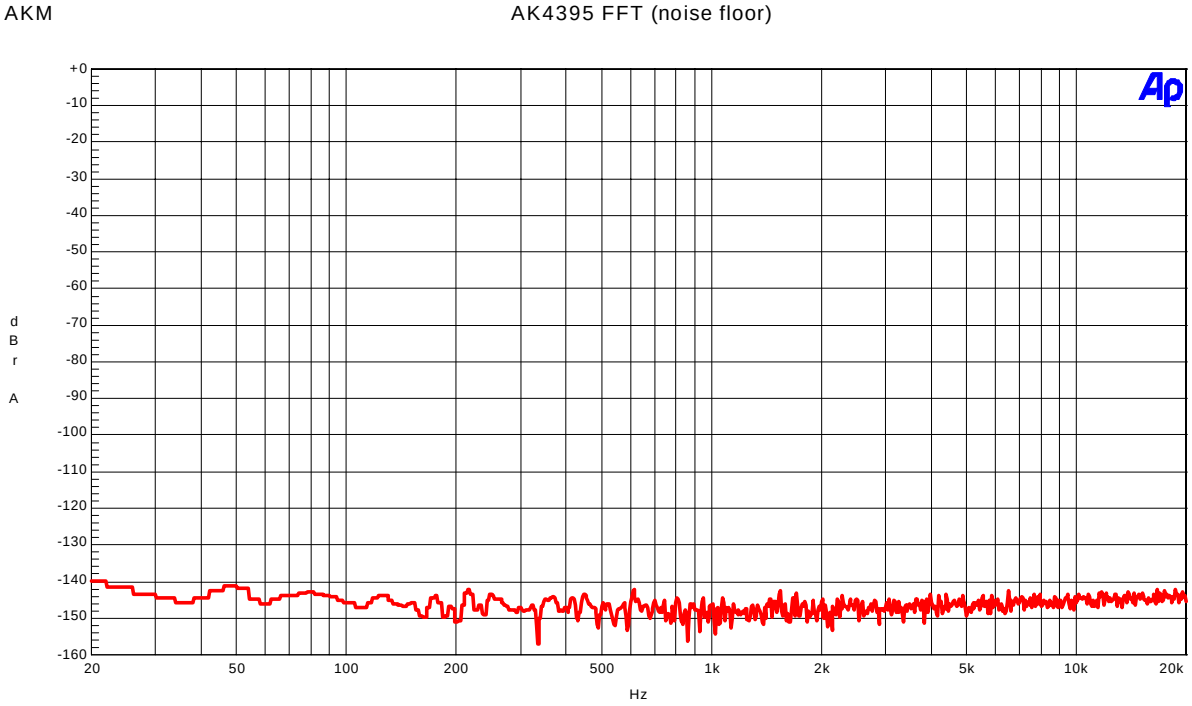


FFT (1kHz, 0dBFS input)

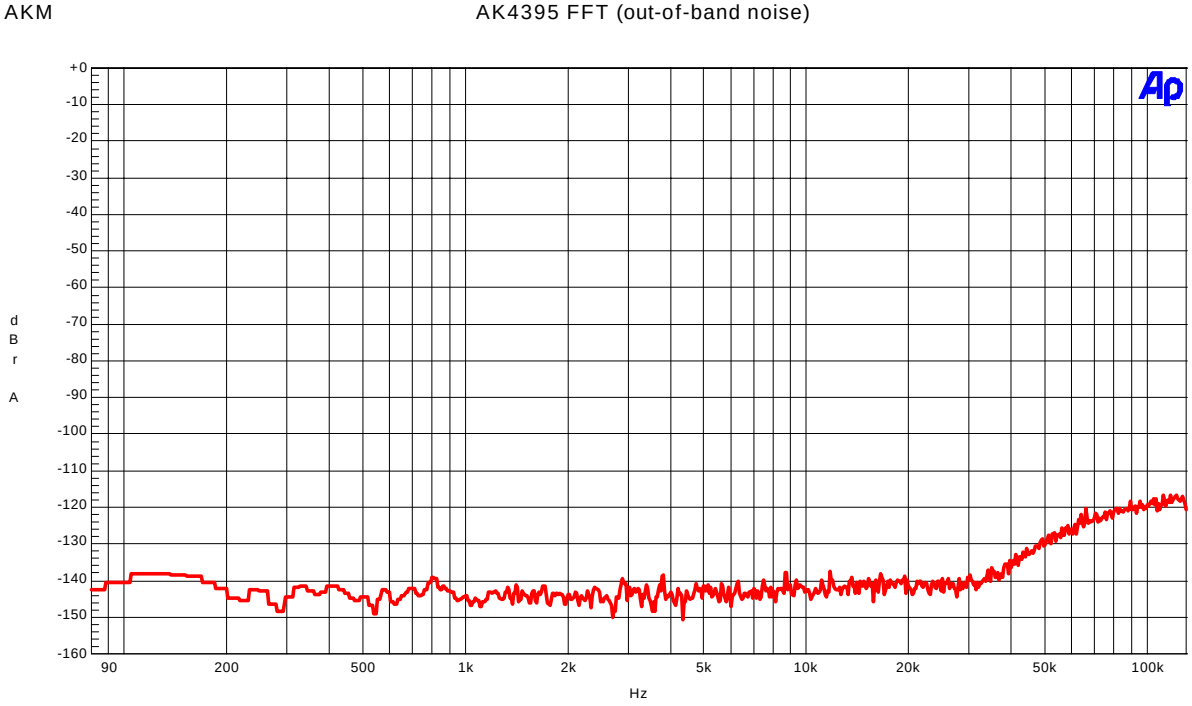


FFT (1kHz, -60dBFS input)

(fs=44.1kHz)

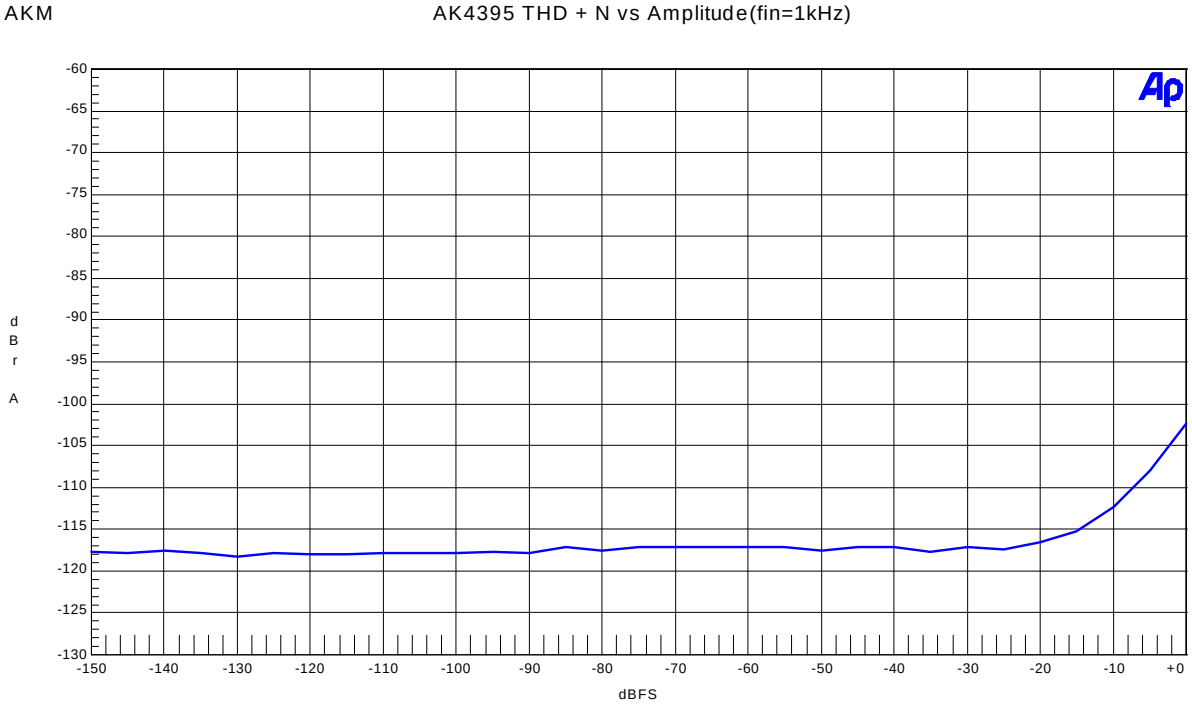


FFT (noise floor)

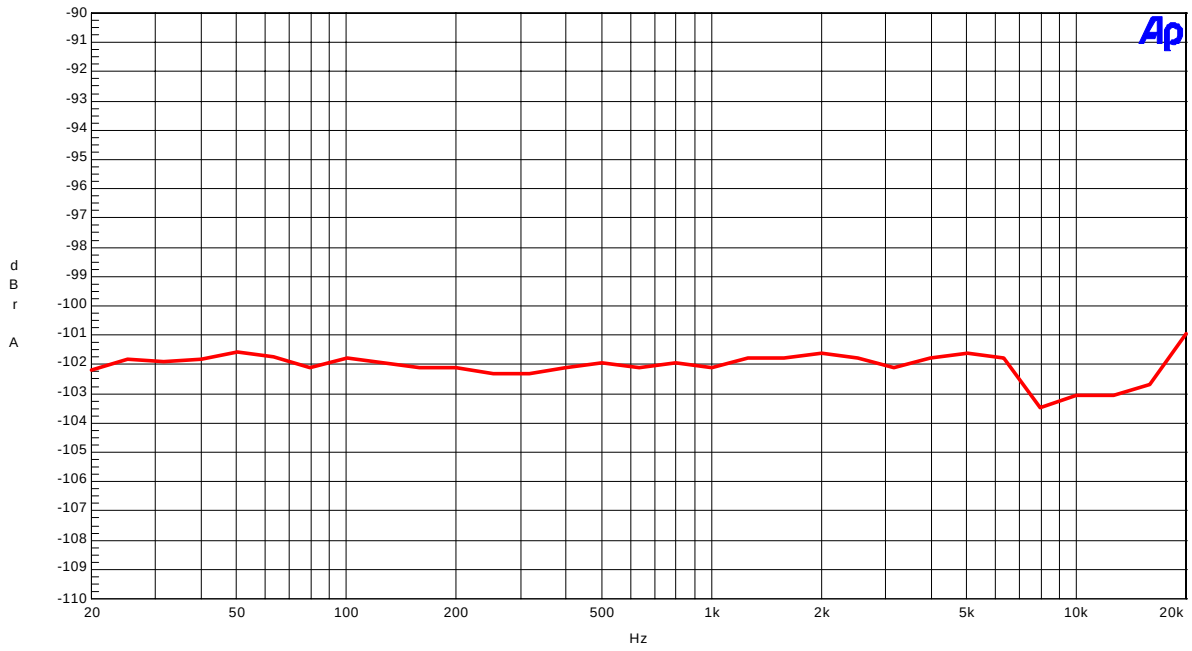


FFT (out-of-band noise)

(fs=44.1kHz)

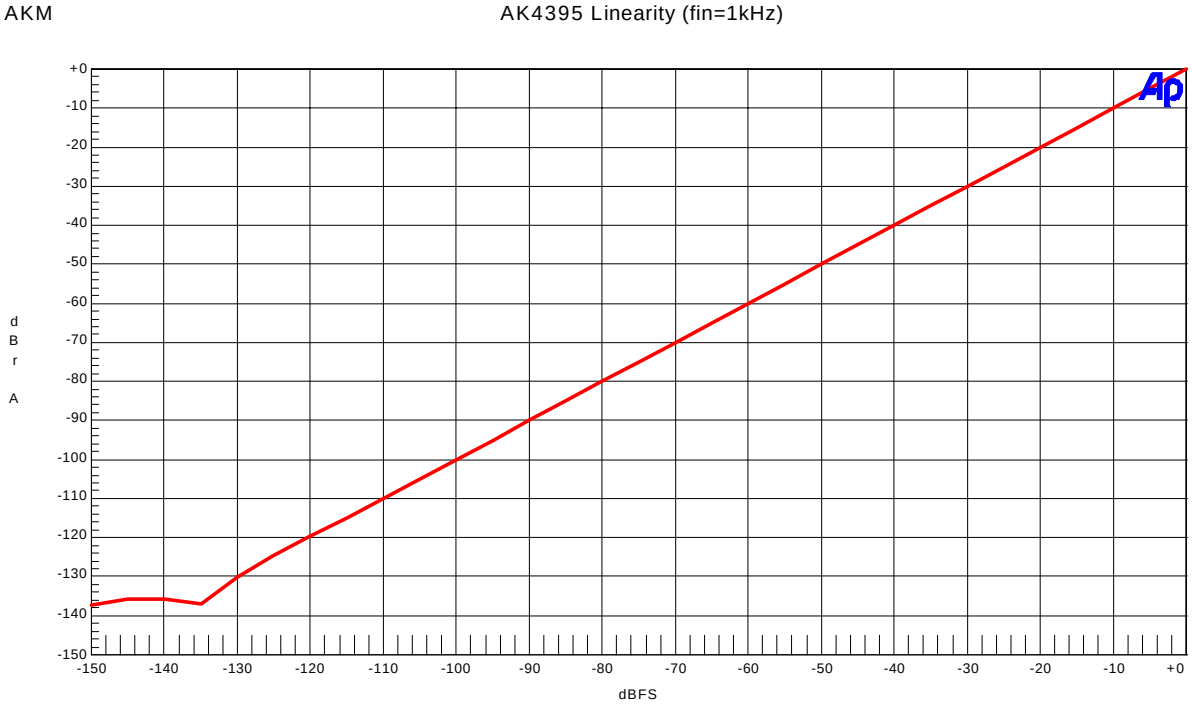


THD+N vs Input Level (fin=1kHz)

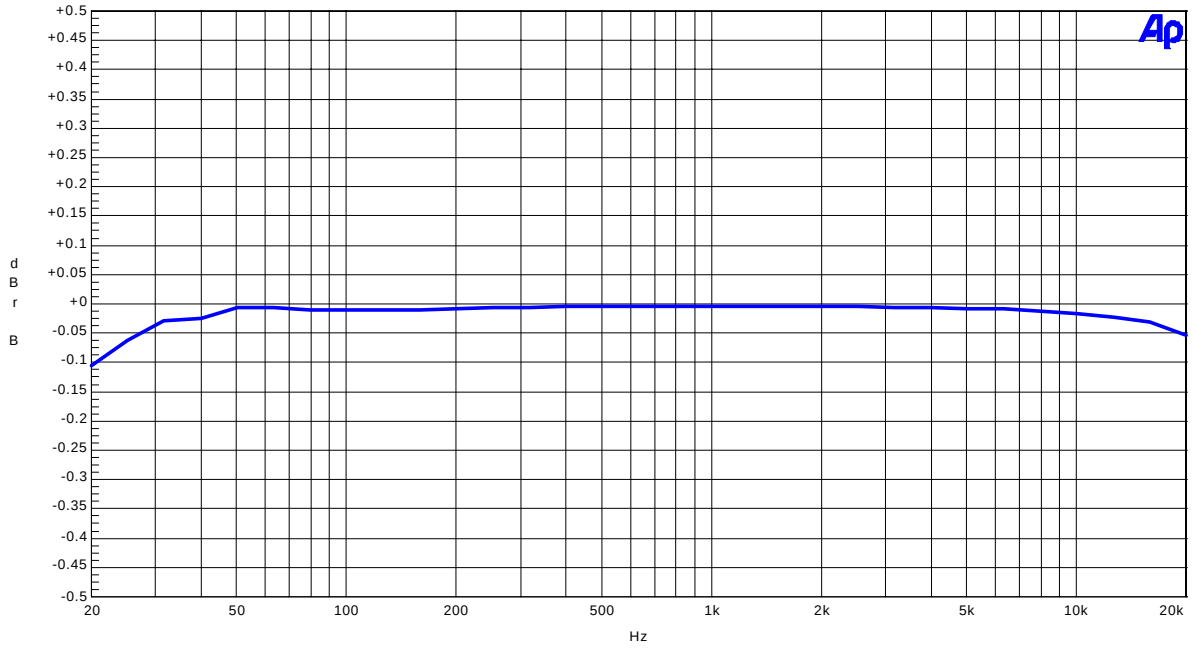


THD+N vs fin (Input level=0dBFS)

(fs=44.1kHz)

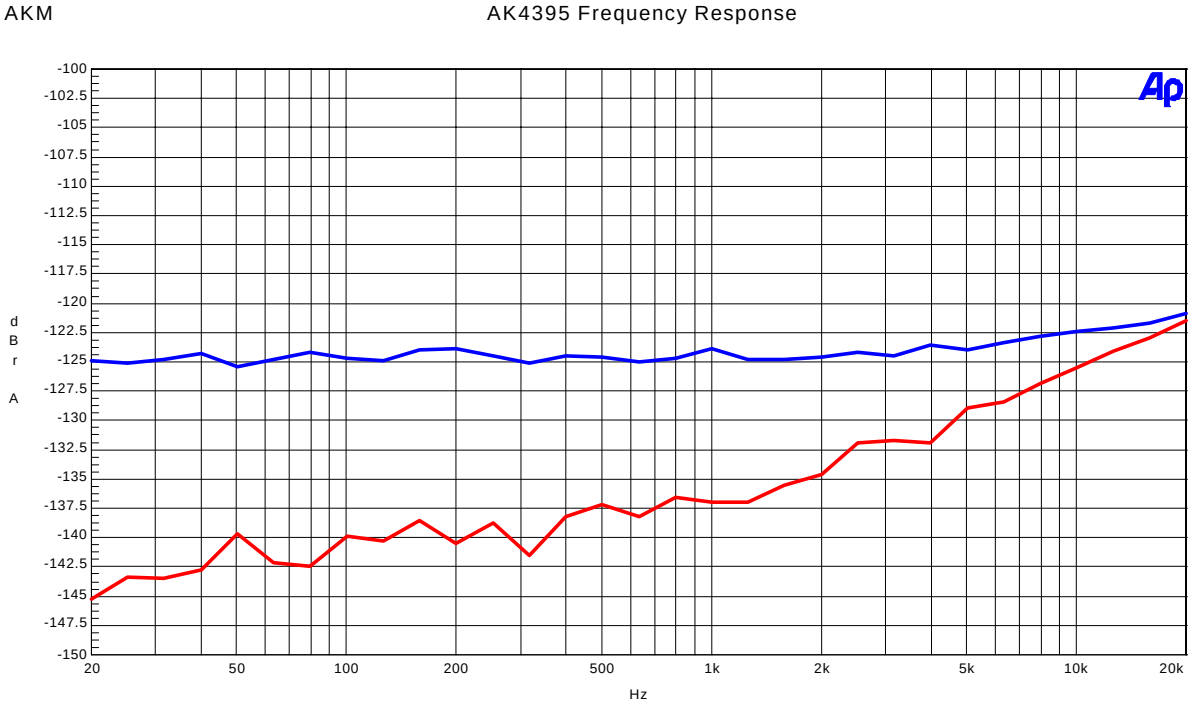


Linearity (fin=1kHz)



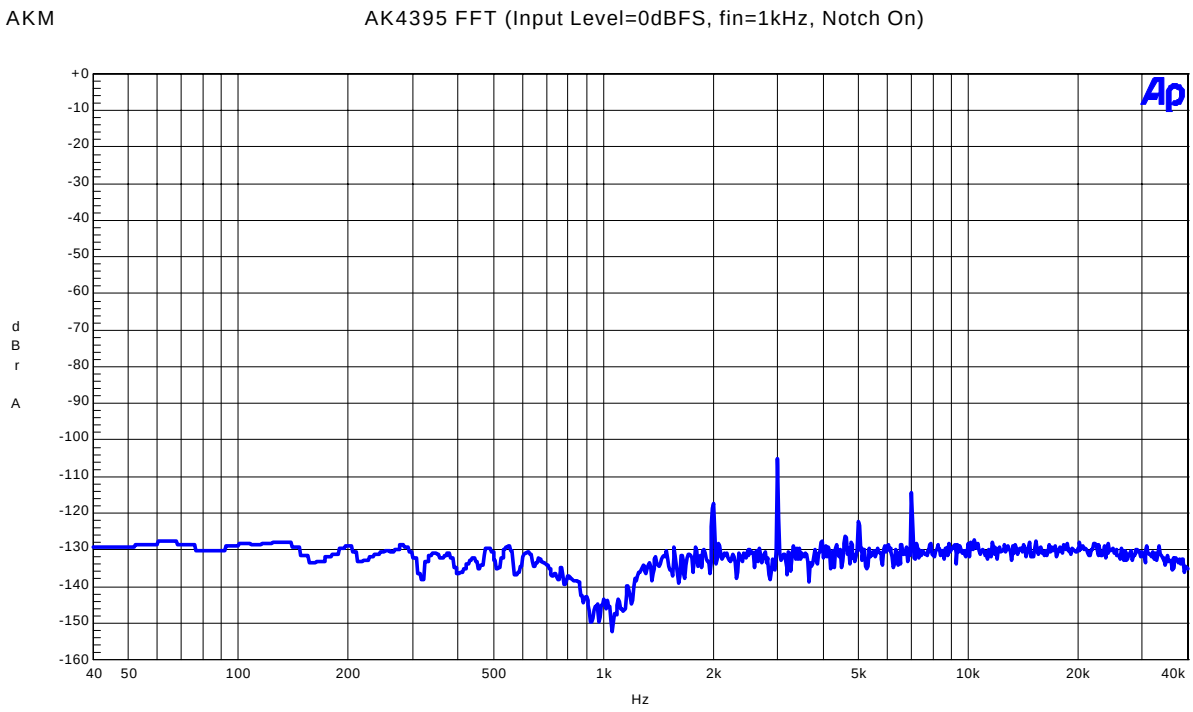
Frequency Response (Input level=0dBFS)

(fs=44.1kHz)

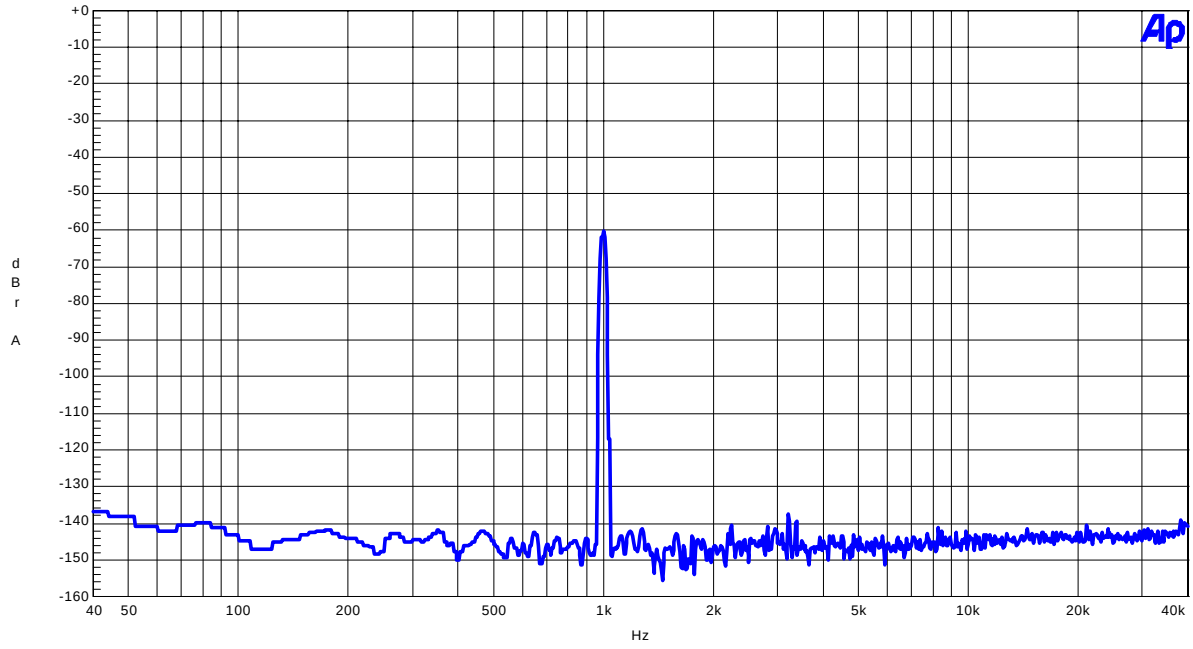


Cross-talk (Input level=0dBFS)

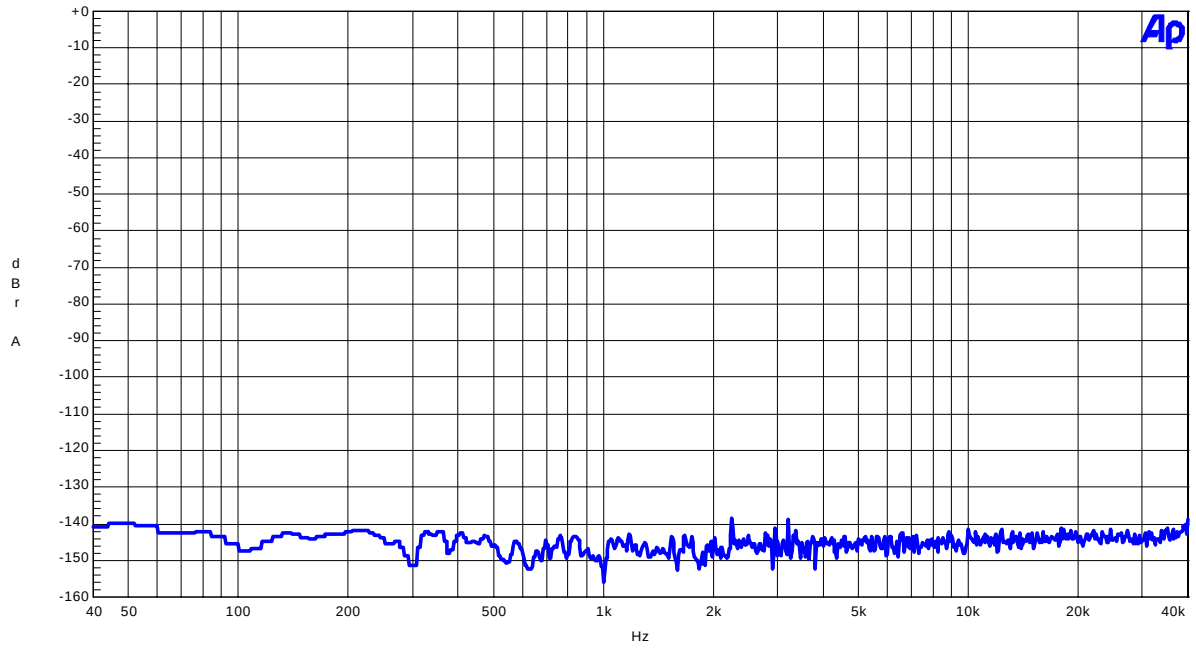
(fs=96kHz)



FFT (1kHz, 0dBFS input, Notch=NO)

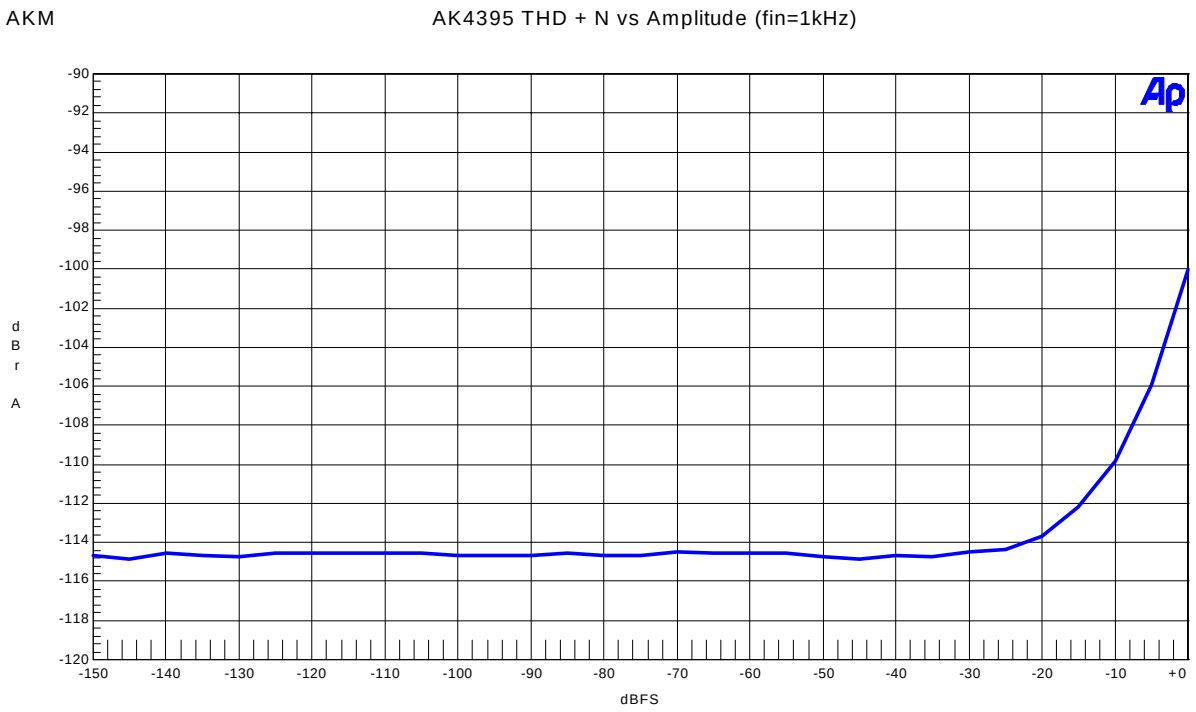


FFT (1kHz, -60dBFS input)

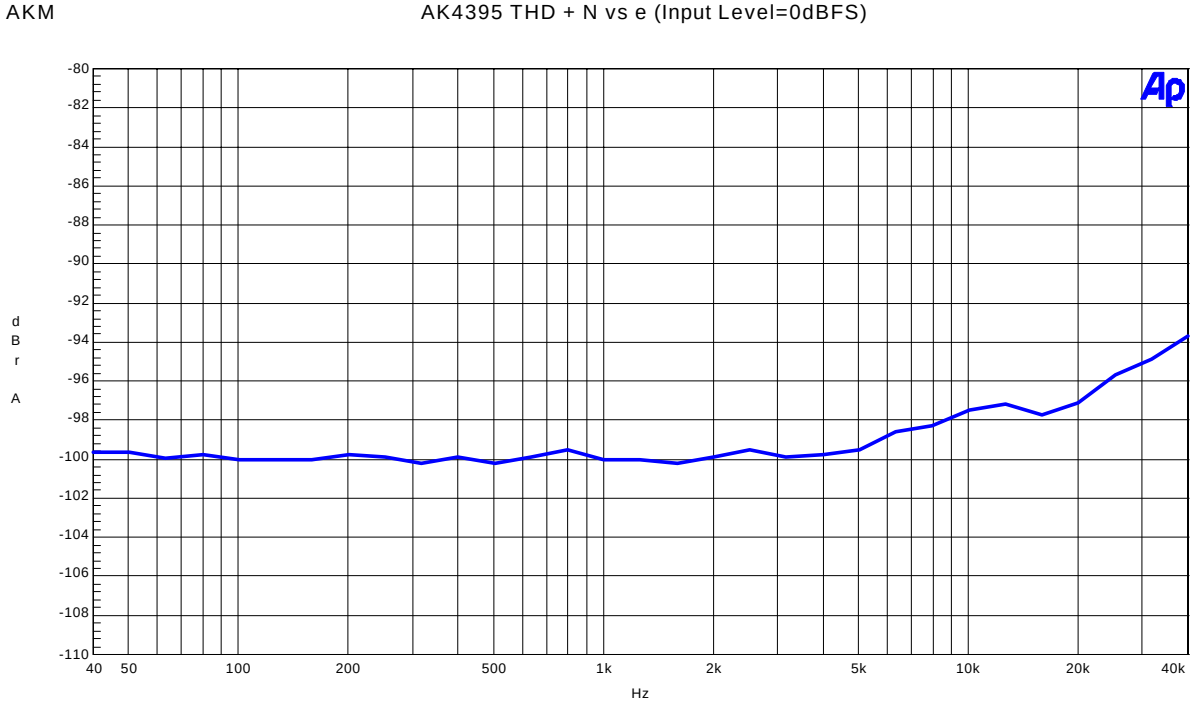


FFT (noise floor)

(fs=96kHz)

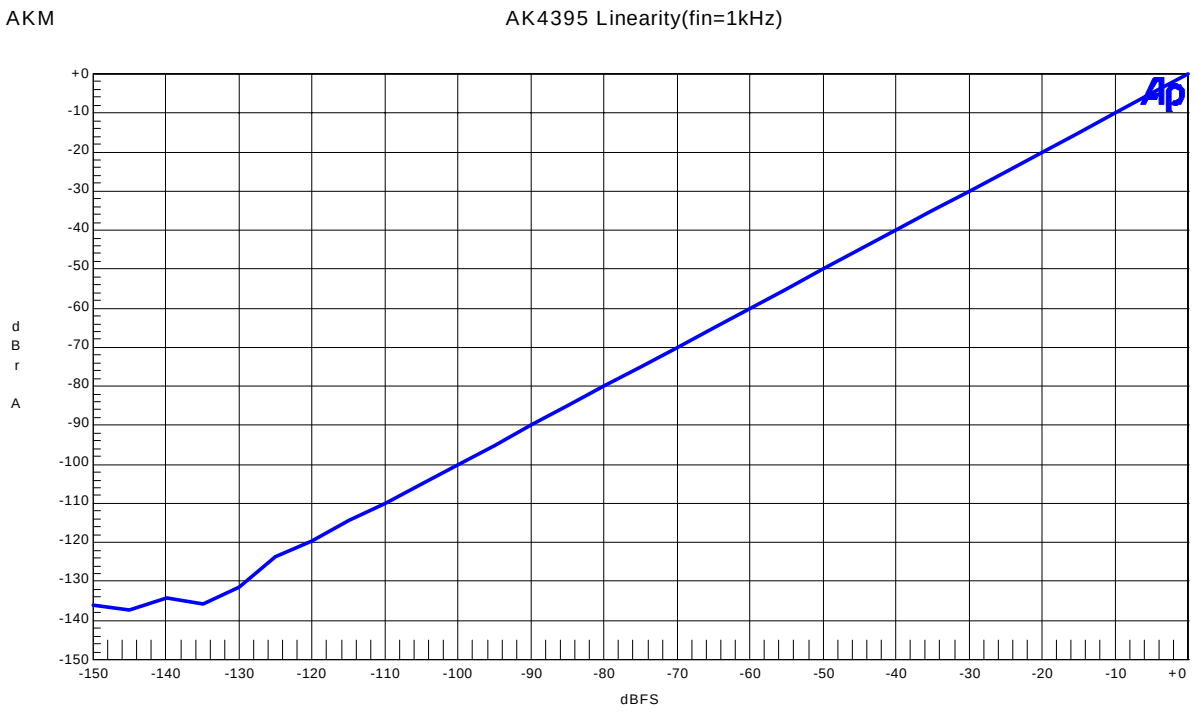


THD+N vs Input Level (fin=1kHz)

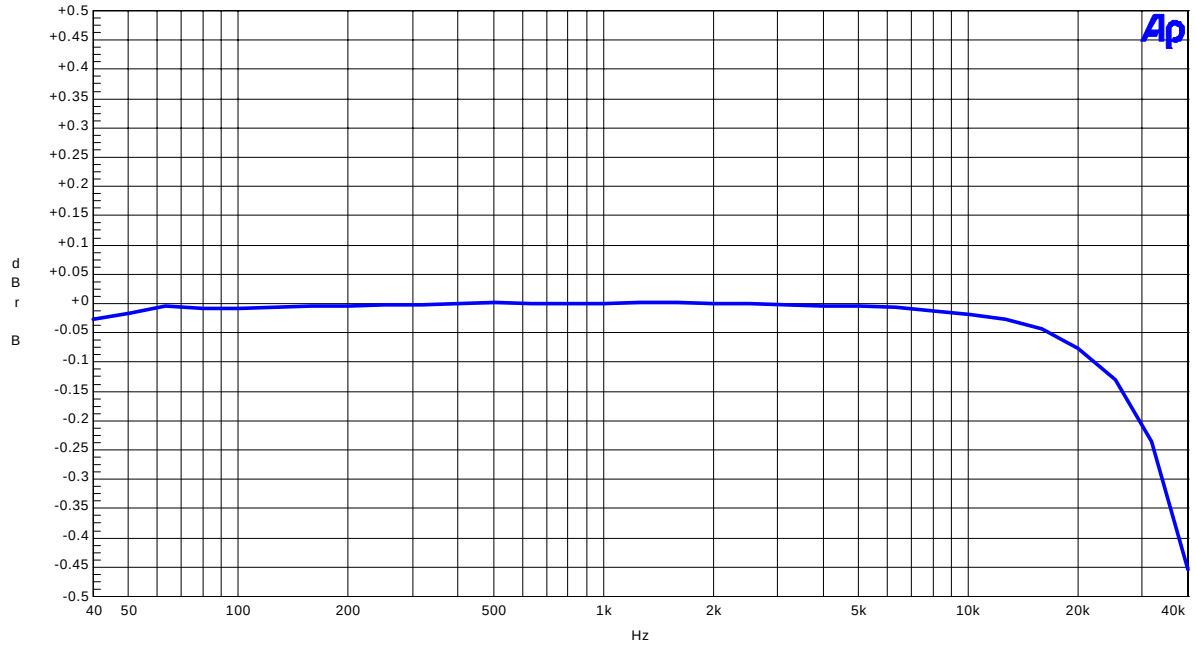


THD+N vs fin (Input level=0dBFS)

(fs=96kHz)



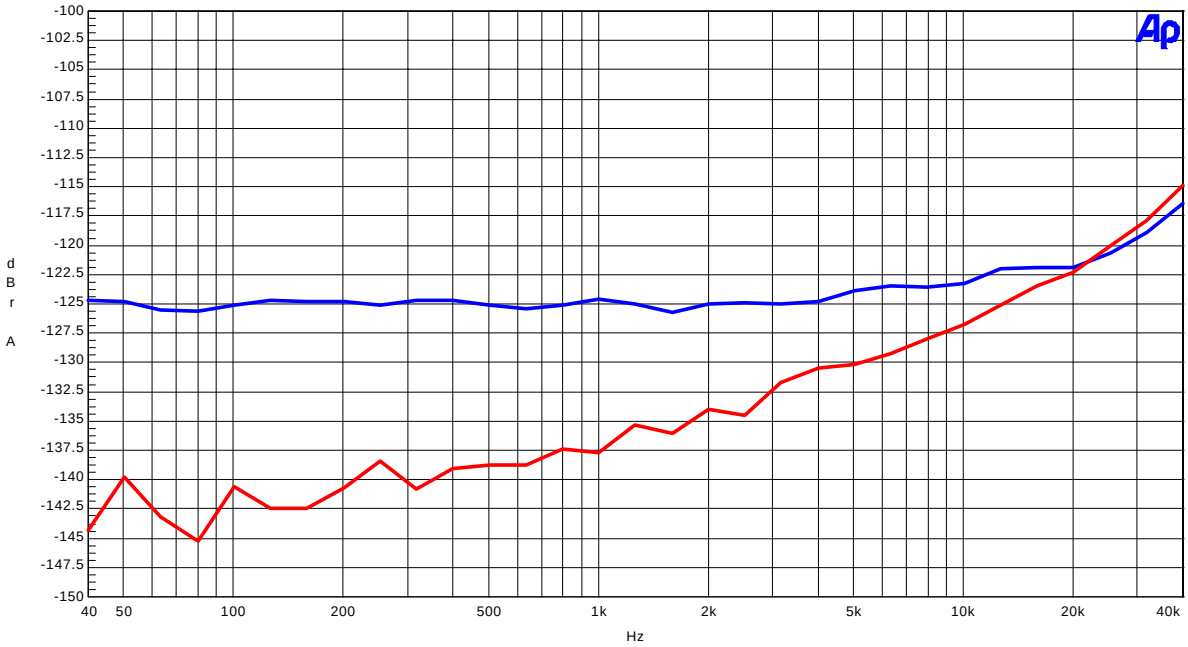
Linearity (fin=1kHz)



Frequency Response (Input level=0dBFS)
(Including external LPF)

(fs=96kHz)

AKM AK4395 Crosstalk



Cross-talk (Input level=0dBFS)

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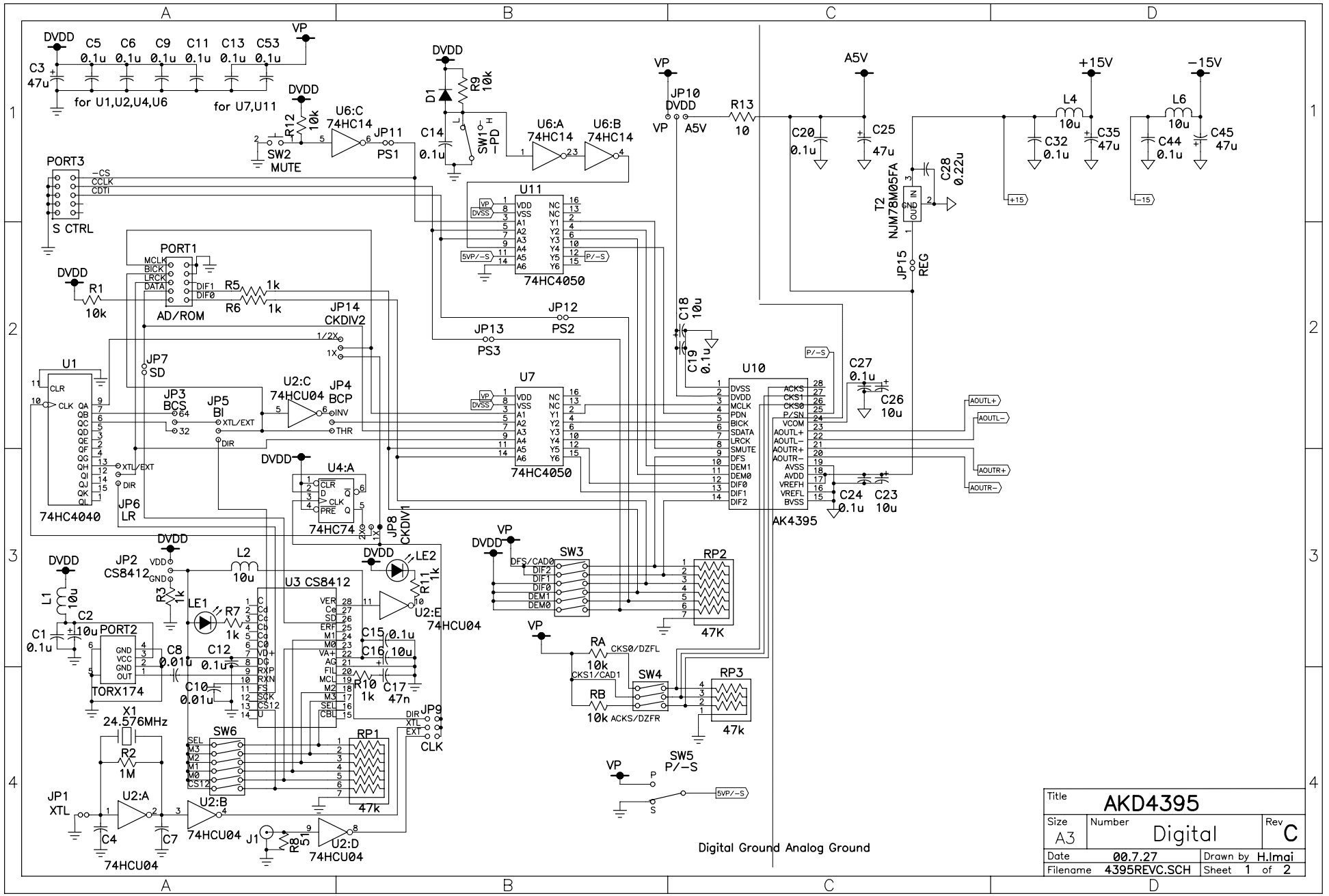
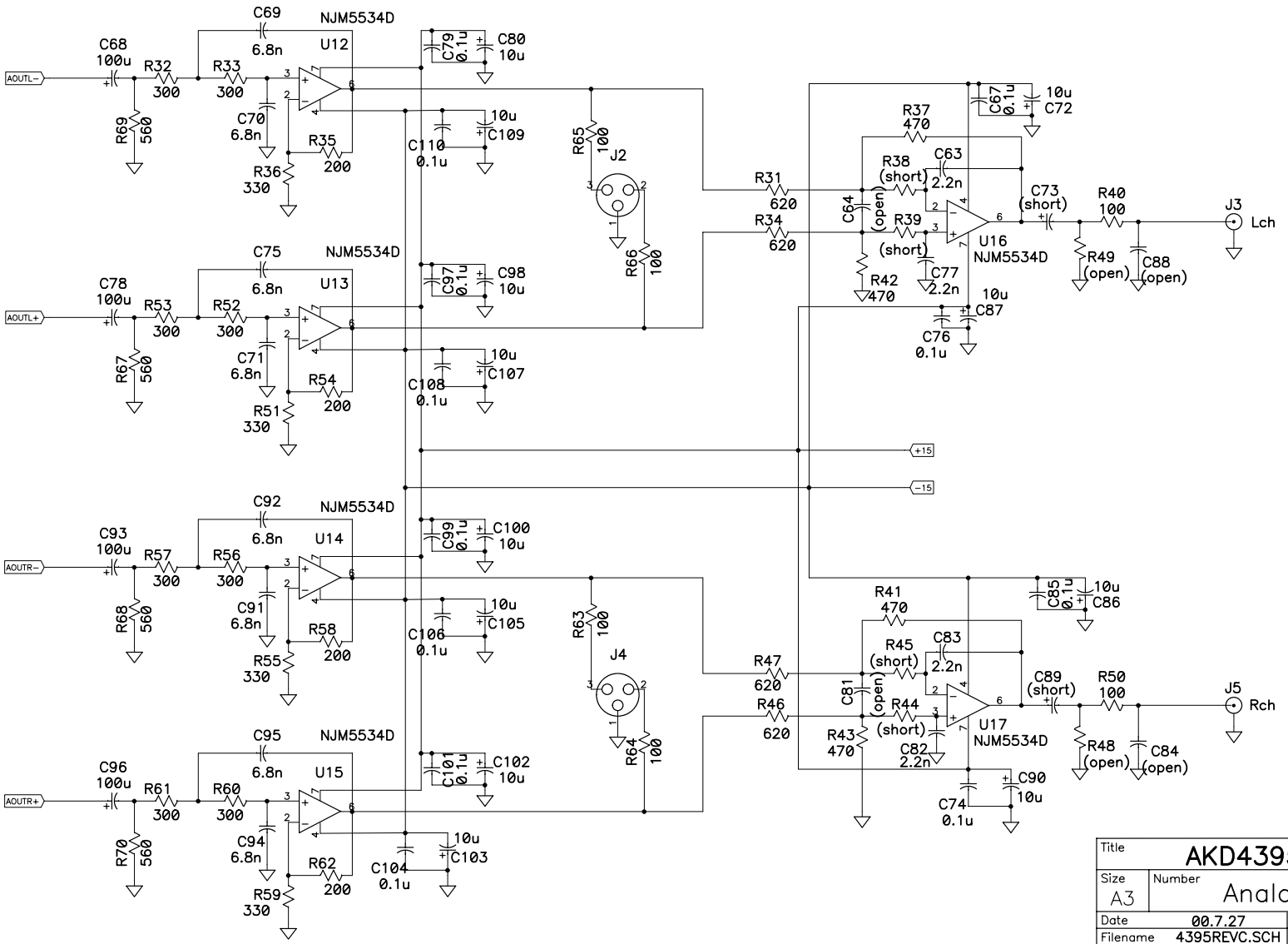

DVDD
VP
C3 47u
C5 0.1u
C6 0.1u
C9 0.1u
C11 0.1u
C13 0.1u
C53 0.1u
for U1,U2,U4,U6
for U7,U11
R12 10k
U6:C 74HC14
JP11
PS1
SW2 MUTE
D1
R9 10k
C14 0.1u
SW1 PD
U6:A 74HC14
U6:B 74HC14
JP10
R13 10
A5V
C20 0.1u
C25 47u
+15V
−15V
L4 10u
L6 10u
C32 0.1u
C35 47u
C44 0.1u
C45 47u
T2 NJM78M05FA
C28 0.22u
JP15 REG
PORT3
−CS
CCLK
CDTI
S CTRL
U11
74HC4050
PORT1
MCLK
BICK
LRCK
SDATA
DIF1
DIF0
AD/ROM
R1 10k
R5 1k
R6 1k
JP14 CKDIV2
1/2X
1X
JP12
PS2
JP13
PS3
C18 10u
C19 0.1u
U1
74HC4040
JP7 SD
JP3 BCS
JP5 BI
XTL/EXT
DIR
U2:C 74HCU04
JP4 BCP
INV
THR
U7
74HC4050
U10
AK4395
P/−S
C27 0.1u
C26 10u
C24 0.1u
C23 10u
AOUTL+
AOUTL−
AOUTR+
AOUTR−
U4:A
74HC74
JP8 CKDIV1
JP6 LR
JP2 CS8412
L2 10u
L1 10u
R3 1k
LE1
R7 1k
LE2
R11 1k
U2:E 74HCU04
U3 CS8412
C2 10u
C1 0.1u
PORT2
TORX174
C8 0.01u
C12 0.1u
C10 0.01u
C15 0.1u
C16 10u
C17 47n
R10 1k
X1 24.576MHz
R2 1M
JP9
XTL
EXT
CLK
SW6
RP1
47k
SW3
DFS/CAD0
DIF2
DIF1
DIF0
DEM1
DEM0
RP2
47K
RA 10k
CKS0/DZFL
CKS1/CAD1
RB 10k
ACKS/DZFR
SW4
RP3
47k
SW5 P/−S
5VP/−S
JP1 XTL
U2:A
U2:B
U2:D
74HCU04
C4
C7
R8 51
J1
Digital Ground Analog Ground
Title AKD4395
Size A3
Number Digital
Rev C
Date 00.7.27
Drawn by H.Imai
Filename 4395REVC.SCH
Sheet 1 of 2



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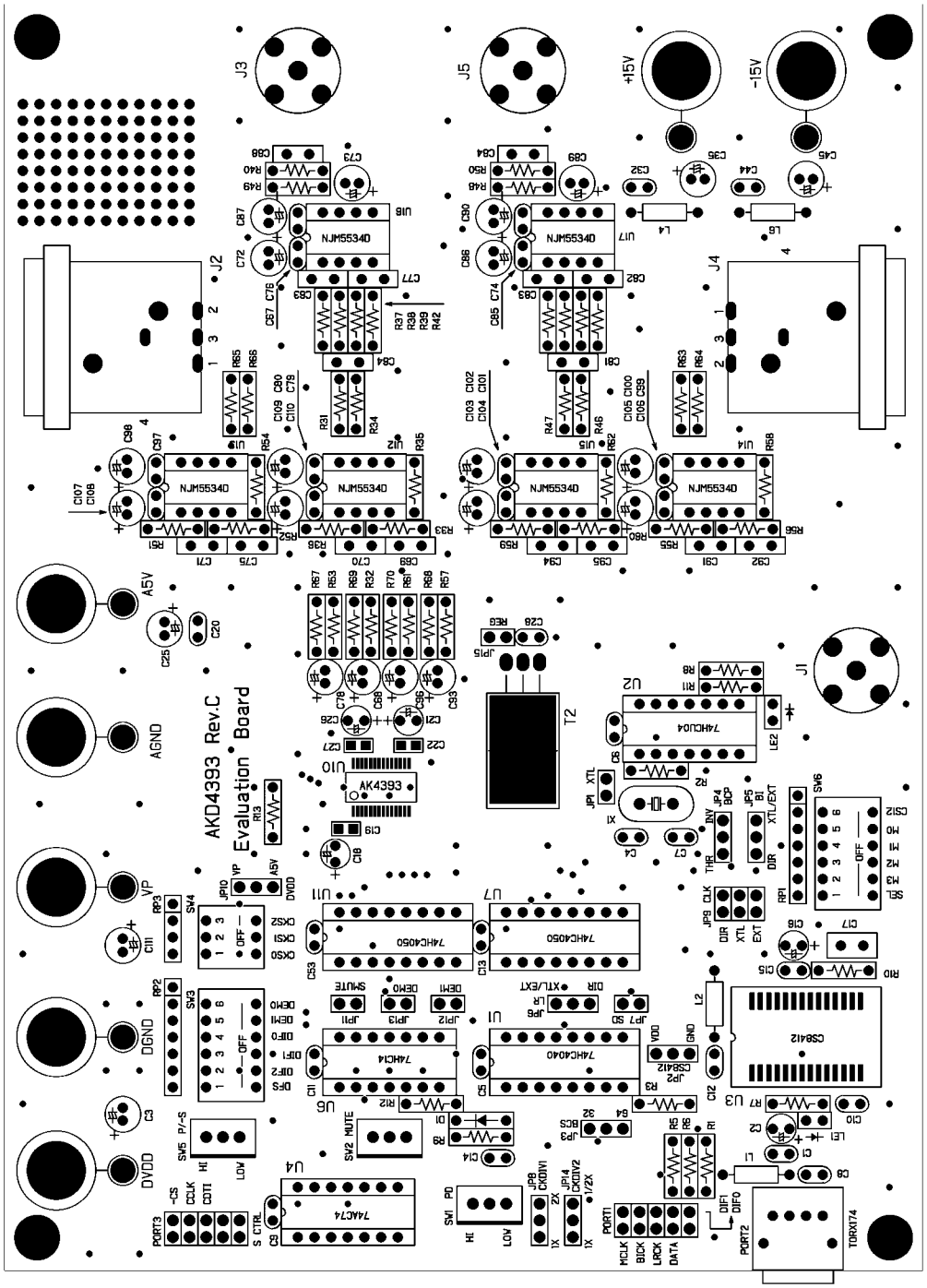
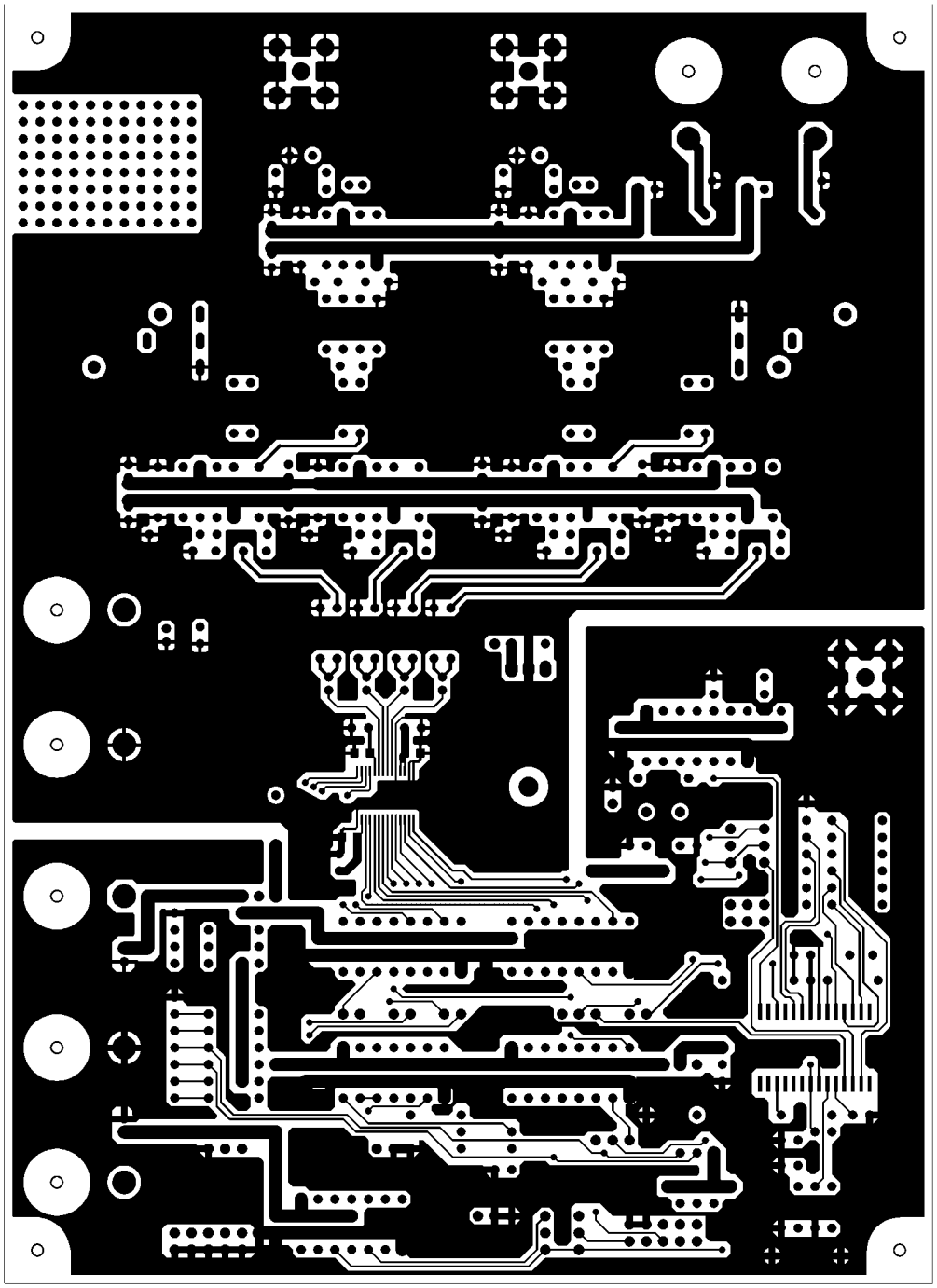
Size A3	Number Analog	Rev C
Date 00.7.27		Drawn by H.Imai
Filename 4395REVC.SCH		Sheet 2 of 2



4393C L1 SR SILK



4393C L1

L2 C3936