

Data Sheet

CX60083-15/-2A

10 Gbps High Gain Limiting Amplifier

Key Features

- Limiting amplifier
- Integrated LOS and peak detect circuit
- Wide bandwidth and high sensitivity
- Compatible with DC- or AC-coupled input and output signals
- Fully differential architecture
- Optional single-ended input and/or output operation
- Available in a 32-terminal, 5 mm square EdQuad TQFP or as dice

Applications

- Fiber-optic communications (OC-48/OC-192)
- SONET/SDH test equipment
- Data communications

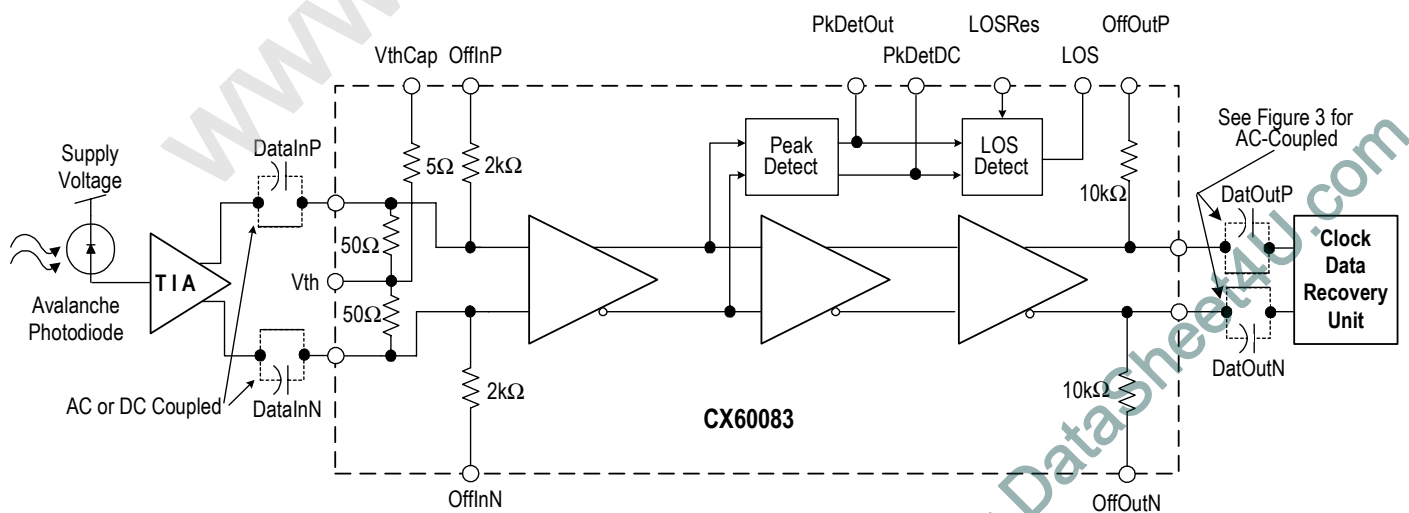
Product Description

The CX60083 is a high-gain, wide-bandwidth, limiting amplifier ideal for use as a post-amplifier in fiber-optic receivers. With its 10GHz bandwidth, this amplifier has been optimized for data rates up to 10.7 Gbps and has an input sensitivity (BER < 10⁻¹⁰) of 5 mV, differential. It accepts both single-ended and differential inputs and may be either AC- or DC-coupled. With approximately 39 dB of small signal gain, this amplifier can limit input voltages at or above 5 mV_{P-P} (single-ended) to an output voltage of 460 mV_{P-P} (single-ended).

An on-chip Loss of Signal (LOS) detection circuit with hysteresis provides an LOS output signal. A high-gain, on-chip, peak detector provides a DC output signal that is linearly proportional to the input signal amplitude. This signal can be used for Automatic Gain Control (AGC) of preceding amplifier stages or a custom LOS network. High-impedance differential outputs and inputs are available for input voltage offset correction.

The CX60083, as shown in Figure 7, is available in a 32-terminal flat pack or as shown in Figure 9 in die form. Figure 1 is the system block diagram.

Figure 1. CX60083 System Block Diagram



Signal Amplification and Termination

The CX60083 is optimized to accept up to 10.7 Gbps data on the 50 Ω inputs DataInP and DataInN. The input signal is amplified 39 dB up to approximately 460 mV_{PP} (single-ended) and is limited to this value with any further input signal increase. Data rates greater than 10.7 Gbps (including 12.5 Gbps) may be input but with reduced small signal gain.

The outputs are available at the DataOutP and DataOutN pins. The outputs have an internal 50 Ω impedance and are designed to drive a 50 Ω load. When terminated in 50 Ω , the outputs swing between approximately –50 mV and approximately +50 mV.

The DataInP and DataInN inputs can be driven either differentially or single-ended, and can be DC-coupled or AC-coupled. Each of the differential inputs has a 50 Ω resistor terminated to the Vth terminal. In most cases Vth is grounded. However, it may be necessary to connect Vth to a DC potential to ensure the input signal does not exceed the maximum or minimum CX60083 peak input voltage. These requirements are described in more detail in Figure 4 and in the application note CX60083AN1: Input and Output Interface Terminations. VthCap provides for additional (optional) decoupling of Vth.

Table 1 lists the CX60083 terminal name descriptions.

Table 1. Terminal Name Descriptions

| Terminal Name | Terminal Number | Description | Signal |
|---------------|---|--|-------------------|
| VthCap | 2 | Vth Decoupling | DC |
| DataInP | 4 | High-speed Input Data (non-inverting polarity) | RF ₍₁₎ |
| DataInN | 5 | High-speed Input Data (inverting polarity) | RF ₍₁₎ |
| Vth | 7 | DataIn termination (Input Common Mode Voltage input when AC-coupled) | Power |
| OffInN | 10 | Negative Offset Control Input | Analog |
| OffInP | 11 | Positive Offset Control Input | Analog |
| OffOutP | 15 | Offset Sense Output (non-inverting) | Analog |
| OffOutN | 16 | Offset Sense Output (inverting) | Analog |
| DataOutN | 20 | High-speed Output Data (inverting polarity) | RF ₍₁₎ |
| DataOutP | 21 | High-speed Output Data (non-inverting polarity) | RF ₍₁₎ |
| PkDetDC | 27 | Peak Detector DC Reference | DC |
| PkDetOut | 28 | Peak Detector Output | DC |
| LOSRes | 29 | Loss Of Signal threshold control resistor | DC |
| LOS | 30 | Loss Of Signal (active high) | DC |
| Vee | 1, 8, 17, 24, 25, 32 | Power Supply | Power |
| Gnd | 3, 6, 9, 12, 13, 14, 18, 19, 22, 23, 26, 31 | Ground | Power |
| EP | Exposed Paddle | Package or die backside | DC ₍₂₎ |

Note 1: These are 50 Ω matched terminals.

Note 2: The package or die backside should be well connected to ground using either conductive epoxy or solder.

Output Terminations

The outputs DataOutP and DataOutN can be either DC- or AC-coupled to the succeeding stage. For further details see Application Note CX60083 AN1.

Offset Sense and Compensation

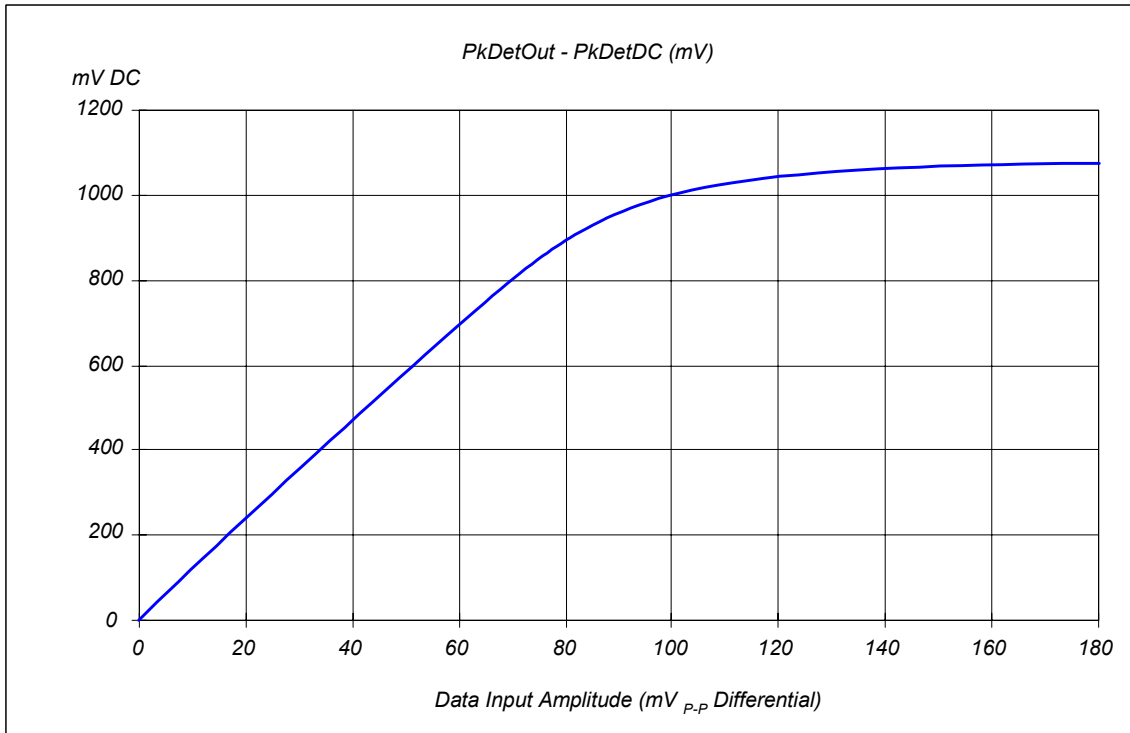
Differential output signals at DataOutP and DataOutN connect to pins OffOutP and OffOutN, respectively, via internal 10 k Ω resistors. These pins can be used to reduce output offset that might produce pulse width distortion. The offset sense outputs indicate any DC offset voltage between the differential outputs. They may be used in a feedback circuit to compensate for any internal voltage offset. The output of the offset compensation circuit may be applied to one or both of the input offset compensation pins: OffInP and OffInN.

Output Signal Peak Detection

The on-chip peak detector generates a DC voltage on PkDetOut, which is proportional to the input signal amplitude. The PkDetDC output is the DC reference voltage for the PkDetOut output signal. The difference between the PkDetOut and PkDetDC pins is a voltage, which is

approximately linearly proportional to the input signal amplitude. The relationship of PkDetOut-PkDetDC, as a function of the input signal amplitude, (differential, peak-to-peak) is illustrated in Figure 2.

Figure 2. Peak Detector Transfer Function Characteristics



Loss of Signal

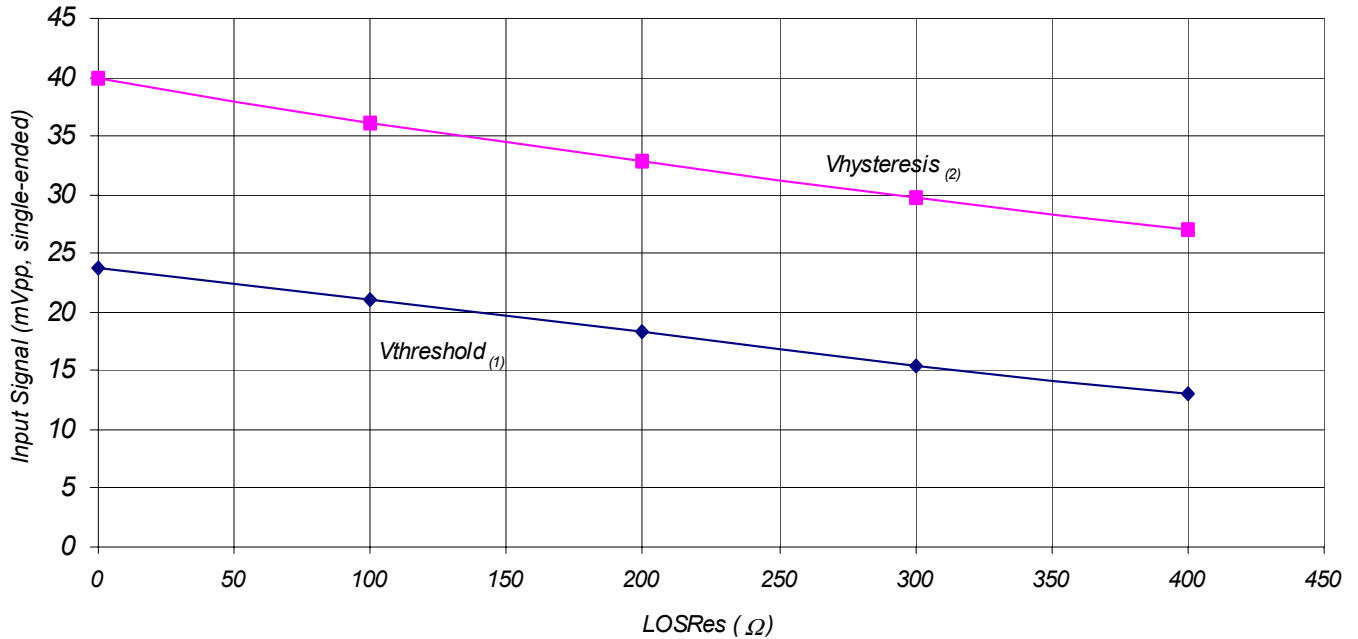
The LOS terminal is an open collector output providing an active high signal indicating a loss of signal (LOS) condition. The LOS terminal sinks 350 μ A when it is low (deasserted) and no current when it is high (asserted). It is possible to connect the LOS terminal to a supply voltage using an external resistor to establish a desired voltage logic level indicating LOS as described below.

The on-chip LOS circuit has built in hysteresis. To use the LOS function approximately 200 Ω needs to be connected between the LOSRes pin and ground.

LOS sinks 350 μ A when it is low (deasserted), and no current when it is high (asserted). It is an active high output. You can connect a resistor between 5 V or 3.3 V and the LOS pin. This can be used to establish output voltage levels as follows:

For a high level of 3.3 V and a low level of approximately 0.0 V, the swing is 3.3 V. When the output is low (not asserted) it sinks 350 μ A. The values: 3.3 V/350 μ A is 9.4 k Ω . Consequently, putting a 9.53 k Ω resistor between 3.3 V and the LOS terminal would give you a 3.3 V output when the signal is high and about 0.0 V when it is low.

Figure 3. Loss of Signal (LOS) Characteristic



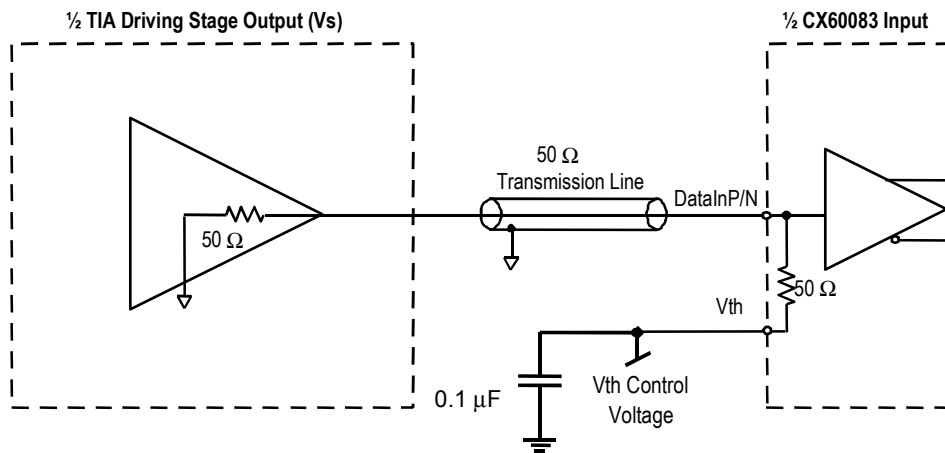
Note 1: With the LOS flag reset, V_{threshold} is defined as the input signal voltage, below which, the LOS flag becomes set.
 Note 2: If LOS flag is set V_{hysteresis} is defined as the input signal voltage above which the LOS flag becomes reset.

Input Voltage Range Determination

The input AC voltage in combination with the DC bias present at the DataIn pins should satisfy the input voltage range specifications according to the following condition: the voltage present at the input pins of the limiting amplifier (DataInP and/or DataInN) needs to fall between -1.0 V and +0.25 V. From Figure 1 it can be observed that the differential voltage present at the CX60083 data inputs is a combination of the voltage at V_{th} and the output level of the preamplifier driving the CX60083 data inputs.

Figures 4a and 4b show the relationship between the TIA output level and the V_{th} reference level to the voltage present at the CX60083 data input pins when the input is either DC- (Figure 4a) or AC- (Figure 4b) coupled. (Note the TIA source level is V_s when terminated into a 50 Ω load).

Figure 4a. CX60083 Input Value When DC-coupled

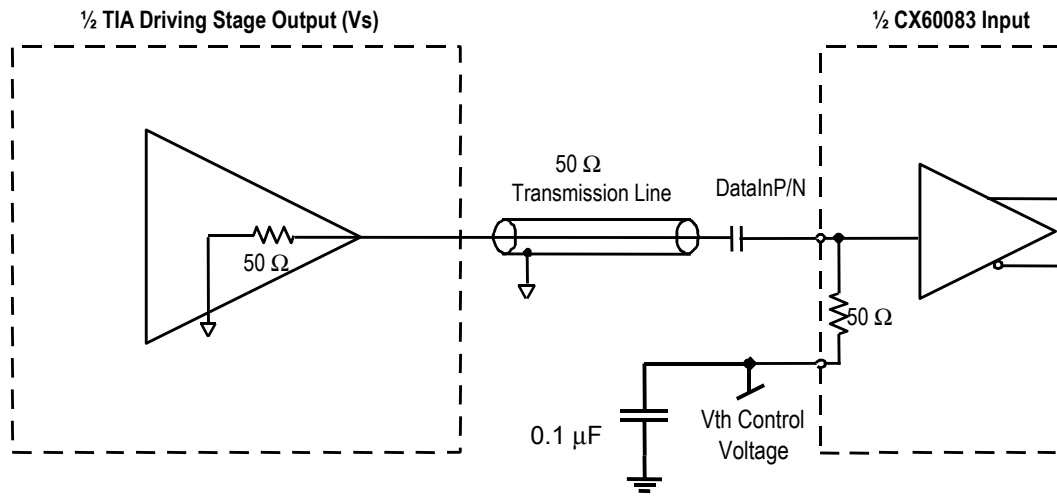


$$\text{DataInN/P} = \frac{V_{th}}{2} \pm V_s$$

$$-1.0 \text{ V} \leq \text{DataInN/P} \leq 0.25 \text{ V}$$

Observe that if V_{th} = 0 V (ground), then the DataInP/N level is simply V_s.

Figure 4b. CX60083 Input Value When AC-coupled



$$\text{DataInN/P} = V_{th} \pm V_s$$

$$-1.0 \text{ V} \leq \text{DataInN/P} \leq 0.25 \text{ V}$$

Vth Reference Value Determination

Referring to Figures 4a and 4b, for a preamplifier output signal of less than 250 mV_{PEAK}, Vth can generally be connected to ground. If the input signal is greater than 250 mV_{PEAK} (and less than 800 mV_{P-P}) then Vth will need to be connected to a negative voltage reference, the level of which, is calculated so that the sum of the AC peak signal and the DC Vth reference voltage ensures the voltage present at DataInP and DataInN input pins falls with the range -1.0 V and 0.25 V as shown in Figures 4a and 4b.

When driving the part with a single-ended input, the non-used CX60083 input terminal should be terminated in a manner similar to the input being driven: if the driven input is DC-coupled to the preamplifier, the non-used input should be DC terminated with 50 Ω. If the driven input is AC-coupled, then the non-used input should be AC-coupled to the 50 Ω termination. The termination voltage needs to be a potential equal to the common mode voltage seen at the driven input terminal (so that the driving signal swings equally above and below the non-used input).

When a DC reference is connected to Vth, it should be decoupled with a good quality high frequency capacitor ≥ 10 nF (if possible, 0.1 μF in parallel with 330 pF is suggested).

For more detailed information on interfacing to the CX60083 please refer to Application Note CX60083 AN1.

Electrical Specifications

Tables 2 through 5 list the CX60083 RF and DC electrical specifications, absolute maximum ratings and power requirements.

Table 2. RF Electrical Specifications (for die, see Note 8)

T_{case} = 0 °C to +85 °C, V_{ee} = -5.2 V ± 5%, Bit Rate = 9.95328 Gbps, input offset compensated for with DC servo loop and exposed paddle connected to ground.

| Parameter | Min | Typical | Max | Unit |
|---|------|---------|------|--------|
| Operating Temperature | 0 | — | 85 | °C |
| Input AC Voltage, Single-ended (1, 2) | 5 | — | 800 | mV |
| Input High Level (VIH) Voltage Range (3) | -1.0 | — | 0.25 | V |
| Input Low Level (VIL) Voltage Range (3) | -1.0 | — | 0.25 | V |
| Input Offset Voltage (without offset compensation) (4) | -5 | 0 | 5 | mV |
| Output Swing, Single-ended (when limiting) | 425 | 450 | 500 | mV p-p |
| Absolute Output Voltage Range, Single-ended (when limiting) | -0.6 | — | 0 | V |
| Output Rise/Fall Time (20% - 80%), input = 20 mV p-p differential (8) | — | 28 | 35 | ps |
| Small Signal Gain (single-ended to single-ended) (5, 7) | 32 | 39 | — | dB |
| Small Signal Gain at 10 GHz (single-ended to single-ended) (5, 7) | — | — | 40 | dB |
| Small Signal Gain Variation (7) | -2 | 0 | +2 | dB |
| Small Signal 3 dB Bandwidth (7) | 8.5 | 10.0 | 10.5 | GHz |
| Input and Output Return Loss (single-ended) 100 kHz – 5 GHz (6, 7) | — | — | -10 | dB |
| Input and Output Return Loss (single-ended) 5 GHz – 10 GHz (6, 7) | — | -10 | -5 | dB |
| Input and Output Return Loss (single-ended) 10 GHz (6, 7) | — | -10 | — | dB |
| Output Jitter (RMS), input = 1600 mV p-p differential (8) | — | 1.6 | 2.0 | ps |
| Output Jitter (RMS), input = 10 mV p-p differential (8) | — | 2.1 | 3.0 | ps |

Note 1: 1600 mV differential peak-to-peak input translates to 800 mV p-p for each signal (single-ended). See Figure 5.

Note 2: Output typically limits for inputs greater than 5 mV p-p single-ended. Smaller and larger signals meeting the VIH and VIL specifications may be input, but performance will be reduced.

Note 3: Signals exceeding 0.25V above ground but less than 0.5V above ground may be input, but performance will be reduced.

Note 4: End-of-life offset specification is ± 7 mV. For maximum sensitivity, a DC servo loop must be used (see Application Note CX60083 AN2).

Note 5: Unused input and output terminated 50 Ω to ground. Differential to differential gain is 6 dB greater.

Note 6: Return Loss measured with packaged part mounted on a characterization board with 50 Ω input and output traces and connectors.

Note 7: AC characteristics are established from characterization of packaged parts.

Note 8: While limited AC testing is done on each die, these characteristics are not guaranteed for die.

Figure 5. CX60083 Differential Input Voltage Definitions

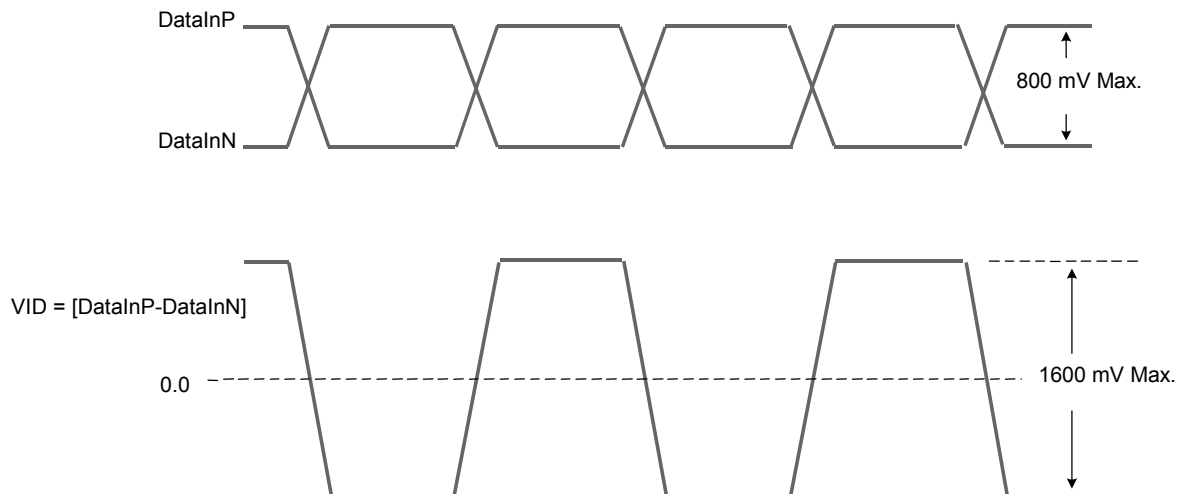


Table 3. DC Signal Electrical Specifications

Tcase = 0 °C to +85 °C, Vee = -5.2 V ± 5%, Bit rate = 9.95328 Gbps

| Parameter | Min | Typical | Max | Unit |
|---------------------|------|---------|-------------------|------|
| PkDetOut | -2.4 | — | -1.3 | V |
| PkDetDC | — | -2.4 | — | V |
| LOSOut | -2.3 | — | +6 ⁽¹⁾ | V |
| LOSRes | 50 | — | 500 | Ω |
| LOS Assert/Deassert | | 250 | | ns |

Note 1: Current sink output. Refer to the LOS subsection for description of voltage behavior.

Table 4. Absolute Maximum Ratings (no damage)

| Symbol | Item | Min | Max | Units |
|--------------------|-------------------------------------|------|------|-------|
| Vee | Supply Voltage | -7.0 | +0.5 | V |
| DataInP, DataInN | High Speed Input Signal | -1.0 | +0.5 | V |
| DataOutP, DataOutN | High Speed Output Signal | -1.0 | +0.5 | V |
| OffOutP, OffOutN | Offset Sense Output | -2.0 | +0.5 | V |
| OffInP, OffInN | Offset Control Input ⁽¹⁾ | -2.0 | +2.0 | V |
| Tst | Storage Temperature | -65 | +150 | °C |

Note 1: With Vth connected to ground ± 1 V, the offset control input range is ± 5 V.

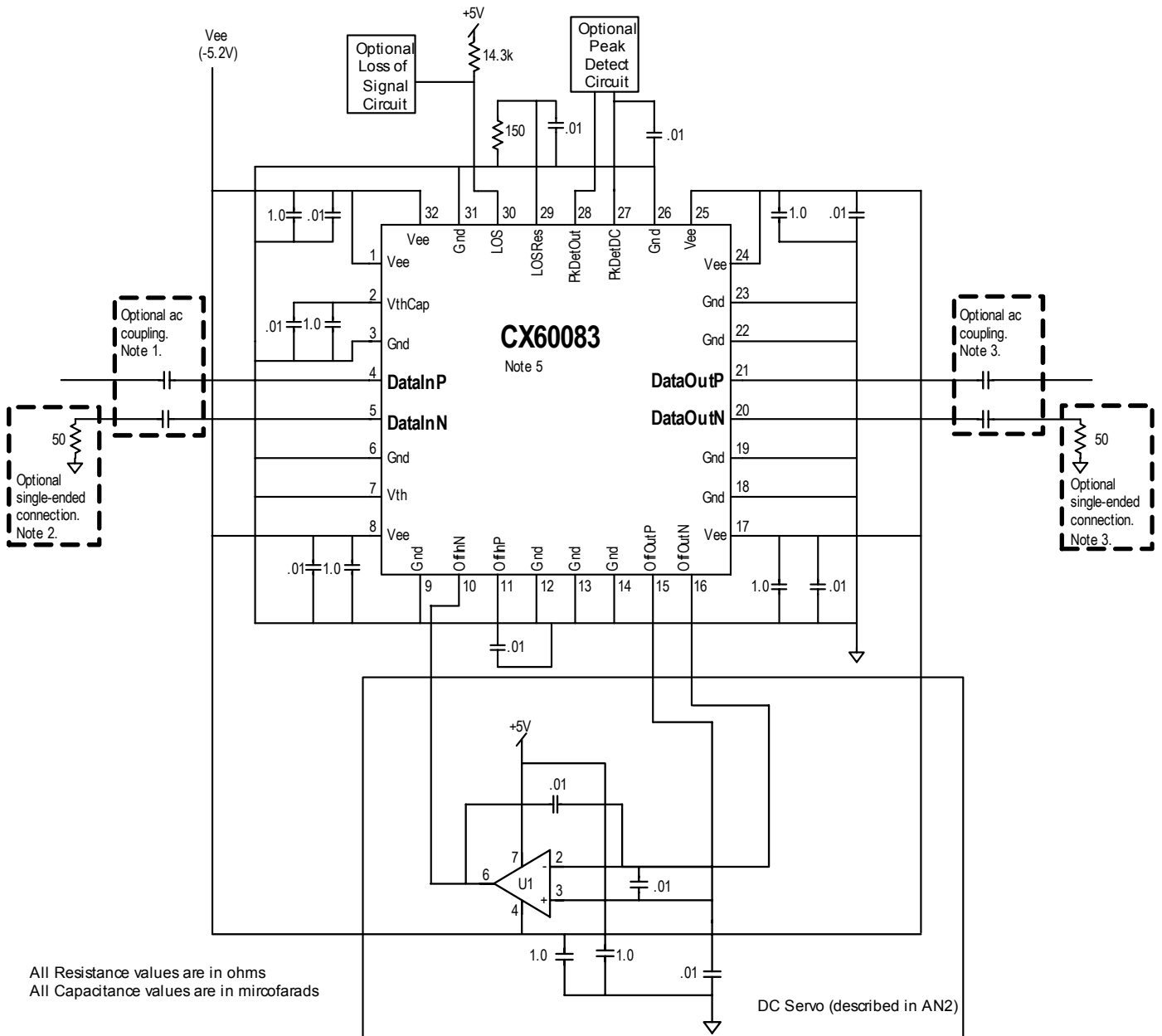
Table 5. Power DC Electrical Specifications

Tcase = 0 °C to +85 °C, Vee = -5.2 V ± 5%

| Symbol | Item | Min | Typical | Max | Units |
|--------|-------------------------|-----|---------|-----|-------|
| Iee | Supply Current | — | 125 | 150 | mA |
| Pdiss | Total Power Dissipation | — | 650 | 825 | mW |

CX60083 Applications Diagram

Figure 6. CX60083 Applications Diagram



Notes:

1. The input(s) may be ac-coupled to the pre-amplifier using a good high frequency capacitor.
2. If driven single-ended by the pre-amplifier, the unused input must be terminated in 50 ohms. If a single-ended ac-coupled connection to the preamplifier, the unused input must be ac-coupled to a 50 ohm termination.
3. The output(s) may be ac-coupled to the CDR/receiver using a good high frequency capacitor.
4. If an output is connected single-ended to the receiver, the unused output must be terminated in 50 ohms. If a single output is ac-coupled to the receiver, the unused output must be ac-coupled to a 50 ohm termination.
5. Package bottom must be attached to PCB ground using conductive epoxy or solder.

CX60083 Package Pin Description

Figure 7 illustrates the pin number versus function configuration. Table 6 lists the pin assignments and function names. Figure 8 illustrates the package pin dimensions.

Figure 7. CX60083 Pin Configuration (TQFP Package)

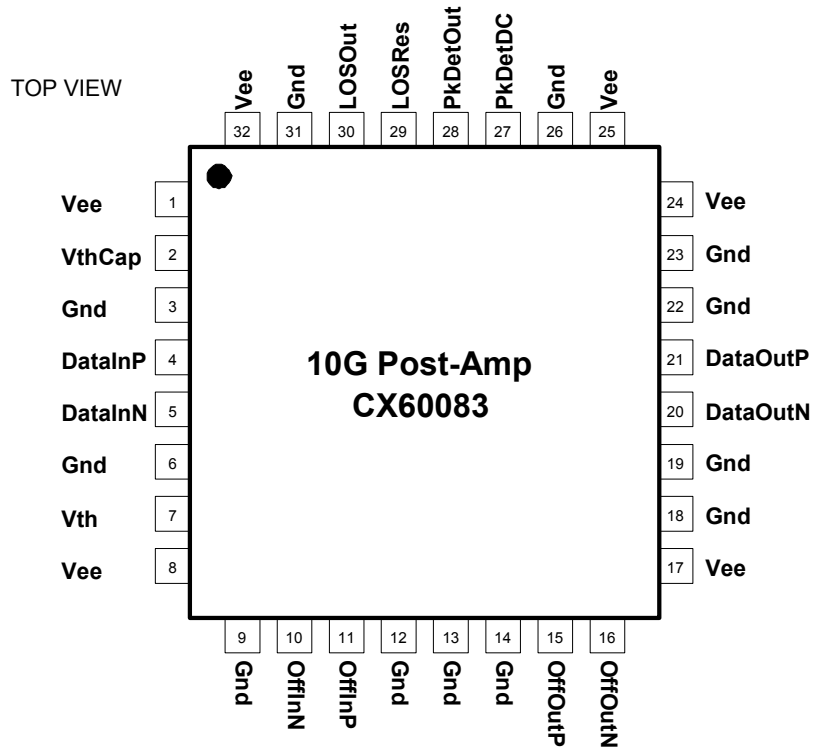
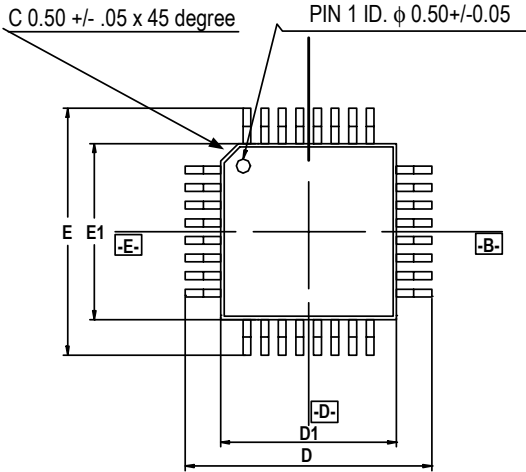


Table 6. Package Pin Assignments

| Package Pin | Signal |
|---|----------|
| 2 | VthCap |
| 4 | DataInP |
| 5 | DataInN |
| 7 | Vth |
| 10 | OffInN |
| 11 | OffInP |
| 15 | OffOutP |
| 16 | OffOutN |
| 20 | DataOutN |
| 21 | DataOutP |
| 27 | PkDetDC |
| 28 | PkDetOut |
| 29 | LOSRes |
| 30 | LOS |
| 1, 8, 17, 24, 25, 32 | Vee |
| 3, 6, 9, 12, 13, 14, 18, 19, 22, 23, 26, 31 | Gnd |
| EP | Gnd |

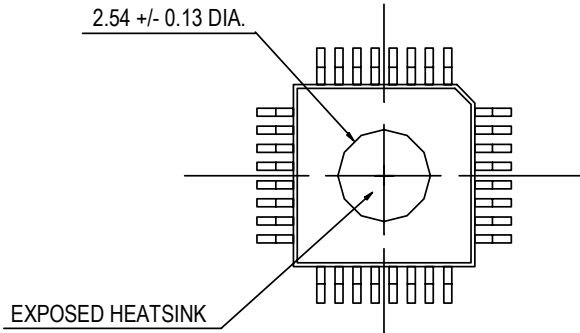
Figure 8. CX60083 Package Dimensions

Note: All dimensions are in millimeters.

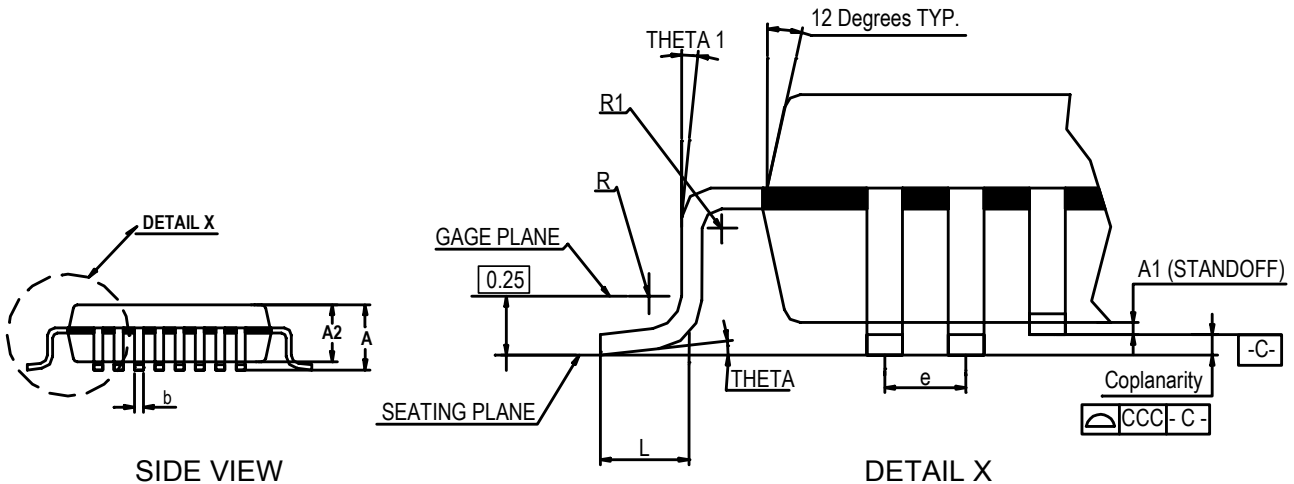


TOP VIEW

| PACKAGE DIMENSIONS | | |
|--------------------|--------------------|-------------|
| LETTER | DIMENSION | TOLERANCE |
| A | 1.60 | MAX. |
| A1 | .10 | \pm .05 |
| A2 | 1.40 | \pm .05 |
| D | 7.00 | \pm .20 |
| D1 | 5.00 | \pm .10 |
| E | 7.00 | \pm .20 |
| E1 | 5.00 | \pm .10 |
| L | .6 | +0.15/-0.10 |
| e | .5 | TYP. |
| b | .22 | \pm .05 |
| THETA | 0° - 7° | |
| THETA 1 | 6° | \pm 4° |
| R | .08 MIN./0.20 MAX. | |
| R1 | .08 MIN. | |
| ccc | .08 | MAX. |



BOTTOM VIEW



SIDE VIEW

DETAIL X

CX60083 Die Information and Pad Configuration Description

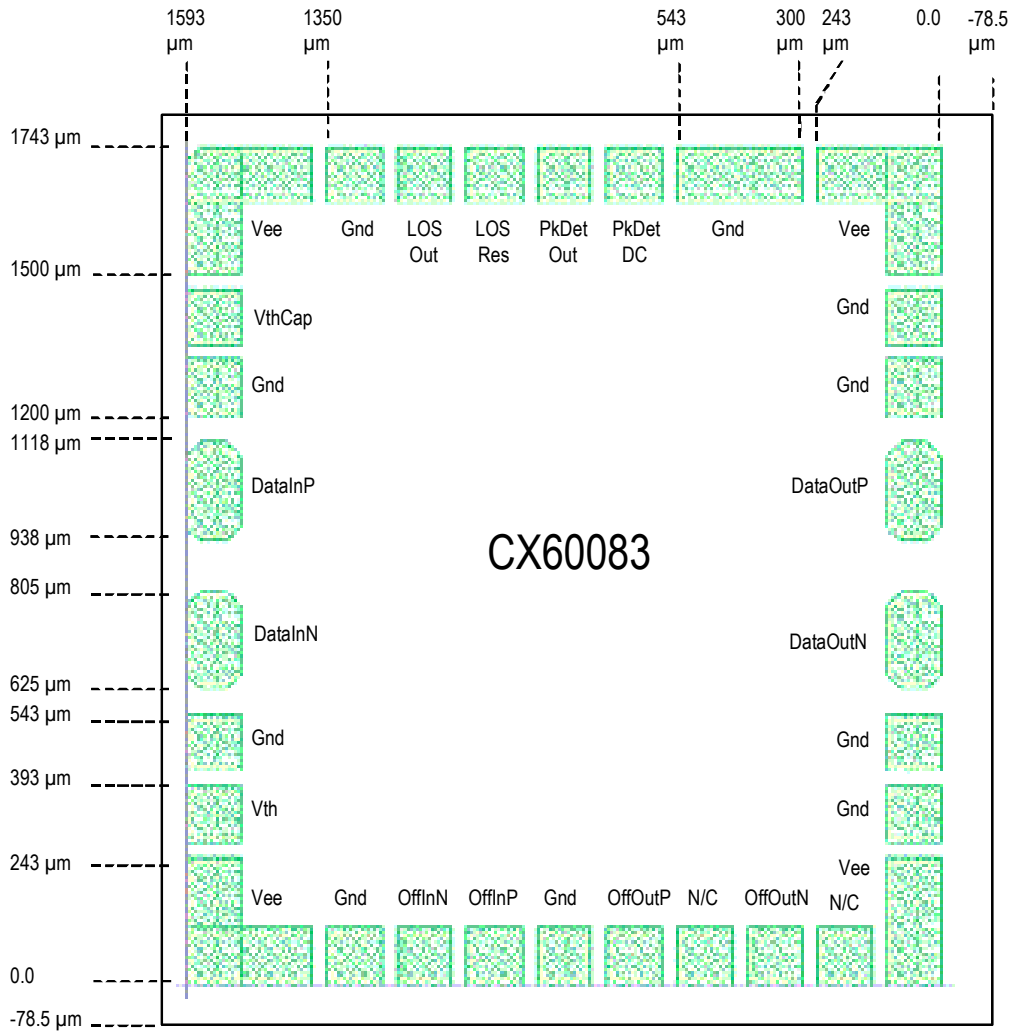
Table 7. Die Information

| Item | Value | Item | Value |
|-----------------------|--------------------|-----------------------|---|
| Product Availability | Die in Waffle Pack | Backside Bias | Most positive potential (0V) using conductive epoxy |
| Process Technology | GaAs | Bond Pad Metalization | Au |
| Die Thickness | 178 ± 13 μm | Pad pitch | 150 μm ⁽¹⁾ |
| Die Size | 1900 μm by 1750 μm | Pad size | 120 μm X 120 μm |
| Die Passivation | Silicon nitride | Opening | 93 μm X 93 μm ⁽²⁾ |
| Die Backside Material | GaAs | | |

Note 1: Others as indicated below.

Note 2: Other pad size indicated below.

Figure 9. CX60083 Die Pad Configuration Drawing



Note: Pad sizes show exposed metal area only.

Ordering Information

| Name | Number | Package Data |
|-------------------------------------|------------|-------------------------|
| 10 Gbps Packaged Limiting Amplifier | CX60083-15 | 32-terminal EdQuad TQFP |
| 10 Gbps Limiting Amplifier Die | CX60083-2A | Die in waffle pack |

Revision History

| Revision | Date | Comments |
|---------------|----------|---|
| CLA10_rev1_2 | 10/13/99 | CLA10 revisions |
| CX8610LA_rev1 | 1/20/00 | Original CX8610LA issue |
| CX60083 | 2/1/00 | Original CX60083 issue; added functional description text |
| CX60083v2a | 2/18/00 | Added illustrations and supporting text to functional description |
| CX60083v2b | 2/10/00 | Reorganized sequence of functional description and specification tables; added System Block Diagram |
| CX60083v2c | 5/8/00 | Transferred descriptive text from Note 2 in Table 3, RF Electrical Specifications to paragraph following table |
| CX60083v2d | 5/12/00 | Internal document |
| CX60083v2e | 6/19/00 | Changed header and footer text; performed QA check and edits; edited Figure 1, System Block Diagram |
| CX60083v2f | 8/8/00 | Modified Table 1 |
| CX60083v2g | 9/15/00 | Added Figure 3 |
| CX60083v3 | 11/28/00 | Technical edits |
| CX60083v4 | 02/26/01 | Technical edits |
| CX60083v4a | 03/12/01 | Made CX60083-15P from CX60083v4; added review comments; made changes to Figure 2, Table 2, and Table 3 (return losses and bandwidth specifications) |
| CX60083v4b | 05/4/01 | Updated Table 2; became figure 2; updated figure and table references; added LOS assert/de-assert time information; added offset specification note; added in die information; removed P designation; general edits |
| CX60083v5 | 01/23/02 | Clarified jitter specification conditions. Update supply and output p-p numbers. Clarified input sensitivity statements. Updated LOS current sink value. Made more explicit the proper connection of the package bottom. Add applications diagram. Add die information and specifications |
| CX60083v5b | 02/20/02 | Added notes 3 and 7, modified note 2, moved other notes down. Added Table 7 |
| CX60083v6 | 04/12/02 | Corrected pin numbers on Applications Diagram (Fig. 6). Added -2A designator to header. Updated sales office information. |

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