GS9064 SD SDI
Adaptive Cable Equalizer

DATA SHEET

KEY FEATURES

- **SMPTE 259 and SMPTE 344 compliant**
- **automatic cable equalization**
- **supports DVB-ASI at 270Mb/s**
- **typical maximum equalized length of Belden 1694A cable at 270Mb/s is 350m**
- **50Ω differential output (with internal 50Ω pull-ups)**
- **cable length indicator**
- **output mute based on maximum cable length adjust or manual override**
- **Pb-free and Green**
- **single 3.3V power supply operation**
- **operating temperature range: 0°C to +70°C**
- **pin compatible with HDLINX™ II GS1524 multirate SDI adaptive cable equalizer**

APPLICATIONS

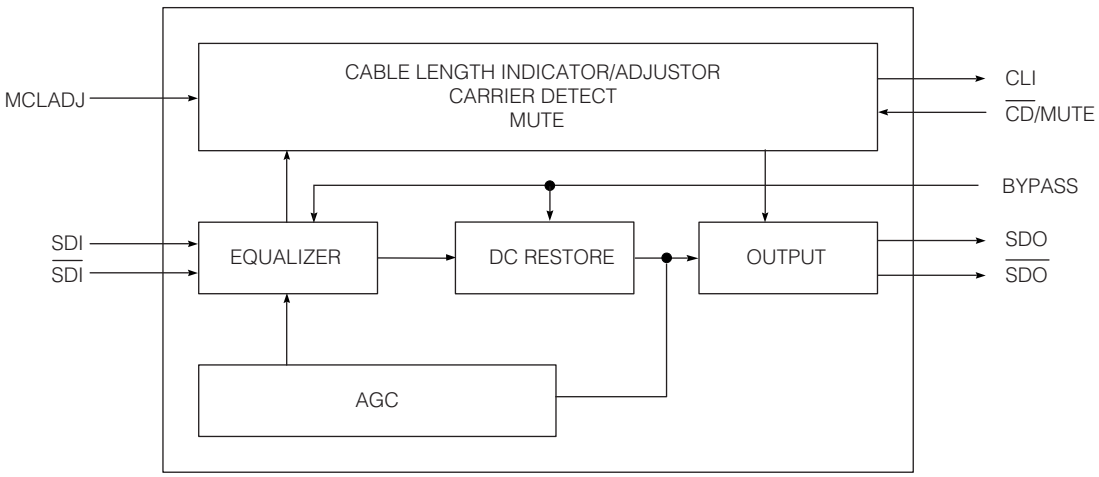
- SMPTE 259M Coaxial Cable Serial Digital Interfaces

DESCRIPTION

The GS9064 is a second-generation high-speed bipolar integrated circuit designed to equalize and restore signals received over 75Ω co-axial cable at data rates from 143Mb/s up to 540Mb/s. The GS9064 is designed to support SMPTE 344M and SMPTE 259M and is optimized for performance at 270Mb/s.

The GS9064 features DC restoration to compensate for the DC content of SMPTE pathological test patterns, and incorporates a Cable Length Indicator (CLI) that provides a linear indication of the amount of cable being equalized.

A voltage programmable mute threshold (MCLADJ) is included to allow muting of the GS9064 output when a selected cable length is reached. This feature allows the GS9064 to distinguish between low amplitude SDI signals and noise at the input of the device. The $\overline{CD}$/MUTE pin provides an indication of the GS9064 mute status in addition to functioning as a mute control input. The output of the GS9064 may be forced to an active or a mute condition by applying a voltage to the $\overline{CD}$/MUTE pin.



GS9064 FUNCTIONAL BLOCK DIAGRAM

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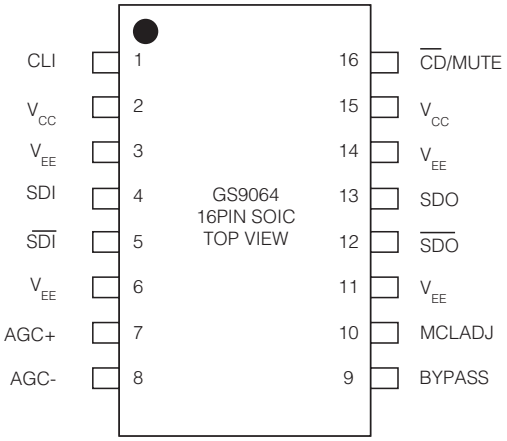
1. PIN OUT

1.1 PIN ASSIGNMENT



1.2 PIN DESCRIPTIONS

PIN NUMBER	NAME	TYPE	DESCRIPTION
1	CLI	Output	CABLE LENGTH INDICATOR An analog voltage proportional to the cable length connected to the serial digital input. NOTE: CLI is recommended for data rates up to 360 Mb/s only.
2, 15	V_{CC}	Input Power	Most positive power supply connection. Connect to +3.3V.
3, 6, 11, 14	V_{EE}	Input Power	Most negative power supply connection. Connect to ground.
4, 5	SDI, $\overline{SDI}$	Input	Serial digital differential inputs.
7, 8	AGC+, AGC-	Passive Input	External AGC capacitor. Should be set to 1µF.
9	BYPASS	Input	Forces the CORE stage and the DC RESTORE stage into bypass mode when HIGH. No equalization occurs in this mode.
10	MCLADJ	Input	MAXIMUM CABLE LENGTH ADJUST Adjusts the approximate maximum amount of cable to be equalized (from 0m to the maximum cable length). The output is muted (latched to the last state) when the maximum cable length is achieved. NOTE: MCLADJ is recommended for data rates up to 360 Mb/s only.
12, 13	$\overline{SDO}$, SDO	Output	Equalized serial digital differential outputs.
16	$\overline{CD}$/MUTE	Input / Output	MUTE INDICATOR-CONTROL / CARRIER DETECT OUTPUT: the output voltage drops to below 1.2V when the carrier is present and the data outputs are active. INPUT: if the $\overline{CD}$/MUTE pin is tied to ground, the data output will never mute and the MCLADJ setting is overwritten. If the $\overline{CD}$/MUTE pin is tied to VCC, the data outputs will always mute and the MCLADJ setting is overwritten.

2. ELECTRICAL CHARACTERISTICS

2.1 ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE
Supply Voltage	-0.5V to +3.6 V_{DC}
Input ESD Voltage	500V
Storage Temperature Range	-50°C< T_s < 125°C
Input Voltage Range (any input)	-0.3 to (V_{CC} + 0.3)V
Operating Temperature Range	0°C to 70°C
Power Dissipation	300mW
Lead Temperature (soldering, 10 sec.)	260°C

2.2 DC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V , V_{EE} = 0V , T_A = 0°C to 70°C, 270Mb/s, unless otherwise shown

PARAMETER	SYMBOL	CONDITIONS	MIN	TYPICAL	MAX	UNITS	TEST LEVEL	NOTES
Supply Voltage	V_{CC}		3.1	3.3	3.5	V	1	-
Power Consumption	P_D	T_A = 25°C	-	265	-	mW	5	-
Supply Current	I_S	T_A = 25°C	-	80	-	mA	1	-
Input Common Mode Voltage	V_{CMIN}		-	1.75	-	V	10	-
Output Common Mode Voltage	V_{CMOUT}		-	V_{CC} - ΔV_{SDO}/2	-	mV	7	-
CLI DC Voltage		Cable length = 0m	-	2.5	-	V	1	-
		No signal (max cable length)	-	1.9	-	V	7	-
Floating MCLADJ DC Voltage			-	1.3	-	V	7	-
MCLADJ Range		0m to max cable length	-	0.69	-	V	7	-
$\overline{CD}$/Mute Output Voltage	$V_{\overline{CD}/Mute(OH)}$	Carrier not present	2.6	-	-	V	1	-
	$V_{\overline{CD}/Mute(OL)}$	Carrier present	-	-	1.2		1	-
$\overline{CD}$/Mute Input Voltage Required to Force Outputs to Mute	$V_{\overline{CD}/Mute)}$	Min to Mute	3.0	-	-	V	7	-
$\overline{CD}$/Mute Input Voltage Required to Force Outputs to Activate	$V_{\overline{CD}/Mute}$	Max to Activate	-	-	2.0	V	7	-

TEST LEVELS

1. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges.
2. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges using correlated test.
3. Production test at room temperature and nominal supply voltage.
4. QA sample test.
5. Calculated result based on Level 1, 2, or 3.
6. Not tested. Guaranteed by design simulations.
7. Not tested. Based on characterization of nominal parts.
8. Not tested. Based on existing design/characterization data of similar product.
9. Indirect test.
10. Wafer Probe

2.3 AC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V , V_{EE} = 0V , T_A = 0°C to 70°C, 270Mb/s, unless otherwise shown

PARAMETER	SYMBOL	CONDITIONS	MIN	TYPICAL	MAX	UNITS	TEST LEVEL	NOTES
Serial Input Data Rate	DR_{SDI}	EQ active	143	-	540	Mb/s	6	-
Input Swing	ΔV_{SDI}	Differential, T_A =25°C Cable length = 0m	720	800	950	mV_{p-p}	1	-
Output Swing	ΔV_{SDO}	Differential, 50 ohm load, T_A =25°C	-	750	-	mV_{p-p}	1	-
Maximum Equalized Cable Length		270Mb/s, Belden 8281 0.20UI output jitter EQ Pathological	-	280	-	m	7	-
		540Mb/s, Belden 8281 0.20UI output jitter EQ Pathological	-	180	-	m	7	-
Output Rise/Fall Time	t_r, t_f	20% - 80%	-	80	220	ps	1	-
Mismatch in Rise/Fall Time			-	-	30	ps	1	-
Duty Cycle Distortion			-	-	100	ps	7	-
Overshoot			-	-	10	%	1	-
Input Return Loss	IRL		15	-	-	dB	7	-

TEST LEVELS

1. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges.
2. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges using correlated test.
3. Production test at room temperature and nominal supply voltage.
4. QA sample test.
5. Calculated result based on Level 1, 2, or 3.
6. Not tested. Guaranteed by design simulations.
7. Not tested. Based on characterization of nominal parts.
8. Not tested. Based on existing design/characterization data of similar product.
9. Indirect test.
10. Wafer Probe

2.4 INPUT/OUTPUT CIRCUITS

All resistors in ohms, all capacitors in farads, unless otherwise shown.

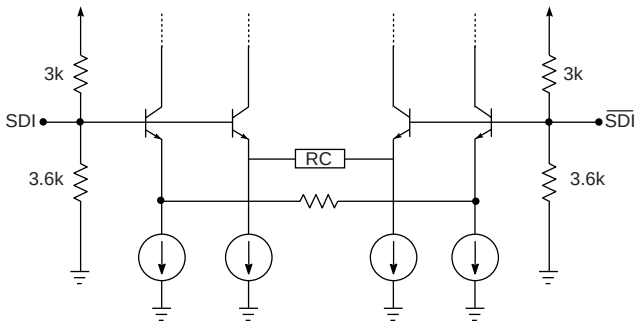


Figure 1 Input Equivalent Circuit

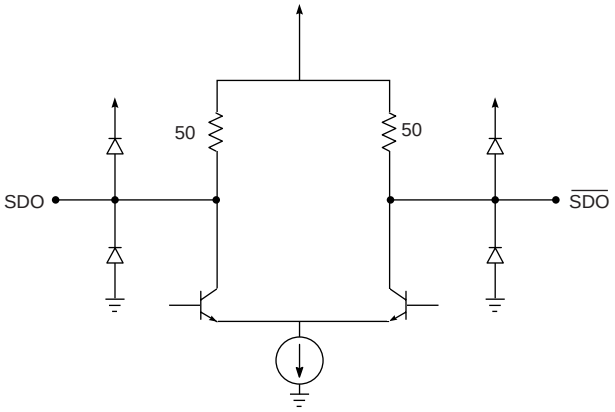


Figure 4 Output Circuit

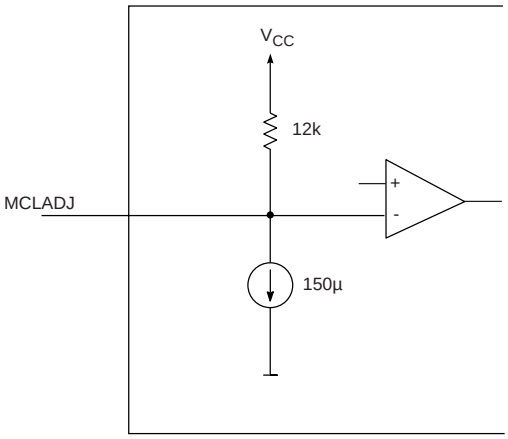


Figure 2 MCLADJ Equivalent Circuit

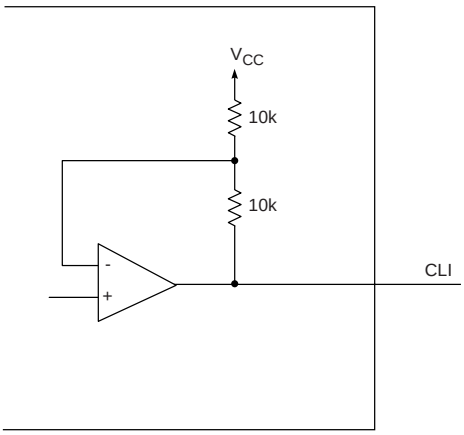


Figure 5 CLI Output Circuit

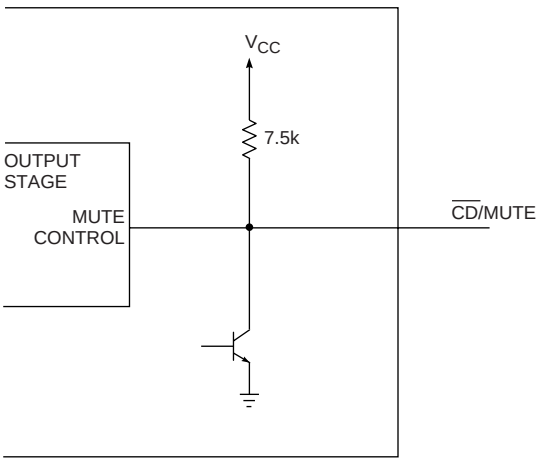


Figure 3 $\overline{CD}$/MUTE Circuit

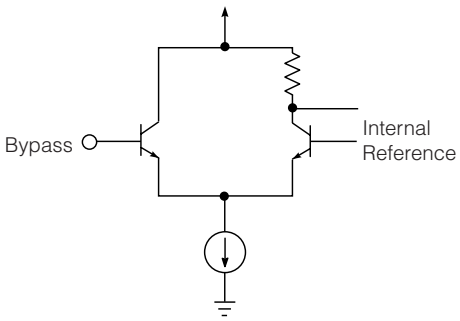


Figure 6 Bypass Circuit

2.5 TYPICAL PERFORMANCE CURVES

All resistors in ohms, all capacitors in farads, unless otherwise shown.

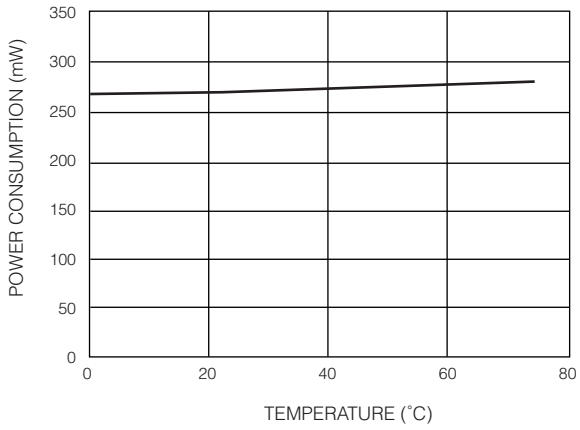


Figure 7 Power Consumption

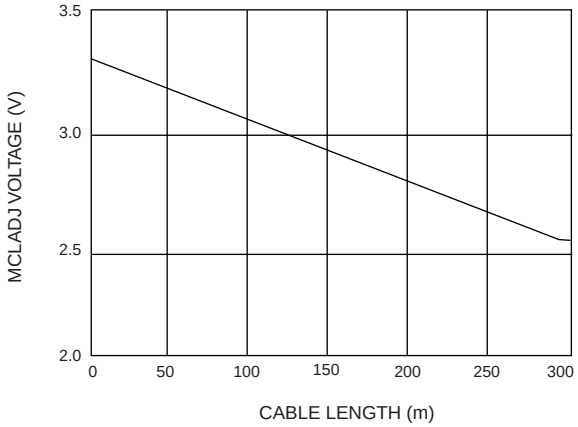


Figure 10 MCLADJ Input Voltage vs 1694A Cable Length, 270Mb/s

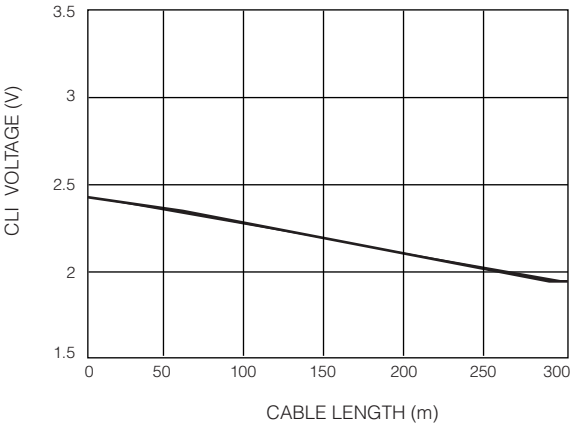


Figure 8 CLI Voltage vs 8281 Cable Length, 270Mb/s

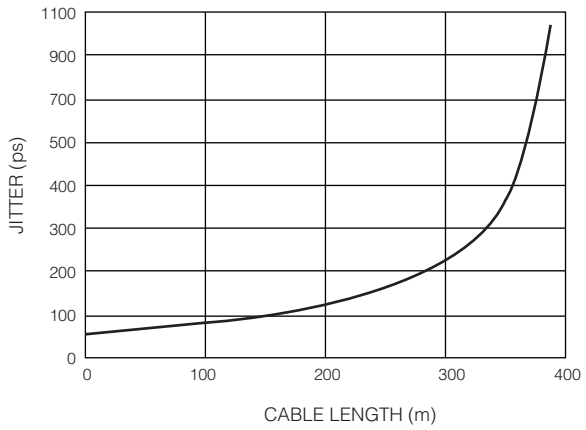


Figure 11 Typical Peak-to-Peak Jitter, PRN2^{23}-1, 1694A, 270Mb/s

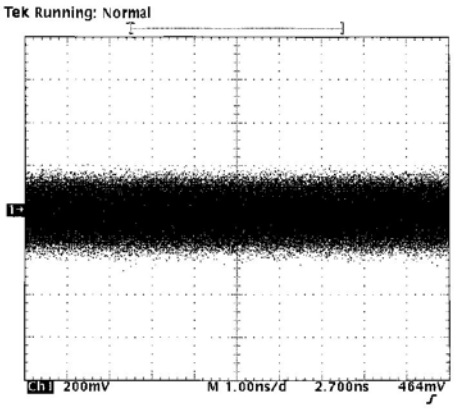


Figure 9 Input 8281, 280m, 270Mb/s

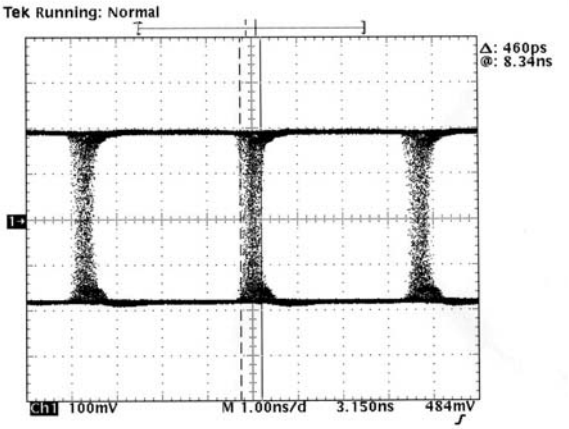


Figure 12 Output 8281, 280m, 270Mb/s

3. DETAILED DESCRIPTION

The GS9064 is a high speed bipolar IC designed to equalize SD serial digital signals. The device can typically equalize 350 meters of Belden 1694A cable at 270Mb/s. Powered from a single +3.3V or -3.3V power supply, the device consumes approximately 240mW of power.

3.1 SERIAL DIGITAL INPUT

The SD serial digital input signal may be connected to the input pins (SDI/$\overline{\text{SDI}}$) in either a differential or single ended configuration. AC coupling of the inputs is recommended, as the SDI and $\overline{\text{SDI}}$ inputs are internally biased at approximately +1.8 volts.

3.2 AUTOMATIC CABLE EQUALIZATION

The input signal passes through a variable gain equalizing stage whose frequency response closely matches the inverse of the cable loss characteristic. In addition, the variation of the frequency response with control voltage imitates the variation of the inverse cable loss characteristic with cable length.

The edge energy of the equalized signal is monitored by a detector circuit which produces an error signal corresponding to the difference between the desired edge energy and the actual edge energy. This error signal is integrated by both an internal and an external AGC filter capacitor providing a steady control voltage for the gain stage. As the frequency response of the gain stage is automatically varied by the application of negative feedback, the edge energy of the equalized signal is kept at a constant level which is representative of the original edge energy at the transmitter.

The equalized signal is also DC restored, effectively restoring the logic threshold of the equalized signal to its correct level independent of shifts due to AC coupling. The digital output signals have a nominal voltage of 750mV$_{pp}$ differential, or 375mV$_{pp}$ single ended when terminated with 50Ω as shown below in Figure 13.

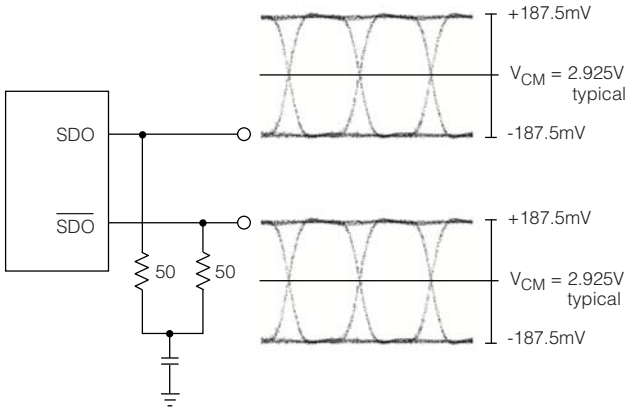


Figure 13 Typical Output Voltage Levels

3.3 CABLE LENGTH INDICATION & CARRIER DETECT/MUTE

The GS9064 incorporates an analog cable length indicator (CLI) output and a programmable threshold output mute (MCLADJ). In addition, a multi-function $\overline{\text{CD}}$/MUTE pin allows control of the GS9064 MUTE functionality for SD inputs.

3.3.1 Cable Length Indicator

The voltage output of the CLI pin is a representation of the amount of cable present at the inputs of the device. Figure 8 shows the CLI voltage versus cable length (signal strength). At 270Mb/s with no cable length and 800mV input signal levels, the CLI output voltage is approximately 2.5V. As the cable length is increased, the CLI voltage decreases, thereby providing an approximate correlation between the CLI voltage and cable length

3.3.2 Programmable Mute Threshold

A voltage programmable mute threshold (MCLADJ) is included to allow muting of the GS9064 output when a selected cable length is reached. This feature allows the device to distinguish between low amplitude SDI signals and noise at its input.

Figure 10 shows the relationship between the voltage applied to the MCLADJ pin and the input cable length accepted by the GS9064. For consistent accurate results this may need to be calibrated for each device. The MCLADJ pin may be left unconnected for applications where output muting is not required.

This feature has been designed for use in applications such as routers where signal crosstalk and circuit noise cause the equalizer to output erroneous data when no input signal is actually present. The use of a Carrier Detect function with a fixed internal reference does not solve this problem since the signal to noise ratio on the circuit board could be significantly less than the default signal detection level set by the on-chip reference.

NOTE: MCLADJ and CLI are only recommended for data rates up to 360 Mb/s.

3.3.3 Carrier Detect/Mute

Applying a HIGH INPUT to the $\overline{\text{CD}}$/Mute pin forces the GS9064 outputs to a muted condition. See the DC Electrical Characteristics table for voltage levels. In this condition the outputs are latched to the last logic level present at the output to avoid signal crosstalk.

Applying a LOW INPUT to the $\overline{\text{CD}}$/Mute pin will force the GS9064 outputs to remain active regardless of input cable length or the voltage applied to the MCLADJ pin. See the DC Electrical Characteristics table for voltage levels.

When used as an OUTPUT, the $\overline{CD}$/Mute pin will provide an indication of the output mute status. The $\overline{CD}$/Mute voltage will fall to below 1.2V when the carrier is present and the data outputs are active.

NOTE: The $\overline{CD}$/Mute pin is not functional in BYPASS mode.

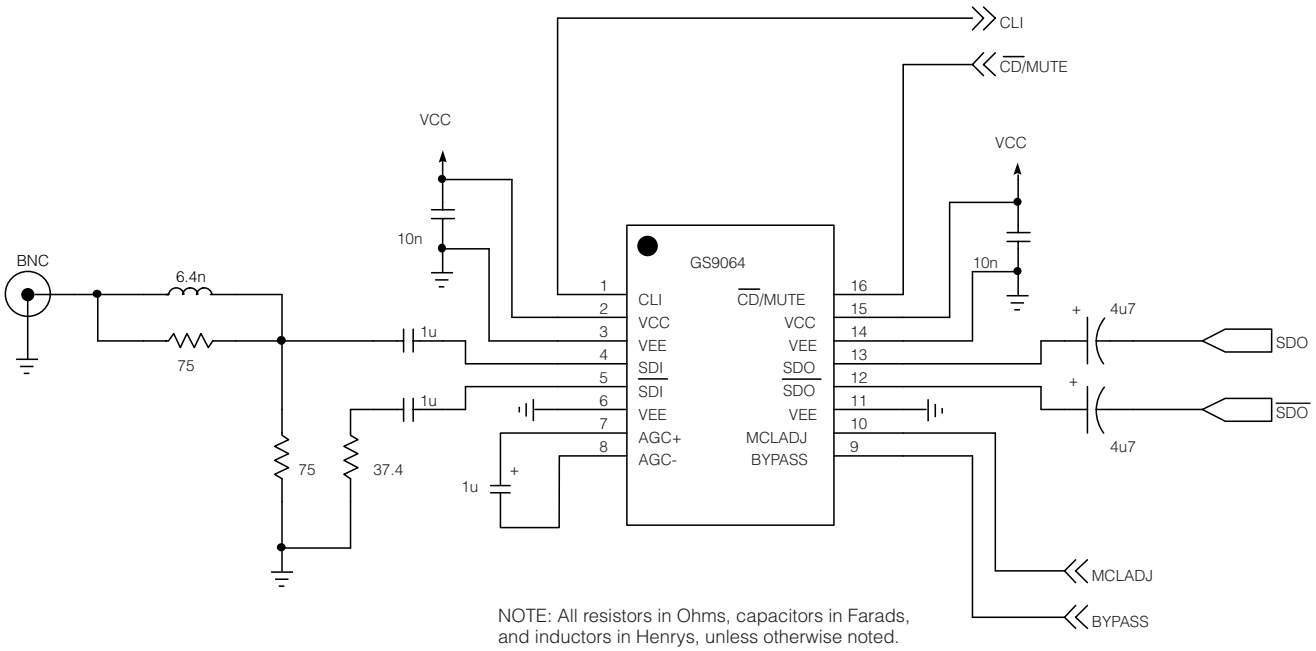
4. APPLICATION REFERENCE DESIGN

4.1 PCB LAYOUT

An FR-4 dielectric can be used, however, controlled impedance transmission lines are required for PCB traces longer than approximately 1cm. Note the following PCB artwork features used to optimize performance:

1. The PCB ground plane is removed under the GS9064 input AND output components to minimize parasitic capacitance.
2. High speed traces are curved to minimize impedance changes.

4.2 TYPICAL APPLICATION CIRCUIT



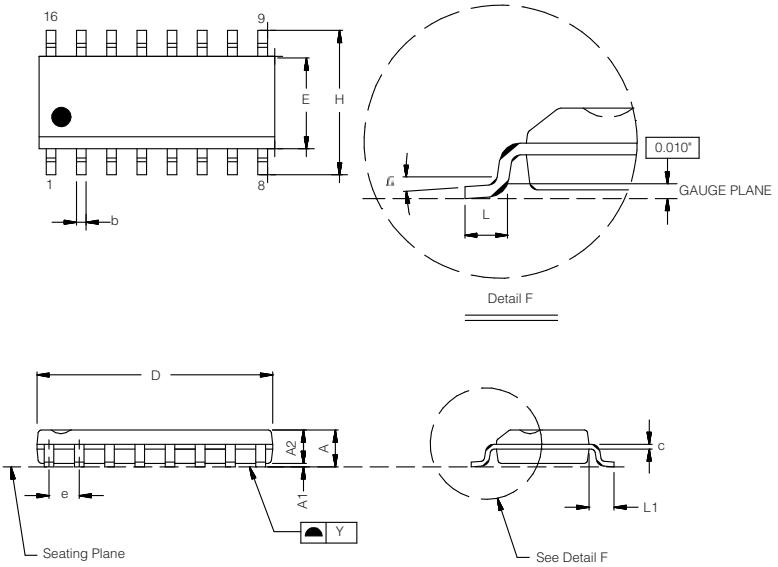
NOTE: All resistors in Ohms, capacitors in Farads, and inductors in Henrys, unless otherwise noted.

5. REFERENCES

Compliant with SMPTE 259M and SMPTE 344.

6. PACKAGE & ORDERING INFORMATION

6.1 PACKAGE DIMENSIONS



* CONTROLLING DIMENSION: MM

Symbol	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.35	1.63	1.75	0.053	0.064	0.069
A1	0.10	0.15	0.25	0.004	0.006	0.010
A2	1.30	1.40	1.50	0.051	0.055	0.059
b	0.33	0.41	0.51	0.013	0.016	0.020
c	0.19		0.25	0.007		0.010
D	9.80	9.91	10.01	0.386	0.390	0.394
E	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.50	
H	5.80	6.00	6.20	0.228	0.236	0.244
L	0.40	0.64	1.27	0.016	0.025	0.050
L1		1.07			0.042	
Y			0.10			0.004
ɑ	0°		8°	0°		8°

16 PIN SOIC

6.2 ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE RANGE	Pb-FREE AND GREEN
GS9064-CKD	16 pin SOIC	0°C to 70°C	No
GS9064-CKDE3	16 pin SOIC	0°C to 70°C	Yes

7. REVISION HISTORY

VERSION	ECR	DATE	CHANGES AND/OR MODIFICATIONS
A	120607	July 2002	New Document
B	125774	July 2002	Added detailed block descriptions and initial applications information.
C	126688	September 2002	Change packaging from LGA to SOIC for pin compatibility with the GS1524.
0	127023	December 2002	Upgrade document to Preliminary Data Sheet and edit AC/DC Characteristics to match current design specification limits.
1	128542	June 2003	Upgrade document to Data Sheet. Power number corrected.
2	133975	June 2004	Added lead-free and green information.

DOCUMENT IDENTIFICATION
DATA SHEET
The product is in production. Gennum reserves the right to make changes at any time to improve reliability, function or design, in order to provide the best product possible.

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