TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

JT6B03-AS

DOT MATRIX LCD CONTROLLER AND DRIVER LSI

The JT6B03-AS is a dot matrix LCD controller that realizes low power and high speed using CMOS silicon gate technology. This driver can drive a dot matrix LCD under 4-bit or 8-bit MPU control, and can displays alphanumerics, kana characters and symbols. It has all the functions to drive the dot matrix LCD. Therefore, the JT6B03-AS can constitute a minimal LCD drive and control system. The JT6B03-AS can generate up to 80 characters using an expansion driver (e.g. T6A41, T6A92).

FEATURES

- Built-in controller for character-type LCD (character fonts : 5×7, 5×10).
- Direct interface with MPU (4-bit or 8-bit interface)
- Bus interface timing : 2 MHz max
- Display data RAM : 80×8 bits (80 characters max)
- Character generator ROM : 12000bits (5×10×240)

  Character font ..... 5×10 dots×240 characters
- Character generator RAM : 64×8 bits

  Character font ..... ① 5×8 dots : 8 characters
  Character font ..... ② 5×11 dots : 4 characters
- Both the display data and character generator RAMs readable by MPU
- Built-in LCD driver circuit

  104-output column driver
  16-output row driver
- Selectable duty factor

  1/8 duty : (5×7 dots + cursor)×1 line
  1/11 duty : (5×10 dots + cursor)×1 line
  1/16 duty : (5×7 dots + cursor)×2 lines
- Built-in power-on reset circuit
- Numerous functions

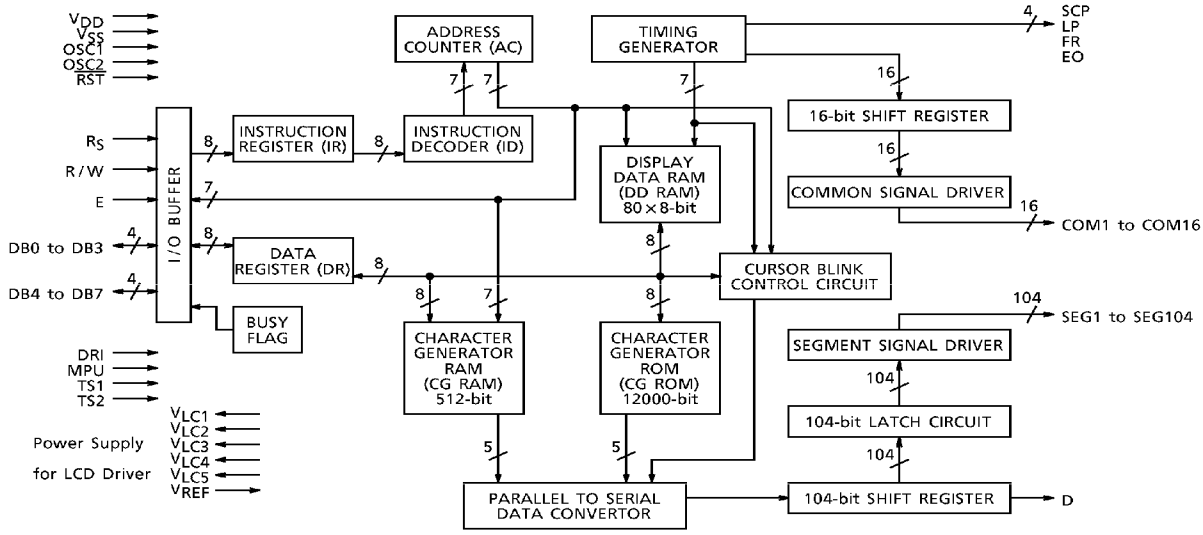
  Display clear, Cursor home, Display ON/OFF, Cursor ON/OFF, Display character blink, Display shift, Cursor shift

NUMBER OF CHARACTERS (CHARACTER × LINE)	EXTENSION COLUMN DRIVER	
	T6A41 (64-OUTPUT)	T6A92 (80-OUTPUT)
20×1	—	—
80×1	5 pcs	4 pcs
20×2	—	—
40×2	2 pcs	2 pcs

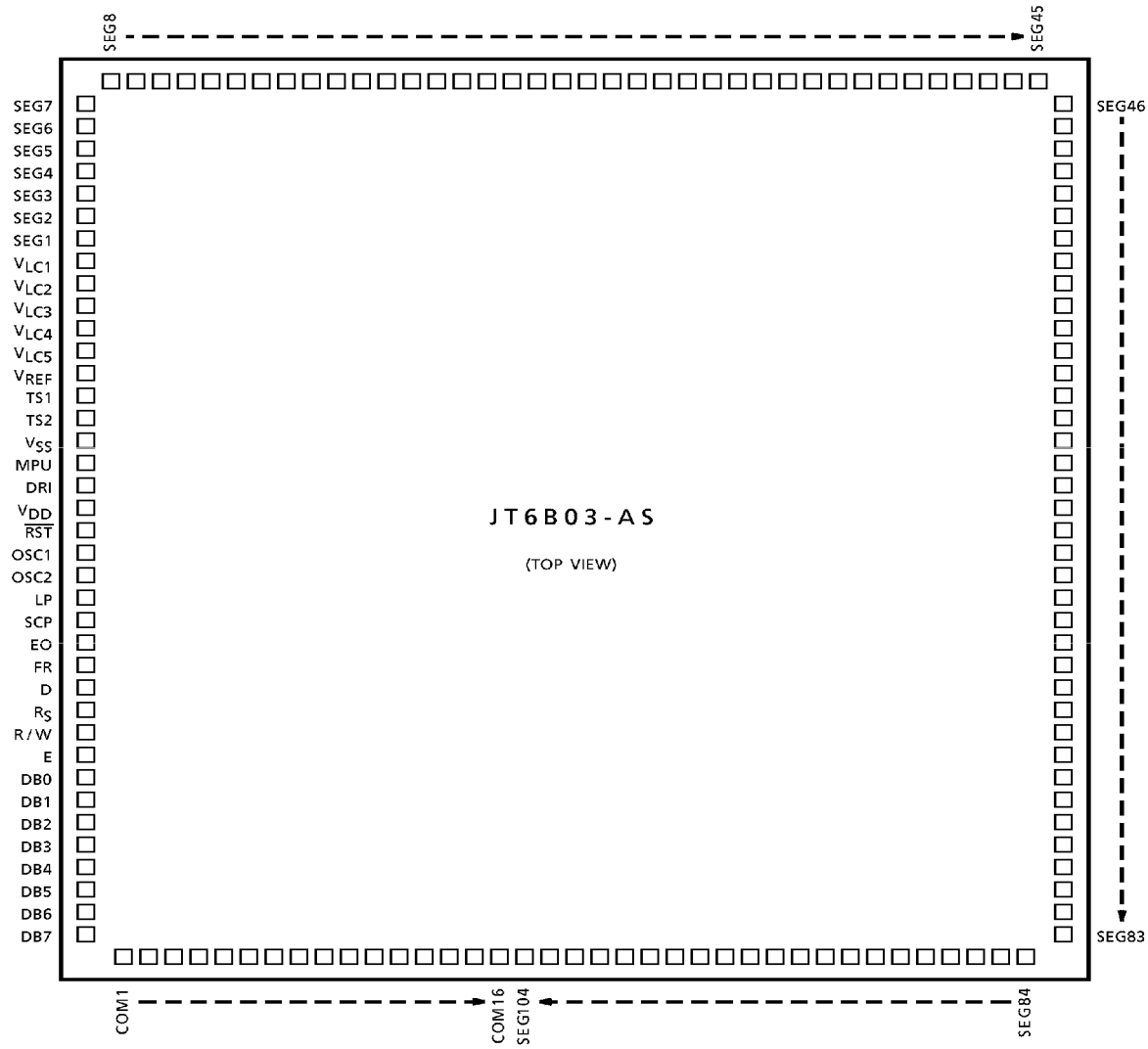
970917EBM2

- Built-in clock generator (with external resistor or ceramic oscillator)
  (external clock operation possible)
- Power supply 5V ± 10%
- Low power consumption
- Built-in resistance ladder for driver (4kΩ × 5)
- CMOS and Si-gate process, Bare chip

BLOCK DIAGRAM



PAD ASSIGNMENT



PAD COORDINATES

Chip Size 6.60 × 6.65 (mm)
Pad Number 151

Chip Tip Coordinates 1 – 3300.0, – 3325.0
Chip Tip Coordinates 2 – 3300.0, 3325.0
Chip Tip Coordinates 3 3300.0, 3325.0
Chip Tip Coordinates 4 3300.0, – 3325.0

No.	NAME	X-POINT	Y-POINT	No.	NAME	X-POINT	Y-POINT
1	SEG7	– 3002	– 3053	37	DB6	2781	– 3053
2	SEG6	– 2782	– 3053	38	DB7	3001	– 3053
3	SEG5	– 2592	– 3053	39	COM1	3058	– 2833
4	SEG4	– 2421	– 3053	40	COM2	3058	– 2643
5	SEG3	– 2262	– 3053	41	COM3	3058	– 2472
6	SEG2	– 2102	– 3053	42	COM4	3058	– 2313
7	SEG1	– 1954	– 3053	43	COM5	3058	– 2153
8	V_{LC1}	– 1805	– 3053	44	COM6	3058	– 2005
9	V_{LC2}	– 1657	– 3053	45	COM7	3058	– 1856
10	V_{LC3}	– 1508	– 3053	46	COM8	3058	– 1708
11	V_{LC4}	– 1360	– 3053	47	COM9	3058	– 1559
12	V_{LC5}	– 1211	– 3053	48	COM10	3058	– 1411
13	V_{REF}	– 1063	– 3053	49	COM11	3058	– 1262
14	TS1	– 914	– 3053	50	COM12	3058	– 1114
15	TS2	– 766	– 3053	51	COM13	3058	– 965
16	V_{SS}	– 617	– 3053	52	COM14	3058	– 817
17	MPU	– 469	– 3053	53	COM15	3058	– 668
18	DRI	– 320	– 3053	54	COM16	3058	– 520
19	V_{DD}	– 172	– 3053	55	SEG104	3058	– 371
20	$\overline{RST}$	– 23	– 3053	56	SEG103	3058	– 223
21	OSC1	125	– 3053	57	SEG102	3058	– 74
22	OSC2	274	– 3053	58	SEG101	3058	74
23	LP	422	– 3053	59	SEG100	3058	223
24	SCP	609	– 3053	60	SEG99	3058	371
25	EO	758	– 3053	61	SEG98	3058	520
26	FR	945	– 3053	62	SEG97	3058	668
27	D	1093	– 3053	63	SEG96	3058	817
28	R_S	1276	– 3053	64	SEG95	3058	965
29	R / W	1425	– 3053	65	SEG94	3058	1114
30	E	1573	– 3053	66	SEG93	3058	1262
31	DB0	1722	– 3053	67	SEG92	3058	1411
32	DB1	1909	– 3053	68	SEG91	3058	1559
33	DB2	2057	– 3053	69	SEG90	3058	1708
34	DB3	2244	– 3053	70	SEG89	3058	1856
35	DB4	2404	– 3053	71	SEG88	3058	2016
36	DB5	2591	– 3053	72	SEG87	3058	2175

No.	NAME	X-POINT	Y-POINT	No.	NAME	X-POINT	Y-POINT
73	SEG86	3058	2346	113	SEG46	– 2905	3053
74	SEG85	3058	2536	114	SEG45	– 3058	2833
75	SEG84	3058	2756	115	SEG44	– 3058	2643
76	SEG83	2978	3053	116	SEG43	– 3058	2472
77	SEG82	2758	3053	117	SEG42	– 3058	2313
78	SEG81	2567	3053	118	SEG41	– 3058	2153
79	SEG80	2397	3053	119	SEG40	– 3058	2005
80	SEG79	2237	3053	120	SEG39	– 3058	1856
81	SEG78	2078	3053	121	SEG38	– 3058	1708
82	SEG77	1929	3053	122	SEG37	– 3058	1559
83	SEG76	1781	3053	123	SEG36	– 3058	1411
84	SEG75	1632	3053	124	SEG35	– 3058	1262
85	SEG74	1484	3053	125	SEG34	– 3058	1114
86	SEG73	1335	3053	126	SEG33	– 3058	965
87	SEG72	1187	3053	127	SEG32	– 3058	817
88	SEG71	1038	3053	128	SEG31	– 3058	668
89	SEG70	890	3053	129	SEG30	– 3058	520
90	SEG69	741	3053	130	SEG29	– 3058	371
91	SEG68	593	3053	131	SEG28	– 3058	223
92	SEG67	444	3053	132	SEG27	– 3058	74
93	SEG66	296	3053	133	SEG26	– 3058	– 74
94	SEG65	147	3053	134	SEG25	– 3058	– 223
95	SEG64	– 75	3053	135	SEG24	– 3058	– 371
96	SEG63	– 223	3053	136	SEG23	– 3058	– 520
97	SEG62	– 372	3053	137	SEG22	– 3058	– 668
98	SEG61	– 520	3053	138	SEG21	– 3058	– 817
99	SEG60	– 669	3053	139	SEG20	– 3058	– 965
100	SEG59	– 817	3053	140	SEG19	– 3058	– 1114
101	SEG58	– 966	3053	141	SEG18	– 3058	– 1262
102	SEG57	– 1114	3053	142	SEG17	– 3058	– 1411
103	SEG56	– 1263	3053	143	SEG16	– 3058	– 1559
104	SEG55	– 1411	3053	144	SEG15	– 3058	– 1708
105	SEG54	– 1560	3053	145	SEG14	– 3058	– 1856
106	SEG53	– 1708	3053	146	SEG13	– 3058	– 2005
107	SEG52	– 1857	3053	147	SEG12	– 3058	– 2153
108	SEG51	– 2005	3053	148	SEG11	– 3058	– 2313
109	SEG50	– 2165	3053	149	SEG10	– 3058	– 2472
110	SEG49	– 2324	3053	150	SEG9	– 3058	– 2643
111	SEG48	– 2495	3053	151	SEG8	– 3058	– 2833
112	SEG47	– 2685	3053				

PIN FUNCTIONS

SYMBOL	TYPE	NAME AND FUNCTION
RS	Input	Register Select : Selects Data or Instruction register RS = 0 and R / W = 0 : Instruction register is selected RS = 0 and R / W = 1 : Busy flag and Address Counter are selected RS = 1 : Data register is selected
R / W	Input	Read / Write : Selects Read operation or Write operation
E	Input	Enable : Enable Read / Write operation
DB0 to DB3	I / O	Data Bus : Three-state bi-directional data bus (lower 4 bits) In 4-bit interface mode, do not use these lines
DB4 to DB7	I / O	Data Bus : Three-state bi-directional data bus (higher 4 bits)
LP	Output	Latch Pulse : Latch pulse for extension driver
SCP	Output	Shift Clock Pulse : Shift Clock Pulse for extension driver
FR	Output	Frame : Frame Signal for extension driver
D	Output	Data : Serial data output for extension driver 0 : OFF 1 : ON
COM1 to COM16	Output	Common : Row signal output 1 / 8 duty operation : COM9 to COM16 are not selected 1 / 11 duty operation : COM12 to COM16 are not selected
SEG1 to SEG104	Output	Segment : Column signal output
V_{LC5}	Input	Power supply for LCD
V_{LC1} to V_{LC4}	Output	Power supply for LCD
V_{DD}, V_{SS}	Input	Power supply for JT6B03-AS V_{DD} = 5.0V ± 10% V_{SS} = 0V
OSC1, OSC2	—	When using the internal clock oscillator, connect a resistor or ceramic oscillator between OSC1 and OSC2. When using an external clock, connect the clock to OSC1 and leave OSC2 open.
$\overline{RST}$	Input	Reset : $\overline{RST}$ = L→ Reset state
EO	Output	Enable out : Enable signal for extension driver
V_{REF}	Input	Power supply for LCD
DRI	Input	Selects extension column driver. 1 : T6A41, 0 : T6A92
MPU	Input	Selects control MPU. 1 : 68-Series, 0 : 80-Series
TS1, TS2	Input	Test pin : Usually connected to V_{SS}

FUNCTION OF EACH BLOCK

- Register

  The JT6B03-AS has two 8-bit registers. One is an instruction register (IR), and the other is a data register (DR).
  The IR stores an instruction code, DD RAM address data or CG RAM address data. The IR is a write-only register for the MPU.
  The DR temporarily holds data that is to be written into or read from the DD RAM or the CG RAM. In the Write sequence, the data in the DR is automatically sent to the DD RAM or the CG RAM. In the Read sequence, when the address data has been written into the IR, the data is automatically sent to the DR from the DD RAM or the CG RAM. Hence, the MPU can read the DD RAM or the CG RAM data from DR. The address data is automatically incremented or decremented after a Read operation.
  The relation between RS, R/W ($\overline{WR}$) and the operation is as shown below.

RS	R/W ($\overline{WR}$)	OPERATION
0	0	Write into IR
0	1	Read Busy flag (DB7) and Address Counter (DB0 to DB6)
1	0	Write into DR
1	1	Read from DR

- Busy flag (BF)

  When an instruction is executed, the JT6B03-AS sets the Busy flag. The MPU reads the status of the Busy flag using the Read Busy Flag instruction. When the Busy flag is set, the JT6B03-AS cannot accept any instructions from the MPU (other than Read Busy Flag). The MPU must check the setting of the Busy flag before sending each instruction.

- Address Counter (AC)

  The JT6B03-AS has a 7-bit Address Counter. The Address Counter points to an address in DD RAM or CG RAM, or to the cursor position. The Set DD RAM Address or Set CG RAM Address instruction specifies which type of address Address Counter contains. The Address Counter is automatically incremented (or decremented) after the data has been written into or read from RAM. When RS = 0 and R/W ($\overline{WR}$) = 1, the contents of the Address Counter is output on DB0 to DB6.

- Display data RAM (DD RAM)

  The display data RAM (DD RAM) stores the display data as 8-bit character codes. Its capacity is 80 characters × 8 bits. The relation between the DD RAM address and the display position is shown below.
  A DD RAM address is expressed as shown below.

	MSB						LSB
AC	DB6	DB5	DB4	DB3	DB2	DB1	DB0

(Example) When DD RAM address = 4CH

MSB						LSB
1	0	0	1	1	0	0
4			C			

(1) The relation between the DD RAM address and the display position in 1-Line Display mode (N = 0)

1	2	3	4	5		79	80	← Display position
00	01	02	03	04	----------	4E	4F	← DD RAM address

a) Using one JT6B03-AS, The first 20 characters are displayed as shown below.

1	2	3	4	5	6	7	8		19	20
00	01	02	03	04	05	06	07	--------	12	13

When a Display Shift operation is executed, the relation between the DD RAM address and the display position is as shown below.

	1	2	3	4	5	6	7	8		18	19	20
Left shift display	01	02	03	04	05	06	07	08	----------	12	13	14

	1	2	3	4	5	6	7	8		18	19	20
Right shift display	4F	00	01	02	03	04	05	06	----------	10	11	12

b) When the JT6B03-AS is used with one T6A92, the first 36 characters are displayed as shown below.

1	2	3	4	5		20	21	22		35	36
00	01	02	03	04	-----	13	14	15	--------	22	23
←—— JT6B03-AS Display ——→						←—— T6A92 Display ——→					

When a Display Shift operation is executed, the relation between the DD RAM address and the display position is as shown below.

	1	2	3	4	5	6	7	8	9	10		35	36
Left shift display	01	02	03	04	05	06	07	08	09	0A	--------	23	24
Right shift display	4F	00	01	02	03	04	05	06	07	08	--------	21	22

c) Each extra T6A92 allows 16 more characters to be displayed. A maximum of four T6A92s can be used, allowing display of up to 80 characters.

1	2	3	4	5		20	21	22		67	68	69	70		78	79	80
00	01	02	03	04	-----	13	14	15	--------	43	44	45	46	--------	4D	4E	4F
←—— JT6B03-AS Display ——→						←—— T6A92 (1) to (3) Display ——→						←—— T6A92 (4) Display ——→					

(2) The relation between the DD RAM address and the display position in 2-Line Display mode (N = 1)

	1	2	3	4		39	40	← Display position
1st line	00	01	02	03	----------	26	27	← DD RAM address
2nd line	40	41	42	43	----------	66	67	

(Note) The DD RAM address of the 2nd line is not the next address after the last address of the 1st line.

a) Using one JT6B03-AS, the first 40 characters (20 characters × 2 lines) are displayed as shown below.

	1	2	3	4	5	6	7	8		19	20
1st line	00	01	02	03	04	05	06	07	----------	12	13
2nd line	40	41	42	43	44	45	46	47	----------	52	53

When a Display Shift operation is executed, the relation between the DD RAM address and the display position is as shown below.

Left shift display

1	2	3	4	5	6	7	8		19	20
01	02	03	04	05	06	07	08	----------	13	14
41	42	43	44	45	46	47	48	----------	53	54

Right shift display

1	2	3	4	5	6	7	8		19	20
27	00	01	02	03	04	05	06	----------	11	12
67	40	41	42	43	44	45	46	----------	51	52

b) Using one JT6B03-AS with one T6A92, the first 72 characters (36 characters × 2 lines) are displayed as shown below.

	1	2	3	4	5		20	21	22		35	36
1st line	00	01	02	03	04	-----	13	14	15	--------	22	23
2nd line	40	41	42	43	44	-----	53	54	55	--------	62	63

JT6B03-AS Display — T6A92 Display

When a Display Shift operation is executed, the relation between the DD RAM address and the display position is as shown below.

Left shift display

1	2	3	4	5	6	7	8	9	10		35	36
01	02	03	04	05	06	07	08	09	0A	----------	23	24
41	42	43	44	45	46	47	48	49	4A	----------	63	64

Right shift display

1	2	3	4	5	6	7	8	9	10		35	36
27	00	01	02	03	04	05	06	07	08	----------	21	22
67	40	41	42	43	44	45	46	47	48	----------	61	62

c) Each extra T6A92 allows 16 more characters to be displayed. Two T6A92s can be used, allowing display of up to 40 characters × 2 lines.

	1	2	3	4	5		20	21	22		35	36	37	38	39	40
1st lines	00	01	02	03	04	-----	13	14	15	--------	22	23	24	25	26	27
2nd lines	40	41	42	43	44	-----	53	54	55	--------	62	63	64	65	66	67

JT6B03-AS Display — T6A92 (1) Display — T6A92 (2) Display

- Character generator ROM (CG ROM)

  The character generator ROM generates the character patterns (5 × 10 dots × 240 characters) according to 8-bit character codes. In the 5 × 7 Dots + Cursor Display mode, the character font uses the upper 5 × 7 dots. The relation between character codes and character patterns is as shown overleaf.

THE RELATION BETWEEN CHARACTER CODES AND CHARACTER PATTERN

HIGHER 4 BITS / LOWER 4 BITS	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
XXXX0000	CGRAM (0)															
XXXX0001	(1)															
XXXX0010	(2)															
XXXX0011	(3)															
XXXX0100	(4)															
XXXX0101	(5)															
XXXX0110	(6)															
XXXX0111	(7)															
XXXX1000	(0)															
XXXX1001	(1)															
XXXX1010	(2)															
XXXX1011	(3)															
XXXX1100	(4)															
XXXX1101	(5)															
XXXX1110	(6)															
XXXX1111	(7)															

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- Character generator RAM (CG RAM)

  The JT6B03-AS can display user-defined original characters using the character generator RAM. (5×7 dots : 8-type or 5×10 dots : 4-type).
  The relation between the character codes, the CG RAM address and character patterns is as shown below.

  (1) For 5×7-dot character patterns

CHARACTER CODES (DD RAM DATA)									CG RAM ADDRESS						CHARACTER PATTERNS (CG RAM DATA)								
7	6	5	4	3	2	1	0		5	4	3	2	1	0	7	6	5	4	3	2	1	0
0	0	0	0	*	0	0	0		0	0	0	0	0	0	*	*	*	1	1	1	1	0
												0	0	1				1	0	0	0	1
												0	1	0				1	0	0	0	1
												0	1	1				1	1	1	1	0
												1	0	0				1	0	0	0	1
												1	0	1				1	0	0	0	1
												1	1	0				1	1	1	1	0
												1	1	1	*	*	*	0	0	0	0	0
0	0	0	0	*	0	0	1		0	0	1	0	0	0	*	*	*	0	1	1	1	1
												0	0	1				1	0	0	0	0
												0	1	0				1	0	0	0	0
												0	1	1				0	1	1	1	0
												1	0	0				0	0	0	0	1
												1	0	1				0	0	0	0	1
												1	1	0				1	1	1	1	0
												1	1	1	*	*	*	0	0	0	0	0
												0	0	0	*	*	*	1	1	1	1	1
												0	0	1				0	0	1	0	0
0	0	0	0	*	1	1	1		1	1	1	0	1	1				0	0	1	0	0
												1	0	0				0	0	1	0	0
												1	0	1				0	0	1	0	0
												1	1	0				0	0	1	0	0
												1	1	1	*	*	*	0	0	0	0	0

Character Pattern Example (1)

← Cursor Position

Character Pattern Example (2)

← Cursor Position

* : Invalid

(Note 1) Character code bit 0 to bit 2 correspond to CG RAM address bit 3 to bit 5.
(Note 2) Bit 0 to bit 2 of the CG RAM address indicate the row within the character bit map. The 8th row (the bottom row) corresponds to the cursor position on the LCD display. Normally the 8th row should be blank (all 0s), otherwise the lowest line of the character will be obscured when used with the cursor.
(Note 3) Character pattern line positions correspond to CG RAM data bit 0 to bit 4. CG RAM data bit 5 to bit 7 is not used for display; the data can be used for general RAM data.
(Note 4) If bit 4 to bit 7 are all 0, a CG RAM character is indicated. The value of bit 3 does not matter. Character codes 00H and 08H select the same character.
(Note 5) 1 : ON, 0 : OFF

(2) For 5 × 10-dot character patterns

CHARACTER CODES (DD RAM DATA)									CG RAM ADDRESS							CHARACTER PATTERNS (CG RAM DATA)										
7	6	5	4	3	2	1	0		5	4	3	2	1	0		7	6	5	4	3	2	1	0		
											0	0	0	0		*	*	*	0	0	0	1	0		
											0	0	0	1					0	0	0	0	0		
											0	0	1	0					0	0	1	1	0		
											0	0	1	1					0	0	0	1	0		Character Pattern
											0	1	0	0					0	0	0	1	0		Example
0	0	0	0	*	0	0	*		0	0	0	1	0	1					0	0	0	1	0		
											0	1	1	0					0	0	0	1	0		
											0	1	1	1					0	0	0	1	0		
											1	0	0	0					1	0	0	1	0		
											1	0	0	1					0	1	1	0	0		
											1	0	1	0		*	*	*	0	0	0	0	0		← Cursor Position
											1	0	1	1		*	*	*	*	*	*	*	*		
											1	1	0	0											
											1	1	0	1											
											1	1	1	0											
											1	1	1	1		*	*	*	*	*	*	*	*		
											0	0	0	0		*	*	*							
											0	0	0	1											
											0	0	1	0											
											1	0	0	0											
0	0	0	0	*	1	1	*		1	1	1	0	0	1											
											1	0	1	0		*	*	*							
											1	0	1	1		*	*	*	*	*	*	*	*		
											1	1	0	0											
											1	1	0	1											
											1	1	1	0											
											1	1	1	1		*	*	*	*	*	*	*	*		* : Invalid

(Note 1) Character code bit 1 and bit 2 correspond to CG RAM address bit 4 and bit 5.

(Note 2) Bit 0 to bit 3 of the CG RAM address indicate the row within the character bit map. The 11th row corresponds to the cursor position on the LCD display. Normally the 11th row should be blank (all 0s), otherwise the lowest line of the character will be obscured when used with the cursor. Lines 12 to 16 are not used for display data and can be used for general RAM data.

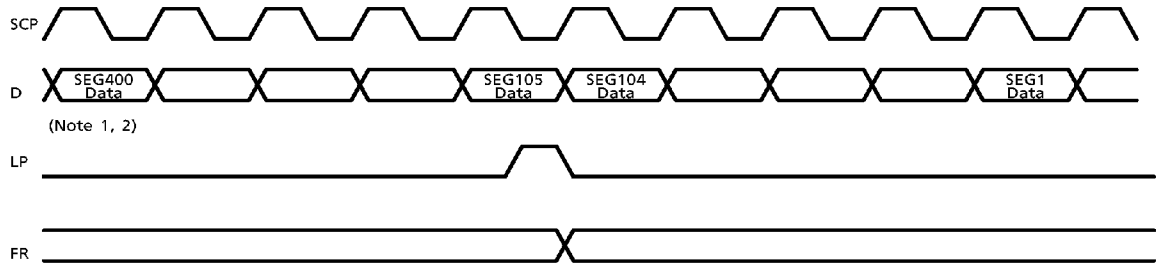
(Note 3) If bit 4 to bit 7 are all 0, a CG RAM character is indicated. The values of bits 0 and 3 do not matter. Character codes 00H, 01H, 08H and 09H all select the same character.

(Note 4) 1 : ON, 0 : OFF

- Timing generation circuit

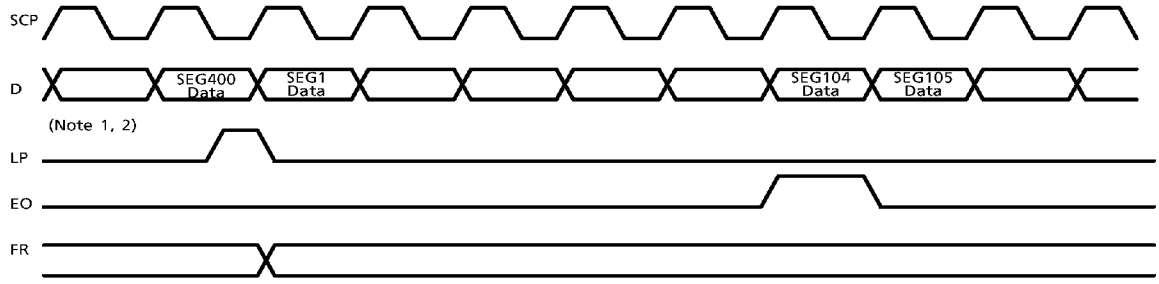
  The timing generation circuit generates timing signals for operating internal circuits such as the DD RAM, CG ROM and CG RAM.
  It is designed to MPU access not disturb display. So in write data to the DD RAM of JT6B03-AS display never disturb expect data writing area.
  This circuit also generates timing signals which operate the extension driver (e.g. T6A41 and T6A92).
  The relation between the timing signals in 1-Line Display mode is as shown below.

  (1) Shift mode



  (Note 1) SEG400 to SEG105 Data for the extension driver
  SEG104 to SEG1 Data for the JT6B03-AS
  (Note 2) In 2-Line Display mode, "SEG400 Data" changes to "SEG200 Data"

  (2) Enable mode

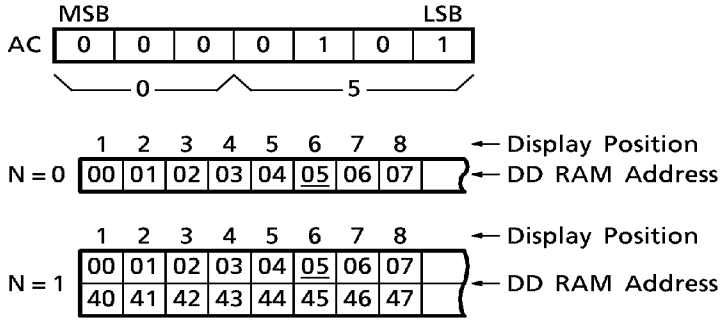


- LCD drive circuit

  The LCD drive circuit consists of 16 row drivers and 104 column drivers. When the character font type and the number of lines have been selected by the appropriate command, the valid row drivers automatically output drive waveforms, and the other row drivers output OFF waveforms. Character pattern data send serially to internal 104-bit shift register, and latch to the register when all needed data send to JT6B03-AS. The column-drivers output drive waveforms corresponding to the latched data.

- Cursor / blink display control circuit

  This circuit generates the cursor or blink display. The cursor or blink is displayed in the digit which corresponds to the DD RAM address set in the Address Counter.
  When the Address Counter is set to 05H, the cursor is displayed as shown below.



  (Note) The cursor or blink is also displayed when the CG RAM address is set in the Address Counter. In this case, the cursor or blink is displayed regardless of the DD RAM address.

- Internal reset circuit

  When the power is on, the JT6B03-AS is automatically initialized by the internal reset circuit. The same is true when $\overline{RST}$ = L. The Busy flag (BF) remains at 1 (Busy state) until initialization ends. The following instructions are executed during initialization.

  (1) Display Clear

  (2) Set Function ..... DL = 1 : 8-bit data interface
  N = 0 : 1-line display
  F = 0 : 5 × 7-dot character font

  (3) Set Entry Mode ..... I / D = 1 : +1
  S = 0 : No shift

  (4) Display ON / OFF Control ... D = 0 : Display OFF
  C = 0 : Cursor OFF
  B = 0 : Blink OFF

  (Note) The MPU should use system reset ($\overline{RST}$ = L), because the internal reset circuit may not move normally according to the power supply condition.

- Interfacing to the MPU

  The JT6B03-AS has two methods of interfacing to the MPU. One is the 8-bit data interface and the other is the 4-bit data interface.

  (1) When using the 4-bit interface, the JT6B03-AS uses DB4 to DB7 as the interface, and does not use DB0 to DB3. In this mode, the MPU must send two sets of 4-bit data. First the higher 4 bits are sent to the JT6B03-AS, then the lower 4 bits are sent.
  The Busy flag and Address Counter data is also sent in 2 parts.

  (2) When the 8-bit interface is used, the JT6B03-AS uses DB0 to DB7 as the interface.

INSTRUCTION

The MPU can directly control two registers. One is the Instruction register (IR) and the other is the Data register (DR).
While the JT6B03-AS is executing an instruction, it cannot accept any other instructions (except for the Read Busy Flag and Address instruction). The Busy flag is maintained at 1 (Busy state) until the instruction completes. A Busy check must be done before the next instruction is sent from the MPU to the JT6B03-AS.
If an instruction is sent to the JT6B03-AS without a Busy check, the MPU must wait the execution time of the instruction before sending the next instruction to the JT6B03-AS.

INSTRUCTION	CODE										DESCRIPTION	EXECUTION TIME (MAX) (f_{osc} = 250kHz)
	R_S	R / W (WR)	D7	D6	D5	D4	D3	D2	D1	D0		
Test	0	0	0	0	0	0	0	0	0	0	Do not use.	0μs
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears the display and sets DD RAM address 0 in Address Counter	1.64ms
Return Home	0	0	0	0	0	0	0	0	1	*	Sets DD RAM address 0 in Address Counter and returns display to home position. The contents of the DD RAM do not change.	1.64ms
Set Entry Mode	0	0	0	0	0	0	0	1	I / D	S	Sets cursor shift direction and display shift. These operations are executed when data is written.	40μs
Display ON / OFF Control	0	0	0	0	0	0	1	D	C	B	Sets ON / OFF for all displays (D), cursor ON / OFF (C), cursor position blink (B).	40μs

INSTRUCTION	CODE										DESCRIPTION	EXECUTION TIME (MAX) (f_{osc} = 250kHz)
	RS	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0		
Cursor / Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Shifts cursor and display without changing DD RAM contents	40μs
Set Function	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL), number of display lines (N), and character font (F)	40μs
Set CG RAM Address	0	0	0	1	CG RAM Address						Sets CG RAM Address	40μs
Set DD RAM Address	0	0	1	DD RAM Address							Sets DD RAM Address	40μs
Read Busy Flag and Address	0	1	BF	Address Counter							Reads Busy Flag (BF), and Address Counter contents	0μs
Write Data to CG RAM or DD RAM	1	0	Write Data								Writes data into DD RAM or CG RAM	46μs
Read Data from CG or DD RAM	1	1	Read Data								Reads data from DD RAM or CG RAM	46μs
—	I/D = 1 : Increment I/D = 0 : Decrement S = 1 : Display Shift On S/C = 1 : Display Shift S/C = 0 : Cursor Shift R/L = 1 : Shift to the Right R/L = 0 : Shift to the Left DL = 1 : 8 bits DL = 0 : 4 bits N = 1 : 2 lines N = 0 : 1 line F = 1 : 5×10 dots F = 0 : 5×7 dots BF = 1 : Busy State BF = 0 : Can Accept Instruction											—	—

*: Invalid

- Clear Display

	RS	R/W ($\overline{WR}$)	DB7						DB0
Instruction Code	0	0	0	0	0	0	0	0	1

When the JT6B03-AS executes this instruction, code 20H (code 20H must be the "Space code") is written to every address in the DD RAM. This command resets DD RAM address in the Address Counter.
The display is inhibited and the cursor or blink is moved to the left of the display. (In 2-Line Display mode, the cursor moves to the left of 1st line of the display.) The I/D of Entry mode is set to 0. The S of Entry mode does not change.

- Return Home

	RS	R/W ($\overline{WR}$)	DB7							DB0
Instruction Code	0	0	0	0	0	0	0	0	1	*

* : invalid

The DD RAM address in the Address Counter is reset by this instruction, and the display shift is cancelled (return to home position). The contents of the DD RAM do not change. The cursor or blink moves to the extreme left end of the display. (In 2-Line Display mode, the cursor moves to the extreme left of the 1st line of the display.)

- Set Entry Mode

	RS	R/W ($\overline{WR}$)	DB7							DB0
Instruction Code	0	0	0	0	0	0	0	1	I/D	S

I/D : The Address Counter is incremented (I/D = 1) or decremented (I/D = 0) after the data has been written to or read from DD RAM.
The same is true when data is written to or read from CG RAM.

S : If S = 1, the entire display is shifted left (I/D = 1) or right (I/D = 0) when data is written to the DD RAM. (The cursor position does not move)
If S = 0, the display is not shifted.

- Display ON / OFF Control

	RS	R / W ($\overline{WR}$)	DB7	----------					DB0
Instruction Code	0	0	0	0	0	0	1	D	C	B

D : D = 1, display is ON; D = 0, display is OFF.
When D is reset, the contents of the DD RAM do not change. Therefore, the contents can be displayed as before by setting D.

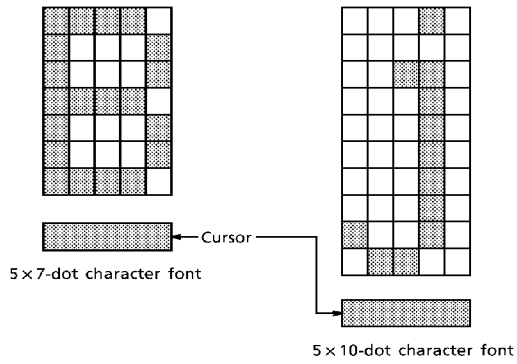
C : C = 1, cursor display is ON; C = 0, cursor display is OFF.
5 × 7-dot character font : cursor display uses 5 dots on the 8th line
5 × 10-dot character font : cursor display uses 5 dots on the 11th line

B : B = 1, character blink is ON (same position of cursor position); B = 0, character blink is OFF.

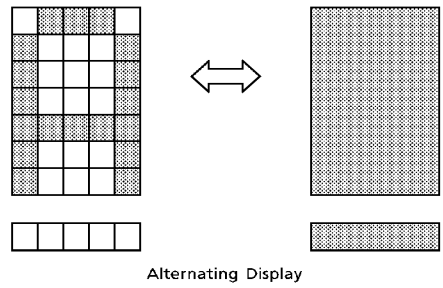
Cursor and blink can operate at same time.

Blink period : Font 5 × 7-dot, f_{OSC} = 250kHz
(1 / 250k) × 5 × 80 × 8 × 32 = 409.6 (ms)

Font 5 × 10-dot, f_{OSC} = 250kHz
(1 / 250k) × 5 × 80 × 11 × 32 = 563.2 (ms)



(1) Cursor display example



(2) Blink display example

- Cursor Display Shift

	RS	R/W ($\overline{WR}$)	DB7							DB0
Instruction Code	0	0	0	0	0	1	S/C	R/L	*	*

* : invalid

When this instruction is executed, the cursor or display is shifted to the right or left without display data being written or read.
In 2-Line Display mode, the cursor is shifted from the 40th digit of the 1st line to the 1st digit of the 2nd line.

S/C	R/L	FUNCTIONS	ADDRESS COUNTER (AC)
0	0	Shift the cursor to the left.	AC = AC − 1
0	1	Shift the cursor to the right.	AC = AC + 1
1	0	Shift the whole display to the left. The cursor follows the display shift direction.	AC = AC
1	1	Shift the whole display to the right. The cursor follows the display shift direction.	AC = AC

When S/C = 1, the contents of the Address Counter do not change.

- Set Function

	RS	R/W ($\overline{WR}$)	DB7							DB0
Instruction Code	0	0	0	0	1	DL	N	F	*	*

DL : DL = 1, 8-bit data interface (DB0 to DB7)
DL = 0, 4-bit data interface (DB4 to DB7)

N : N = 0, 1-Line Display mode
N = 1, 2-Line Display mode

F : F = 0, 5 × 7-dot character font
F = 1, 5 × 10-dot character font

(Note) Execute this instruction first in a program before executing any other instructions (except for the Busy Flag / Address Read instruction).
After this instruction has been used once, it cannot be used again, except to change the DL bit setting.

N	F	No. OF DISPLAY LINES	CHARACTER FONT	DUTY	NOTE
0	0	1	5 × 7 dots	1/8	—
0	1	1	5 × 10 dots	1/11	—
1	*	2	5 × 7 dots	1/16	When N = 1, the 5 × 10 dots character font cannot be selected.

- Set CG RAM Address

	R/W									
	RS	($\overline{WR}$)	DB7	----------						DB0
Instruction Code	0	0	0	1	A	A	A	A	A	A
					MSB					LSB

This instruction sets CG RAM address data (e.g. AAAAAA (bin)) into Address Counter.
The MPU can now read or write CG RAM data.

- Set DD RAM Address

	R/W									
	RS	($\overline{WR}$)	DB7	----------						DB0
Instruction Code	0	0	1	A	A	A	A	A	A	A
				MSB						LSB

This instruction sets DD RAM address data (e.g. AAAAAAA (bin)) to the Address Counter.
The MPU can now read or write DD RAM data.

- Read Busy Flag and Address

	R/W									
	RS	($\overline{WR}$)	DB7	----------						DB0
Instruction Code	0	1	BF	A	A	A	A	A	A	A
				MSB						LSB

This instruction makes the JT6B03-AS output the Busy flag and the contents of the Address Counter. The Busy flag indicates whether the JT6B03-AS can receive an instruction or not. A Busy check must done before the next instruction is sent to the JT6B03-AS.
The Address Counter indicates the CG or DD RAM address.
The preceding two instructions (Set CG RAM Address and Set DD RAM Address) determine whether the Address Counter is used to hold a CG RAM address or a DD RAM address.

- Write Data to CG or DD RAM

	R / W									
	RS	($\overline{WR}$)	DB7	----------						DB0
Instruction Code	1	0	D	D	D	D	D	D	D	D
			MSB							LSB

This instruction writes 8-bit data (e.g. DDDDDDDD (bin)) to CG RAM or DD RAM. The previous instruction (Set CG RAM Address or Set DD RAM Address) determines whether the data will be written to CG RAM or DD RAM. Before this instruction is executed, the Set CG RAM or DD RAM Address instruction must be executed.
After the data has been written, the address is automatically incremented by 1 or decremented by 1 according to the entry mode. The display mode is also determined by the entry mode.

- Read Data from CG or DD RAM

	R / W									
	RS	($\overline{WR}$)	DB7	----------						DB0
Instruction Code	1	1	D	D	D	D	D	D	D	D
			MSB							LSB

This instruction reads 8-bit data (e.g. DDDDDDDD (bin)) from CG RAM or DD RAM. The previous instruction (Set CG RAM Address or Set DD RAM Address) determines whether the data will be read from CG RAM or DD RAM. Before this instruction is executed, the Set CG RAM or DD RAM Address instruction must be executed. If neither of these instructions is executed, the first data read will not yield valid data.

A Read Data from CG or DD RAM instruction just after a Write Data to CG or DD RAM instruction cannot read the RAM data pointed to by Address Counter.
To read the RAM data indicated by Address Counter, perform one of the following operations:

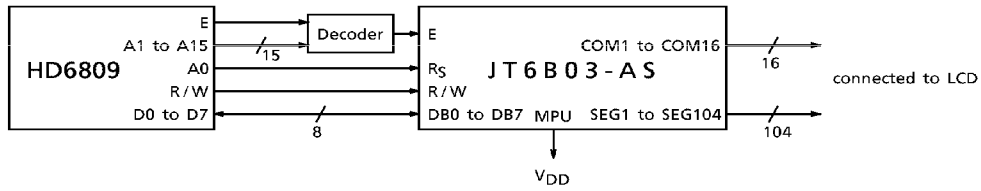
① Use Set CG RAM Address or Set DD RAM Address command.
② (For DD RAM only) perform a cursor shift. (Note)
③ Read RAM data once (to read invalid data) then read RAM data again.

(Note) A Cursor Shift instruction does the function which is the same as Set DD RAM Address instruction.

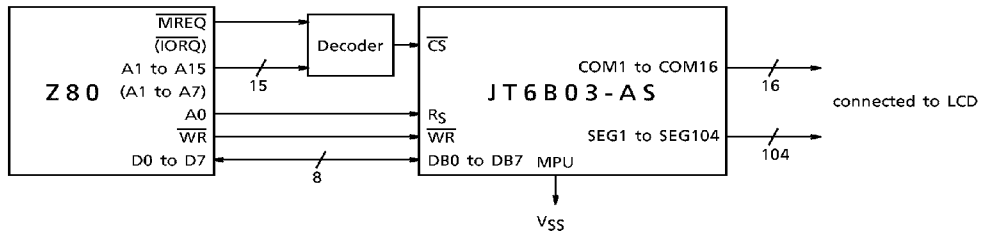
After the data has been read, the RAM address is automatically incremented by 1 or decremented by 1 according to the entry mode.

HOW TO USE THE JT6B03-AS

- Interface to 68-Series MPU



- Interface to 80-Series MPU



(Note) Z80 is a trademark of ZILOG Inc.

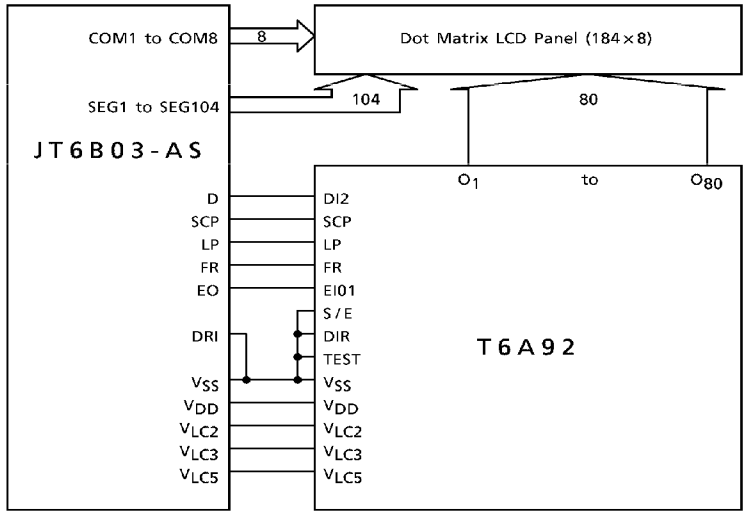
- Interface to LCD

The JT6B03-AS can display a 5×7-dot or 5×10-dot character font plus a cursor, and can display up to two lines with 5×7-dot characters.
The relation between number of lines and character font is as shown below.

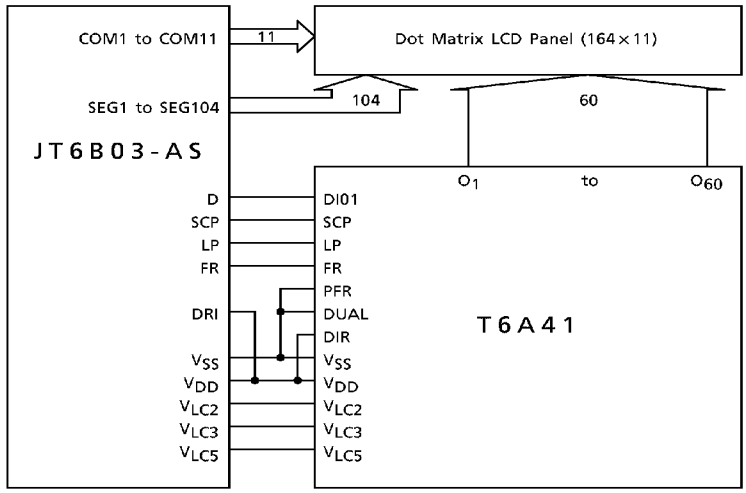
NUMBER OF LINES	CHARACTER FONT	DUTY
1	5×7 dots + Cursor	1 / 8
1	5×10 dots + Cursor	1 / 11
2	5×7 dots + Cursor	1 / 16

- Application

(1) 36-character × 1-line display (5 × 7 dots) on the T6A92

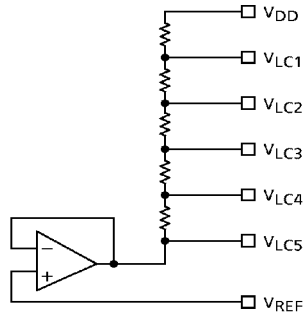


(2) 32-character × 1-line display (5 × 10 dots) on the T6A41

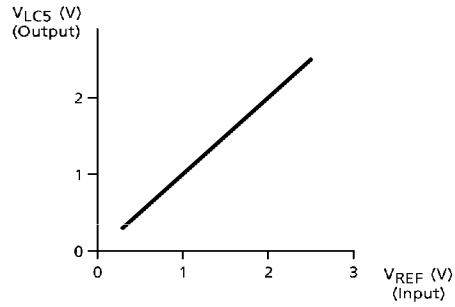


POWER SUPPLY FOR LCD DRIVE

The JT6B03-AS includes internal resistors to divide the bias voltage, and a power supply op-amp.



OP-AMP CHARACTERISTICS

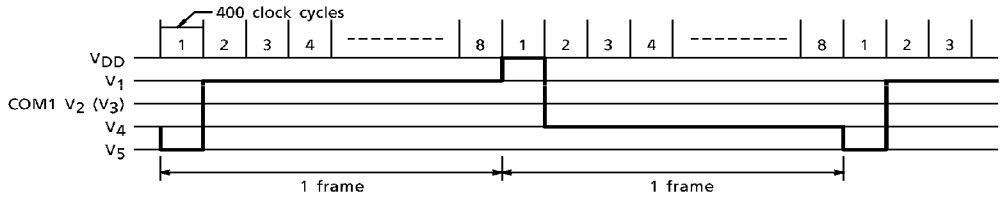


(Note) When JT6B03-AS is reset, $V_{LC5} = V_{DD}$.

THE RELATION BETWEEN OSCILLATION FREQUENCY AND LCD FRAME FREQUENCY

LCD frame frequency example (f_{OSC} = 250kHz)

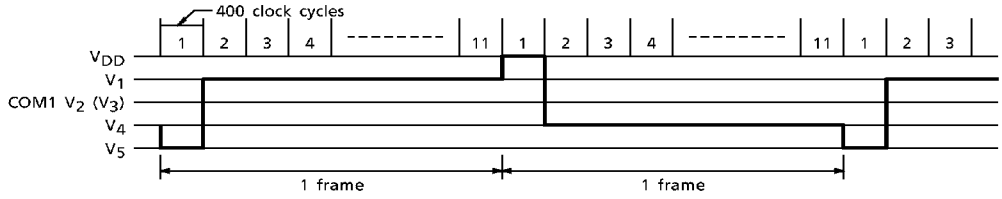
- 1 / 8 duty



1 frame = 4 μs × 400 × 8 = 12800 μs = 12.8 ms

Frame frequency = $\frac{1}{12.8\ \text{ms}}$ = 78.1 Hz

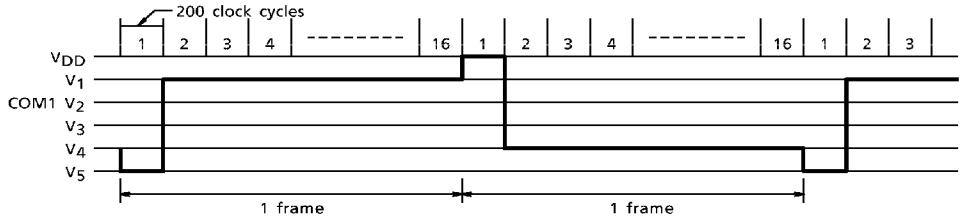
- 1 / 11 duty



1 frame = 4 μs × 400 × 11 = 17600 μs = 17.6 ms

Frame frequency = $\frac{1}{17.6\ \text{ms}}$ = 56.8 Hz

- 1 / 16 duty



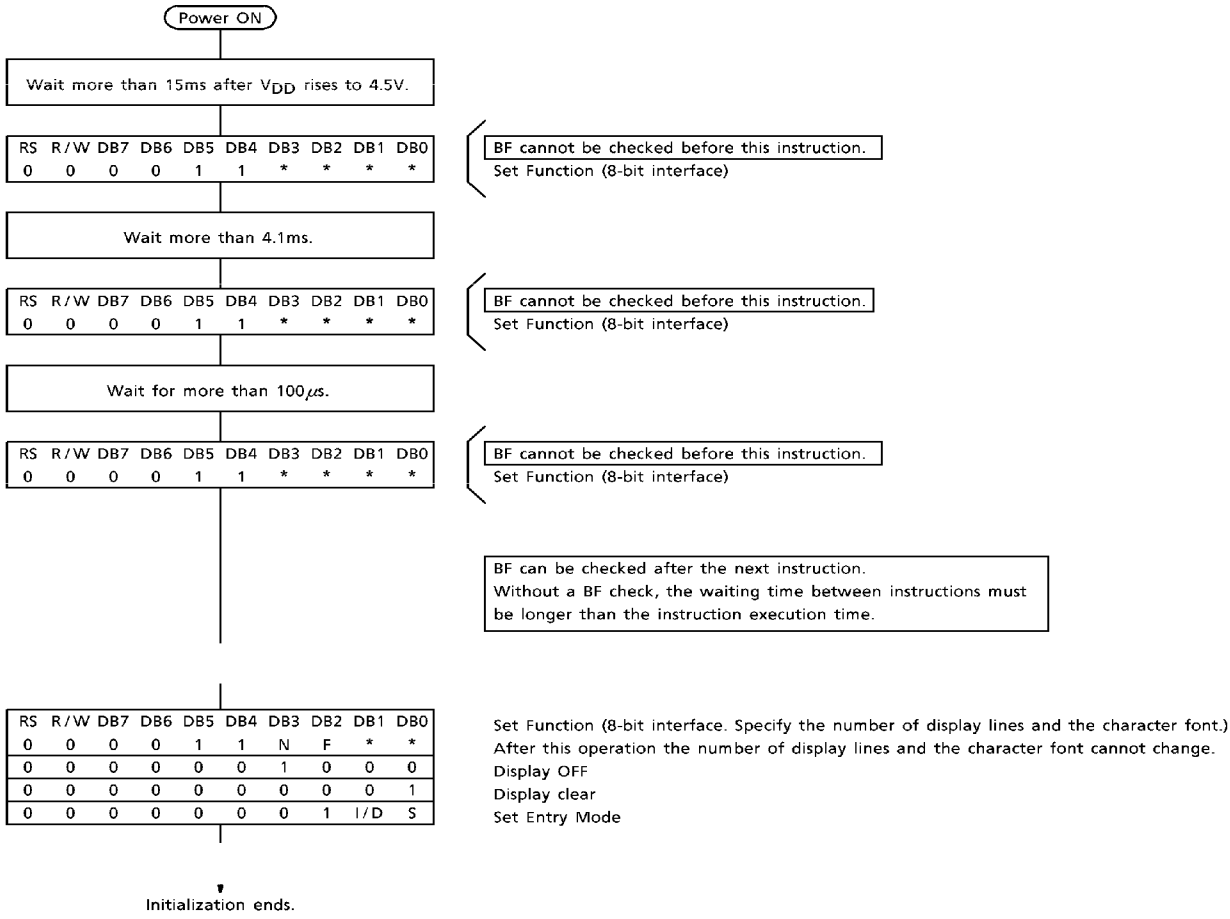
1 frame = 4 μs × 200 × 16 = 12800 μs = 12.8 ms

Frame frequency = $\frac{1}{12.8\ \text{ms}}$ = 78.1 Hz

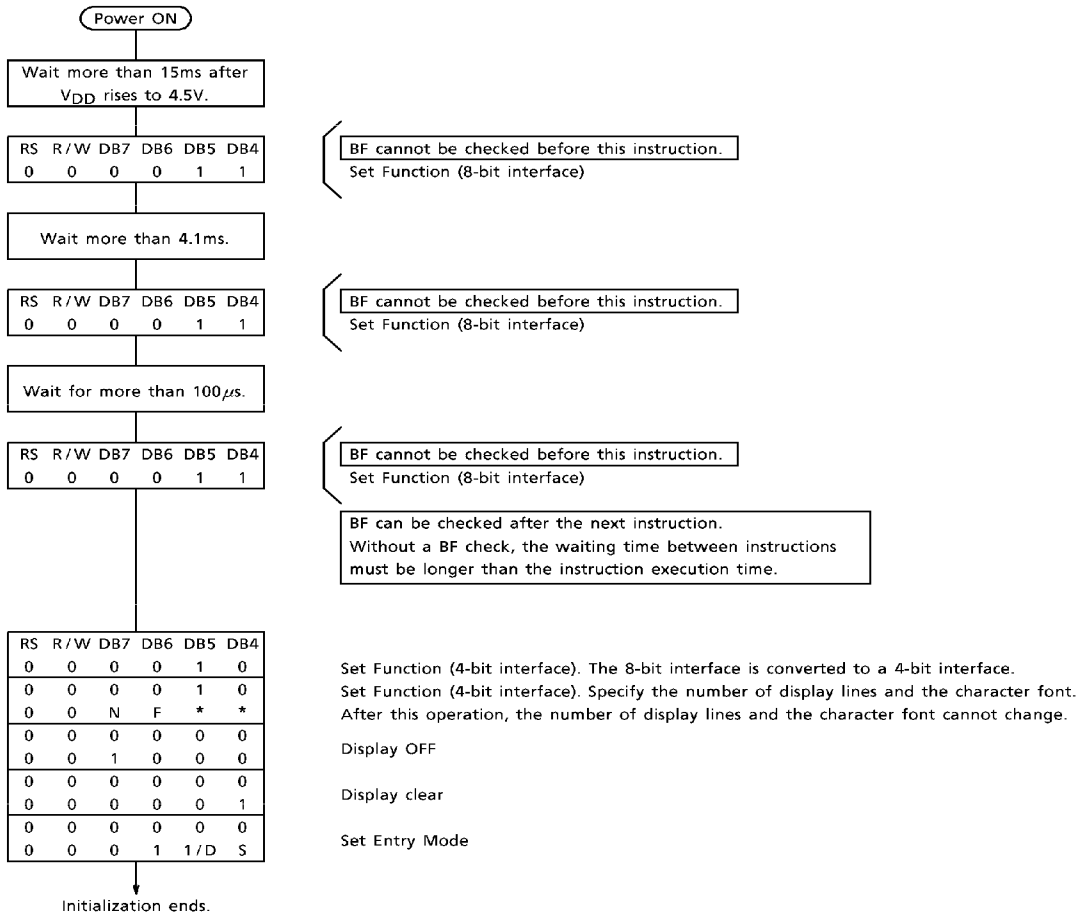
INITIALIZATION BY INSTRUCTION

If the internal reset circuit does not operate correctly, initialization by instruction is required. Use the following initialization sequence.

- 8-bit data interface



- 4-bit data interface



ABSOLUTE MAXIMUM RATINGS (Ta = 25° C)

ITEM	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{DD}	− 0.3 to 7.0	V
Input Voltage	V_{IN}	− 0.3 to V_{DD} + 0.3	V
Operating Temperature	T_{opr}	− 20 to 75	°C
Storage Temperature	T_{stg}	− 55 to 125	°C

(Note 1) All voltage values are referenced to V_{SS} = 0V.

(Note 2) Ensure that the following condition is always maintained.

$$V_{DD} \geqq V_{LC1} \geqq V_{LC2} \geqq V_{LC3} \geqq V_{LC4} \geqq V_{LC5} \geqq V_{SS}$$

ELECTRICAL CHARACTERISTICS

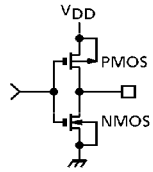
DC CHARACTERISTICS

TEST CONDITIONS (Unless otherwise noted, V_{DD} = 5.0V ± 10%, V_{SS} = 0V, Ta = − 20 to 75°C)

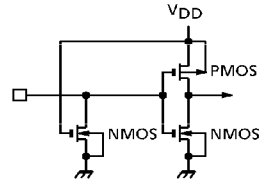
ITEM		SYMBOL	TEST CIR-CUIT	TEST CONDITIONS	MIN	TYP.	MAX	UNIT	PIN NAME
Operating Voltage (1)		V_{DD}	—	—	4.5	—	5.5	V	—
Operating Voltage (2)		V_{LCD}	—	$V_{LCD} = V_{DD} - V_{LC5}$	3.0	—	V_{DD}	V	—
Input Voltage (1)	H Level	V_{IH1}	—	—	V_{DD} − 1.0	—	V_{DD}	V	OSC1, DRI MPU, TS1
	L Level	V_{IL1}	—	—	0	—	1.0	V	TS2
Input Voltage (2)	H Level	V_{IH2}	—	—	2.0	—	—	V	R / W, RS, E DB0 to DB7 $\overline{RST}$
	L Level	V_{IL2}	—	—	—	—	0.8	V	
Output Voltage (1)	H Level	V_{OH1}	—	I_{OH} = − 0.625mA	V_{DD} − 0.3	—	—	V	D, SCP, EO LP, FR OSC2
	L Level	V_{OL1}	—	I_{OL} = 0.625mA	—	—	0.3	V	
Output Voltage (2)	H Level	V_{OH2}	—	I_{OH} = − 1.2mA	2.4	—	—	V	DB0 to DB7
	L Level	V_{OL2}	—	I_{OL} = 2.0mA	—	—	0.4	V	
Row Output Resistance		RCOM	—	I_d = ± 50μA	—	—	20	kΩ	COM1 to COM16
Column Output Resistance		RSEG	—	I_d = ± 50μA	—	—	30	kΩ	SEG1 to SEG104
Input Leakage Current		I_{IL}	—	V_{IN} = 0 to V_{DD} (Note 2)	—	—	1	μA	R / W, RS, E DB0 to DB7, MPU, TS1, TS2, DRI, $\overline{RST}$
Pull-up MOS Current		− I_P	—	V_{DD} = 5V	50	125	250	μA	R / W, RS DB0 to DB7
Power Supply Current (1)		I_{DD1}	—	(Note 3)	—	—	900	μA	V_{DD}
Power Supply Current (2)		I_{DD2}	—	(Note 4)	—	—	700	μA	V_{DD}
Clock Oscillation Frequency		f_{osc}	—	(Note 5)	190	270	350	kHz	OSC1, OSC2
External Clock Frequency		f_{IN}	—	(Note 6)	125	250	350	kHz	OSC1
External Clock Duty		f_{Duty}	—	(Note 7)	45	50	55	%	OSC1
External Clock Rise Time		t_r	—	(Note 8)	—	—	200	ns	OSC1
External Clock Fall Time		t_f	—	(Note 8)	—	—	200	ns	OSC1
Internal Clock Frequency		f_{osc}	—	(Note 9)	245	250	255	kHz	OSC1, OSC2
Pull-up Resistance		R_{up}	—	V_{DD} = 5V	70	100	130	kΩ	$\overline{RST}$
Pull-down Resistance		R_{do}	—	V_{DD} = 5V	70	100	130	kΩ	TS1, TS2

(Note 1) I/O pin details (except for LCD output)

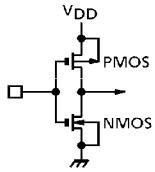
- Output pin : SCP, LP, FR, D, EO



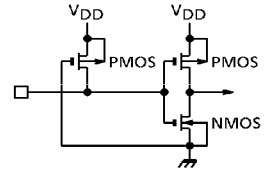
- Input pin : TS1, TS2
  (With pull-down MOS)



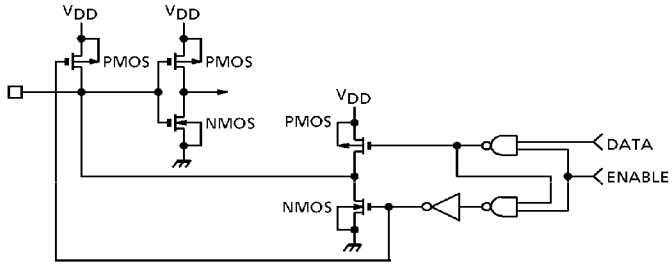
- Input pin : E, MPU, DRI
  (No pull-up MOS)



- Input pin : RS, R/W, $\overline{RST}$
  (With pull-up MOS)



- I/O pin : DB0 to DB7

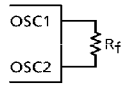


(Note 2) This current does not include pull-up MOS current.

(Note 3) Ceramic Oscillation mode ..... $V_{DD} = 5.0V$, $f_{osc} = 250kHz$

(Note 4) R_f oscillation or external clock mode ..... $V_{DD} = 5.0V$, $f_{osc} = f_{cp} = 270kHz$

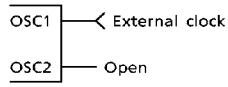
(Note 5) Additional resistor R_f connection



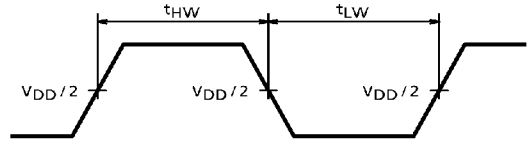
$R_f = 120k\Omega \pm 2\%$

Oscillation frequency depends on OSC1 and OSC2 pin capacitance, therefore wiring must be as short as possible.

(Note 6) External clock input connection

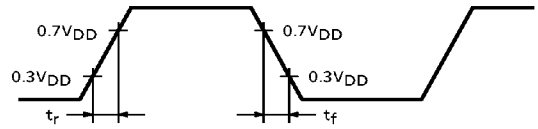


(Note 7) External clock waveform 1

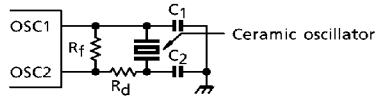


$f_{Duty} = t_{HW} / (t_{HW} + t_{LW}) \times 100$ (%)

(Note 8) External clock waveform 2



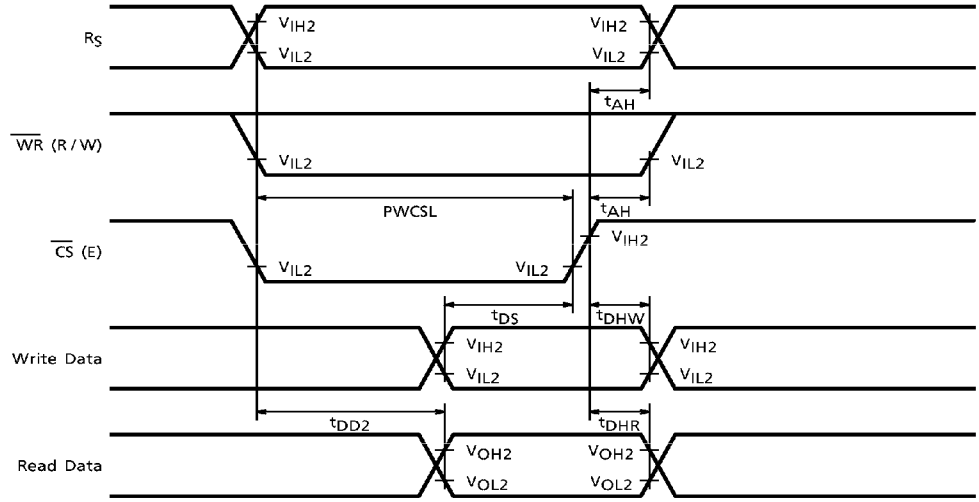
(Note 9) Ceramic oscillator connection



Ceramic oscillator : CSB250D (Murata)
R_f : $1M\Omega \pm 10\%$
R_d : $3.3k\Omega \pm 5\%$
C_1 : $680pF \pm 10\%$
C_2 : $680pF \pm 10\%$

AC CHARACTERISTICS

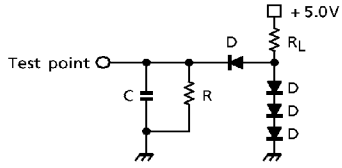
- 80-Series MPU Read / Write operation



TEST CONDITIONS (V_{SS} = 0V, V_{DD} = 5.0V ± 10%, Ta = − 20 to 75°C)

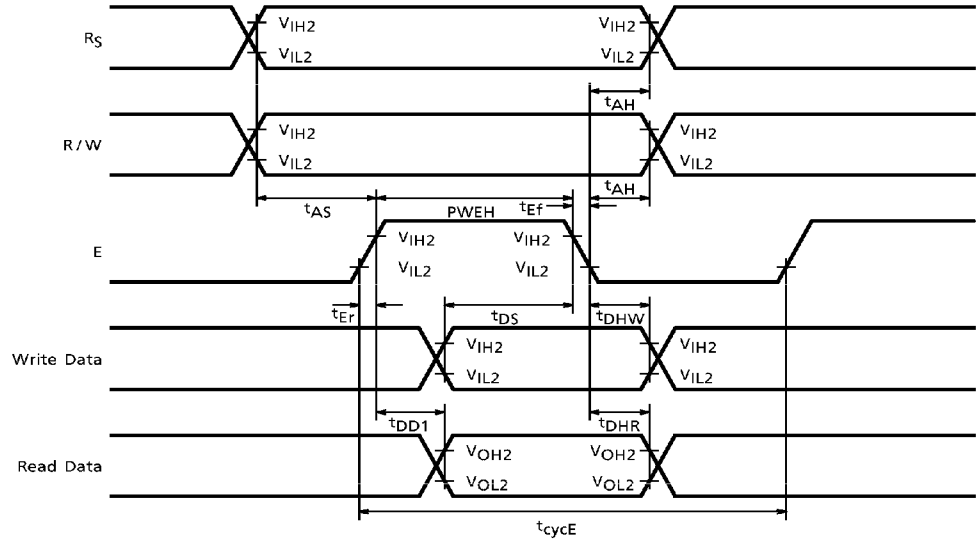
ITEM	SYMBOL	MIN	MAX	UNIT
Chip Select Pulse Width	PWCSL	260	—	ns
Address Hold Time	t_{AH}	10	—	ns
Data Set-up Time	t_{DS}	60	—	ns
Data Hold Time	t_{DHW}	10	—	ns
Data Delay Time	t_{DD2} (Note)	—	180	ns
Data Hold Time	t_{DHR} (Note)	20	—	ns

(Note) With load circuit connected (DB0 to DB7)



R_L = 2.4kΩ
R = 10kΩ
C = 130pF (including wiring capacitance)
D = 1S1588

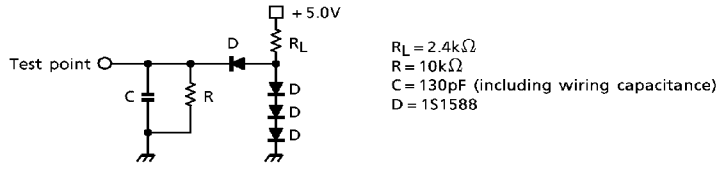
- 68-Series MPU Read / Write operation



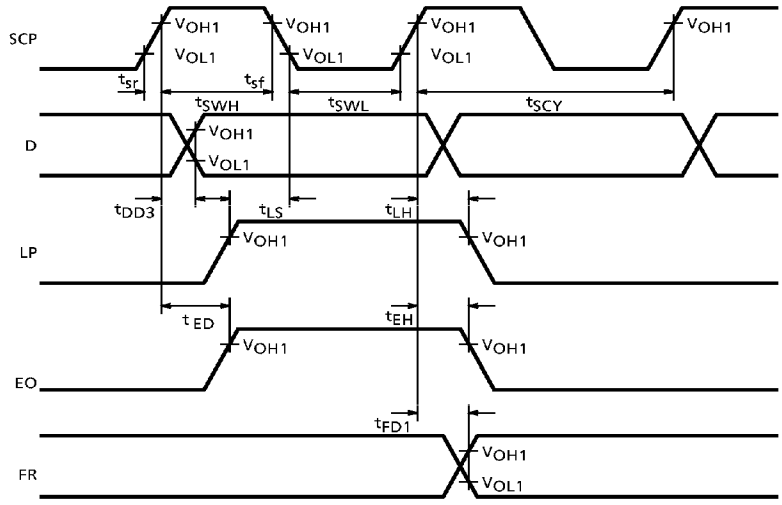
TEST CONDITIONS (V_{SS} = 0V, V_{DD} = 5.0V ± 10%, Ta = − 20 to 75°C)

ITEM	SYMBOL	MIN	MAX	UNIT
Enable Cycle Time	t_{cycE}	500	—	ns
Enable Pulse Width	PWEH	220	—	ns
Enable Rise / Fall Time	t_{Er}, t_{Ef}	—	20	ns
Address Set-up Time	t_{AS}	40	—	ns
Address Hold Time	t_{AH}	10	—	ns
Data Set-up Time	t_{DS}	60	—	ns
Data Hold Time	t_{DHW}	10	—	ns
Data Delay Time	t_{DD1} (Note)	—	120	ns
Data Hold Time	t_{DHR} (Note)	20	—	ns

(Note) With load circuit connected (DB0 to DB7)



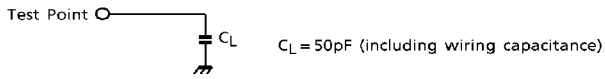
- Extension driver interface timing (e.g. T6A41, T6A92)



TEST CONDITIONS (V_{SS} = 0V, V_{DD} = 5.0V ± 10%, Ta = – 20 to 75°C)

ITEM	SYMBOL	MIN	MAX	UNIT
SCP Cycle Time	t_{SCY}	2000	—	ns
SCP Pulse Width	$t_{SWH, L}$	800	—	ns
SCP Rise / Fall Time	t_{sr}, t_{sf}	—	100	ns
Data Delay Time	t_{DD3} (Note)	—	100	ns
LP Set-up Time	t_{LS}	– 120	0	ns
LP Hold Time	t_{LH} (Note)	– 100	0	ns
FR Delay Time	t_{FD1} (Note)	– 100	100	ns
EO Delay Time	t_{ED} (Note)	—	100	ns
EO Hold Time	t_{EH} (Note)	– 100	0	ns

(Note) With load circuit connected



APPLICATION CIRCUIT